Course: CS 223 Digital Design
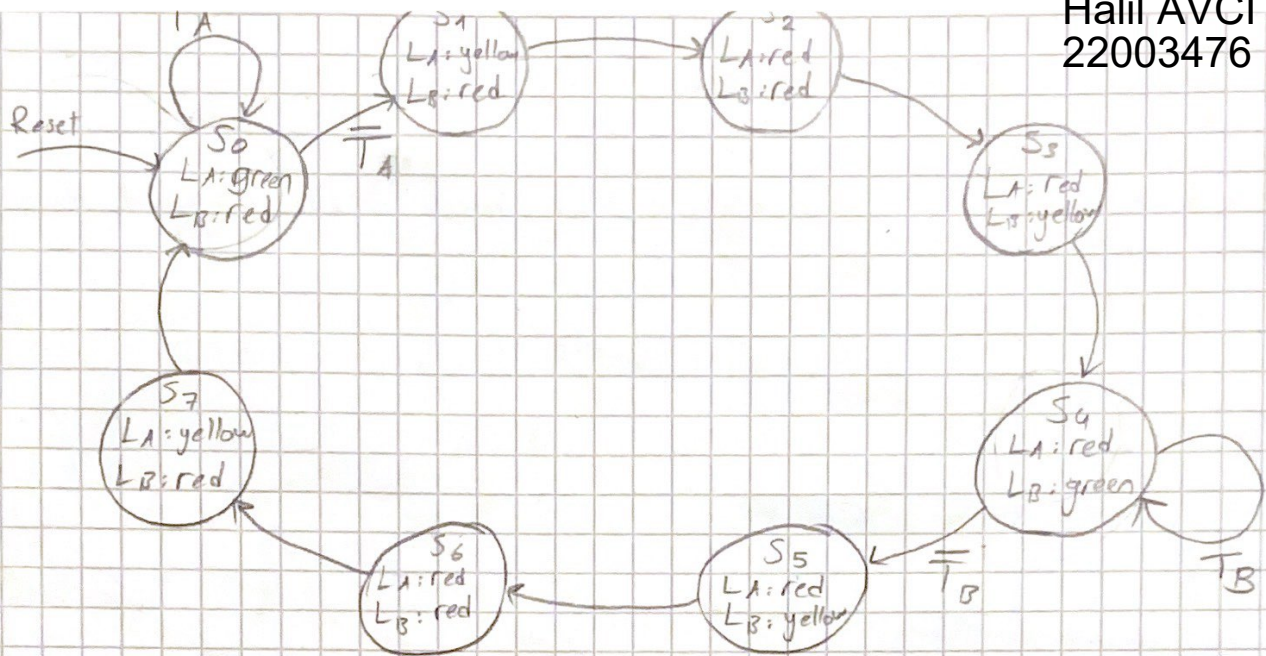
Section: 6

Lab: 5

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State diagram (finite state machine):

- Reset → S_0 (L_A: green, L_B: red)
- S_1 (L_A: yellow, L_B: red)
- S_2 (L_A: red, L_B: red)
- S_3 (L_A: red, L_B: yellow)
- S_4 (L_A: red, L_B: green)
- S_5 (L_A: red, L_B: yellow)
- S_6 (L_A: red, L_B: red)
- S_7 (L_A: yellow, L_B: red)

Self-loop on S_0 with T_A, exit with $\overline{T_A}$. Self-loop on S_4 with T_B, exit with $\overline{T_B}$.

State Encodings

States	Encoding $S_{2:0}$
S0	000
S1	001
S2	010
S3	011
S4	100
S5	101
S6	110
S7	111

Output Encodings

Outputs	Encoding $L_{1:0}$
green	00
yellow	01
red	10

☆One flip flop would be enough.

State Transition Table

Current State			Inputs		Next State		
S_2	S_1	S_0	T_A	T_B	S_2'	S_1'	S_0'
0	0	0	0	X	0	0	1
0	0	0	1	X	0	0	0
0	0	1	X	X	0	1	0
0	1	0	X	X	0	1	1
0	1	1	X	X	1	0	0
1	0	0	X	0	1	0	1
1	0	0	X	1	1	0	0
1	0	1	X	X	1	1	0
1	1	0	X	X	1	1	1
1	1	1	X	X	0	0	0

Output Table

Current State			Outputs			
S_2	S_1	S_0	L_{A1}	L_{A0}	L_{B1}	L_{B0}
0	0	0	0	0	1	0
0	0	1	0	1	1	0
0	1	0	1	0	1	0
0	1	1	1	0	0	1
1	0	0	1	0	0	0
1	0	1	1	0	0	1
1	1	0	1	0	1	0
1	1	1	0	1	1	0

$$S_2' = S_2 \overline{S_1} + S_2 \overline{S_0} + \overline{S_2} S_1 S_0$$

$$S_1' = \overline{S_1} S_0 + S_1 \overline{S_0} = S_1 \oplus S_0$$

$$S_0' = S_1 \overline{S_0} + \overline{S_2} \, \overline{S_1} \, \overline{S_0} \, \overline{T_A} + S_2 \overline{S_1} \, \overline{S_0} \, \overline{T_B}$$

$$L_{A1} = S_2 \overline{S_1} + \overline{S_2} S_1 + S_1 \overline{S_0}$$

$$L_{A0} = \overline{S_2} \, \overline{S_1} S_0 + S_2 S_1 S_0$$

$$L_{B1} = \overline{S_2} \, \overline{S_1} + S_2 S_1 + S_1 \overline{S_0}$$

$$L_{B0} = \overline{S_2} S_1 S_0 + S_2 \overline{S_1} S_0$$

Next State Logic
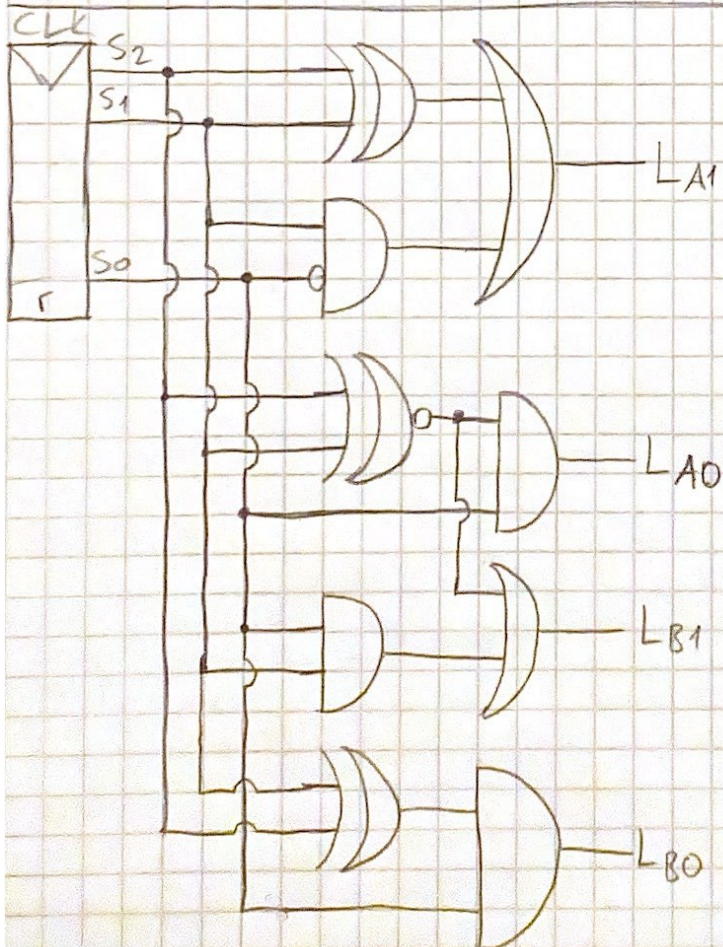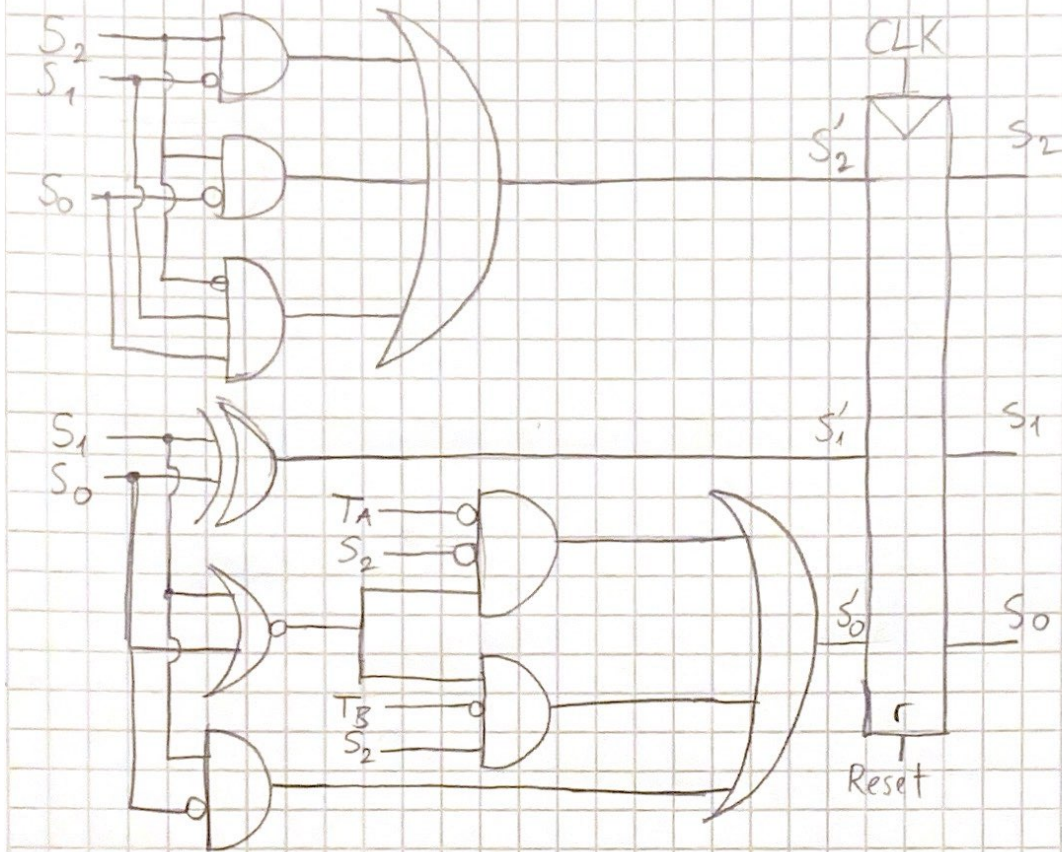
Output Logic
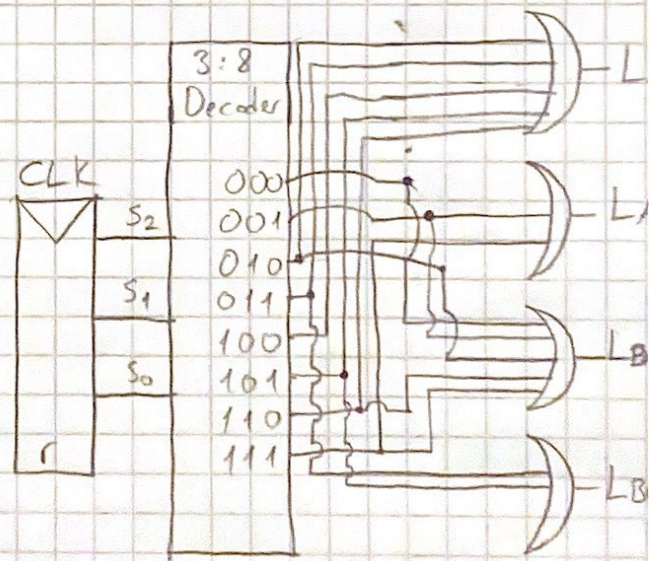
Output Logic with Decoder

Labels visible in the diagrams: S_2, S_1, S_0, CLK, S_2', S_1', S_0', Reset, T_A, T_B, r, L_{A1}, L_{A0}, L_{B1}, L_{B0}, 3:8 Decoder, 000, 001, 010, 011, 100, 101, 110, 111, L, L_A, L_B