ÇUKUROVA ÜNİVERSİTESİ

Department
of
Computer Engineering

# CEN 263
# Digital Design

Autumn 2024

Lecture 0

# Outlines

- Administration
- Scope of Lecture

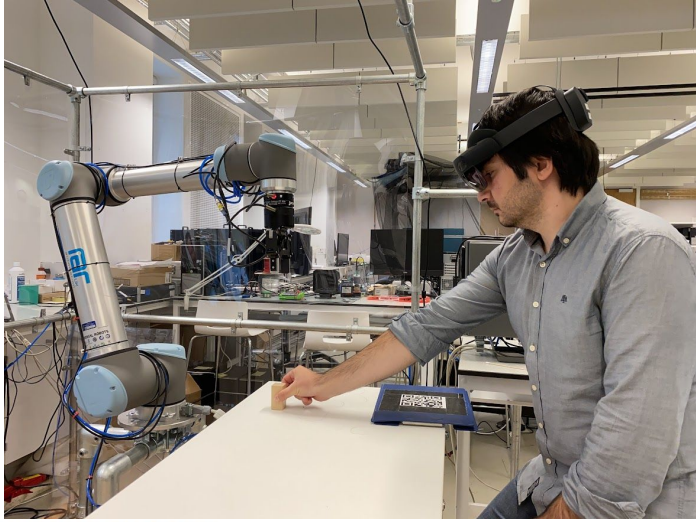
# Administration

- Lecturer:
  Dr Yunus Emre Cogurcu

- Lab Lead:
  Res. Asst. Fırat Kumru

# Administration

## Dr Yunus Emre Cogurcu



| Graduation | Degree |
|---|---|
| 2024 | Ph.D., Computer Science, The University of Sheffield, UK |
| 2022 | MPA, Public Administration, Social Sciences University of Ankara, Türkiye |
| 2018 | M.Sc., Computer Science, The University of Sheffield, UK |
| 2018 | M.Sc., Applied Operations Research, Gazi University, Türkiye |
| 2014 | B.Sc., Computer Engineering, Ege University, Türkiye |

# Administration

- Lecture web site: https://ebs.cu.edu.tr/En/Course/Information/627871

- Office Hour: By appointment
  - ycogurcu@cu.edu.tr

# Administration

- Lecture hours:
    - Monday - Afternoon (First Group)
    - Monday - Evening (Second Group)
- Lectures are at R2-308
- Labs are at YAZILIM 2

# Scope of Lecture

- No prerequisite lecture

- Textbook
  - David Money Harris, Sarah L. Harris, Digital Design and Computer Architecture, 2nd ed. Morgan Kaufmann, 2012. (Textbook)
  - Link of book

# Scope of Lecture

- Lecture description:
  - The introduction to digital design course covers **combinational and sequential circuits**, **memory and logic arrays**, and an introduction to **processor architecture** and includes a **weekly laboratory**.
  - **Verilog and SystemVerilog** hardware description language will be used throughout the semester to model and implement digital designs.

# Scope of Lecture

- **Lecture contents:**
  - Week 1: Number systems, Binary numbers, Logic levels, transistors, gates, Boolean expressions.
  - Week 2: Combinational logic: Boolean algebra, simplification of Boolean expressions.
  - Week 3: Karnaugh Maps (K-Maps) for Simplification. Minimization Techniques for Boolean Expressions.
  - Week 4: Combinational building blocks, multiplexers, decoders, propagation delays. Introduction to Verilog & SystemVerilog.
  - Week 5: Sequential logic: SR latch, D-latch, D flip-flop, synchronous sequential circuits. Verilog & SystemVerilog modeling.

# Scope of Lecture

- **Lecture contents:**
  - Week 6: Registers and Counters.
  - Week 7: Timing and Control Circuits. Clock Signals, Timing Diagrams.
  - Week 8: Finite State Machine (FSM) design, Moore and Mealy models.
  - Week 9: Memory and Programmable Logic Devices (PLDs). Memory Types: ROM, RAM, SRAM, DRAM
  - Week 10: Arithmetic Circuits: Binary Multipliers and ALU Design
  - Week 11: Combining Combinational and Sequential Circuits. Hierarchical Design Approach

# Scope of Lecture

| WEEK | TOPICS COVERED | READINGS |
|---|---|---|
| 1 | Introduction, digital values, number systems: decimal, binary and hexadecimal | Digital Design and Computer Architecture DDCA 1.1 - 1.4 |
| 2 | Logic gates and physical characteristics, CMOS transistors, power consumption, Boolean algebra, Boolean equations, canonical forms | DDCA 1.5 - 1.9, 2.1 - 2.3 (excluding: 1.6.4, 1.6.5, 1.7.7, 1.7.8) |
| 3 | Combinational logic, hardware reduction, X and Z logic values, introduction to SystemVerilog | DDCA 2.4 - 2.6, 4.1 - 4.2 |
| 4 | Karnaugh maps, multiplexers and decoders, combinational timing and non-ideal behavior, SystemVerilog modeling | DDCA 2.7 - 2.9, 4.3 (excluding: 2.9.2) |
| 5 | Latches & flip-flops, basic register, synchronous logic design, SystemVerilog modeling | DDCA 3.1 - 3.3, 4.4 - 4.5 |

# Scope of Lecture

| | | |
|---|---|---|
| 6 | Finite state machines, FSM design, state encoding, Mealy vs. Moore models, SystemVerilog modeling | DDCA 3.4, 4.6 (excluding: 3.4.4) |
| 7 | FSM examples | na |
| 8 | Timing | DDCA 3.5 (excluding: 3.5.4, 3.5.5, 3.5.6, 3.6) |
| 9 | Arithmetic functions, adders, subtractors, comparators, shifters, ALU, SystemVerilog models MIDTERM EXAM | DDCA 5.1 - 5.2 (excluding Prefix Adder, 5.2.6, 5.2.7) |
| 10 | Registers, shift registers, counters, timers, SystemVerilog models | DDCA 5.4 |
| 11 | Memory components, static & dynamic RAM, ROM/PROM, SystemVerilog models | DDCA 5.5 |

# Scope of Lecture

- **Lecture grading:**
  - **Attendance of Lecture and Labs: 10 %**
  - **Midterm Exam: 40%**
  - **Final Exam: 50%**

# Scope of Lecture

- **IMPORTANT !!!:**

- **Only original and unmarked textbooks will be allowed in the midterm AND OR final exams. If you have any notes OR drawings OR markings OR etc. on your textbook, you will not be able to use it during the midterm AND OR final exams.**

- **You cannot use your own notes in the exams.**

- **You cannot use a photocopy or paper copy of the textbook in exams.**

# Scope of Lecture

- **Lecture GenAI Policy (Chatgpt etc.):**
    - Using AI models for coursework including lab work is allowed.