System Specifications

Parameter	Specifications
Output Power	20 kW
Output Voltage	Three Phase 380 Vac
Output Frequency	50 Hz
Output Current	39 Amper (25 kW) -78 Amper With Parallel Sic at 25 °C
Nominal Input Voltage	700 Vdc
Input Voltage Range	550 to 1000 Volt
Switching Frequency	20-30 kHz
Efficiency	?
Power Density	?
Topology	Traditional Two Level
Switching Device	Silicon Carbide Mosfet

Block Diagram

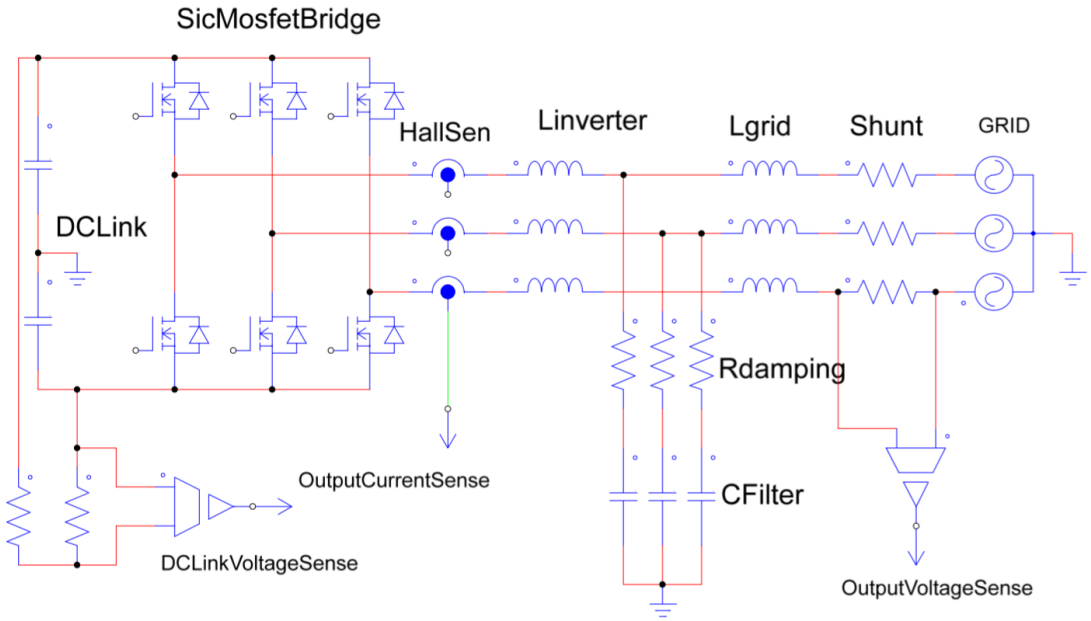


Figure 1.1.Block Diagram of System

Optimum DC Link Voltage

DC link voltage, Vdc has effects on some features of the inverter, such as efficiency and high frequency current ripple on the filter inductor. For the same output filter inductance value, higher DC link voltage results in increase of the switching frequency current ripple, which increase magnetic losses in the inductor and current harmonic distortion at the switching frequency. Value of DC link voltage, which is MPPT converter output, and VSI input is kept constant by the inverter in the entire range of operation, no matter the amount of PV power. VSI is supposed to transfer all the power from MPPT converter, into grid and by keeping the value of the DC link constant, this duty is accomplished. As the solar power increases, power output of the MPPT converter increases, and this condition results in the increase of the DC link voltage. As the Vdc increases, M, which is the modulation index, decreases when the output voltage value is constant.

$$M = \frac{2\sqrt{2}}{\sqrt{3}} \frac{V}{V_{dc}}$$

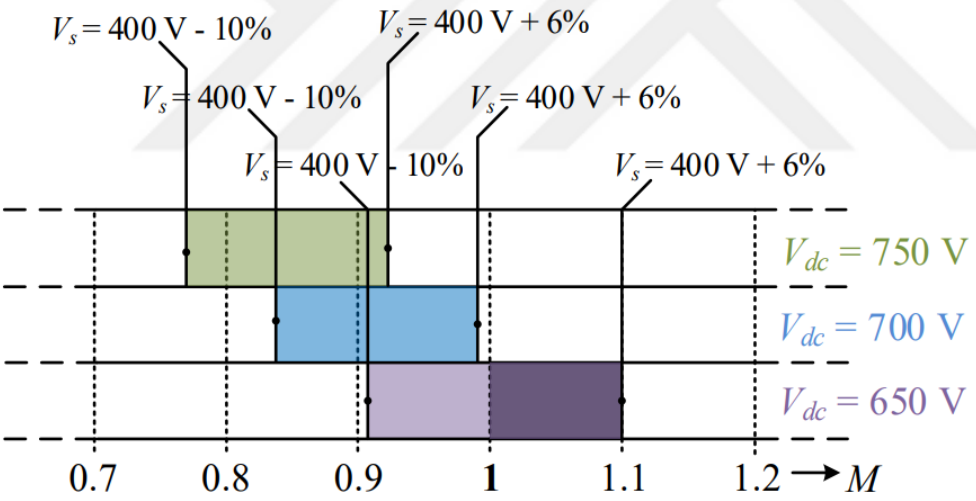


Figure 1. 2. Range of variation of modulation index M for different fixed values of DC bus voltage and for connected 400 V l-to-l, 50 Hz grid voltage variations upper and lower limits as 400 V +6% -10% as specified in IEC 60038 2002-07 Standard Voltages for the supply side voltage range

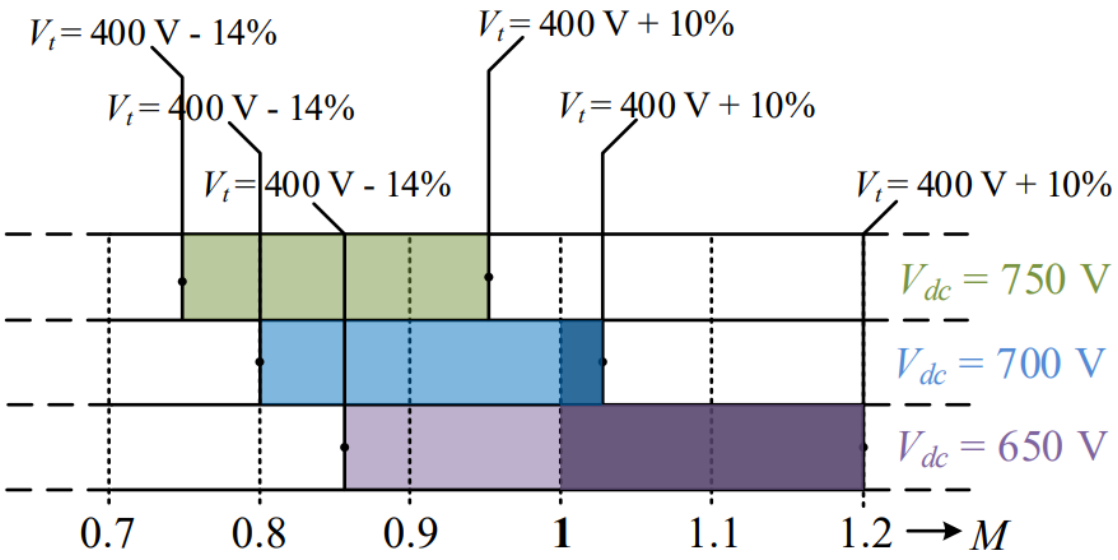


Figure 1. 3. Range of variation of modulation index M for different fixed values of DC bus voltage and for connected 400 V l-to-l, 50 Hz grid voltage variations upper and lower limits as 400 V +10% -14% as specified in IEC 60038 2002-07 Standard Voltages for the utilization voltage range

According to these plots, which are shown in Figures it can be understood that optimum value for DC link voltage is around 700 V. For the supply side voltage upper and lower band limits, inverter does not goes into overmodulation, which causes low order harmonics. For the utilization voltage range, inverter works in slightly over-modulated at the upper band limit, which is acceptable. For 650 V DC bus voltage, inverter works highly over-modulated at the upper band limits of both supply side voltage and utilization voltage, which is unacceptable since low order harmonics grow dramatically. In the case of 750 V DC link voltage, inverter does not does into over-modulation in any case for both supply side and utilization side voltage limits, but modulation index M, is too low, which increases losses for the same switching frequency and same output filter. By considering these reasons listed above. DC link voltage is designated as 700 V

Optimum Switching Frequency

For many modulation techniques, such as SPWM and SVPWM, as the switching frequency increases, frequency of high order harmonics, which are also known as side-band harmonics occurring both sides of switching frequency and its' multiplies, also increases .So that, output filter corner frequency, in other words resonant frequency of LCL filter, can be set to a higher value in order to reduce the volume of passive components. However, increasing switching frequency has a drawback in terms of losses. As the switching frequency increases, switching loss occurring in power semiconductors proportionally increases with the frequency. Traditional Si based power semiconductors, such as IGBT, has significantly larger turn-on, turnoff times with respect to SiC based power semiconductor. So that, with the emergence of SiC power MOSFETs, switching frequency can be increased more, in comparison to IGBT switching frequency, for the same power rating of the inverter and for the same switching loss. But, benefits of increasing switching frequency, in terms of lowering the size of passive components, start to saturate at one point in the view point of control stability. Reducing inductor component of output filter causes stability problems, since voltage and phase difference between inverter output voltage and grid voltage is necessary to control power flow to grid. Low order voltage harmonics in the grid cause low order current flows, despite control circuitry current loop attenuation. Because of this reasons, output filter inductance has a minimum value which has shown in output filter design section, so that increasing switching frequency too much has no advantage after one point. In order to find optimum switching frequency, 10 kHz switching frequency has almost no advantage in terms of losses and LCL filter size needs to be increased significantly. LCL filter copper loss increases dramatically, in order to have the same switching current ripple. In the case of 30 kHz switching frequency, LCL filter volume reduction according to 20 kHz switching frequency is not very remarkable, in addition, switching loss of SiC MOSFETs starts to be a considerable amount. Also, because of mentioned control loop stability problems, due to insufficient impedance between inverter output and grid voltage, 30 kHz switching frequency is not considered as advantageous.

DC Bus Capacitance Calculation and Capacitor Selection

When choosing DC link capacitor of the three-phase grid connected inverter, some parameters such as DC link capacitance, rated DC link voltage, capacitor ripple current and life time of capacitor need to be considered. Capacitance of DC link is a key feature, that affects DC link high frequency voltage ripple due to switching current ripple, and DC link capacitance is typically selected as to meet the design criteria of 1 or 2% ripple voltage on the DC link voltage. Maximum power transfer from DC bus to grid in a single switching period, is given in the following formula.

$$\Delta W = T \text{ x } Pmax$$

According to maximum power transfer, DC link capacitance, DC link voltage and ripple voltage on the DC link are given as;

$$\Delta V_{dc} = \frac{\Delta W}{V_{dc} x C_{min}}$$

Minimum DC link capacitance can be calculated, in order to meet the required ripple at the maximum power transferring to grid as;

$$C_{min} = \frac{TxPmax}{V_{dc} x \Delta V_{dc}}$$

Even though installed PV array power rating is 20kW, inverter is designed to transfer 30 kW power to grid. Because of that, calculations made for 30 kW maximum power. For 30 kW Pmax, 30 kHz switching frequency, 700 V DC link voltage and 1% ΔVdc, Cmin is calculated as 480 uF. Other criteria to select DC bus capacitor, are equivalent series inductor, ESL, and equivalent series resistance, ESR, value of the capacitor. ESR value is critical in a way that determining ripple current capacity of the capacitor. Lower ESR means higher ripple current capacity, so less thermal stress on the capacitor, in order to increase the life time of the capacitor. ESL value of capacitor is important, in terms of voltage spikes on SiC MOSFETs, during turn off. By considering all the reasons listed above, we choose

Specification	C3D2H226JB00C00	K055002210PM0E040
Type	Metallized Polypropylene	Electrolytic
Irms	10 Amper	950mAmper

ESR(Equivalent Series Resistance)	5 m ohm	455m ohm
Capacity	22uF	220uF
Voltage	500 Volt DC	500 Volt DC
Life cycle	100 000 hour at 70 Degree	5000 hour at 105 Degree

For 480 uF 1000 volt DC link system can be made by film and electrolytic capacitor series and parallel combination this will help us in these condition.

- High ESR value of electrlytic capacitor will be decrease
- Low ripple current of electrlytic capacitor will be increase
- Because of Low capacity of film capacitor, if we use just film capacitor we have to use 86 film capacitor to reach 480uf so this will increase budget and PCB size
- High capacitance value of electrolytic capacitor will help us reduce the budget and PCB size effectively

To Reach 480 uF we will connect 2 electrolytic capacitor in series for 1000v voltage value and we will parallel 4 series connected branch it will 440 uF and we will connect in series 2 film capacitor and we will connect 4 series connected branch it will 44uF and total will be 484uF Connection can seen on figure.

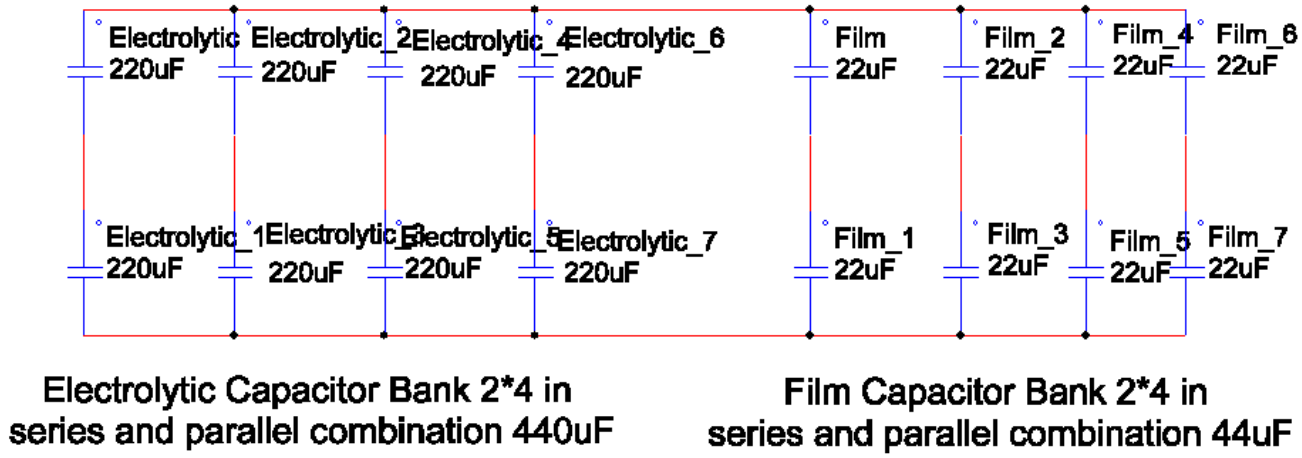
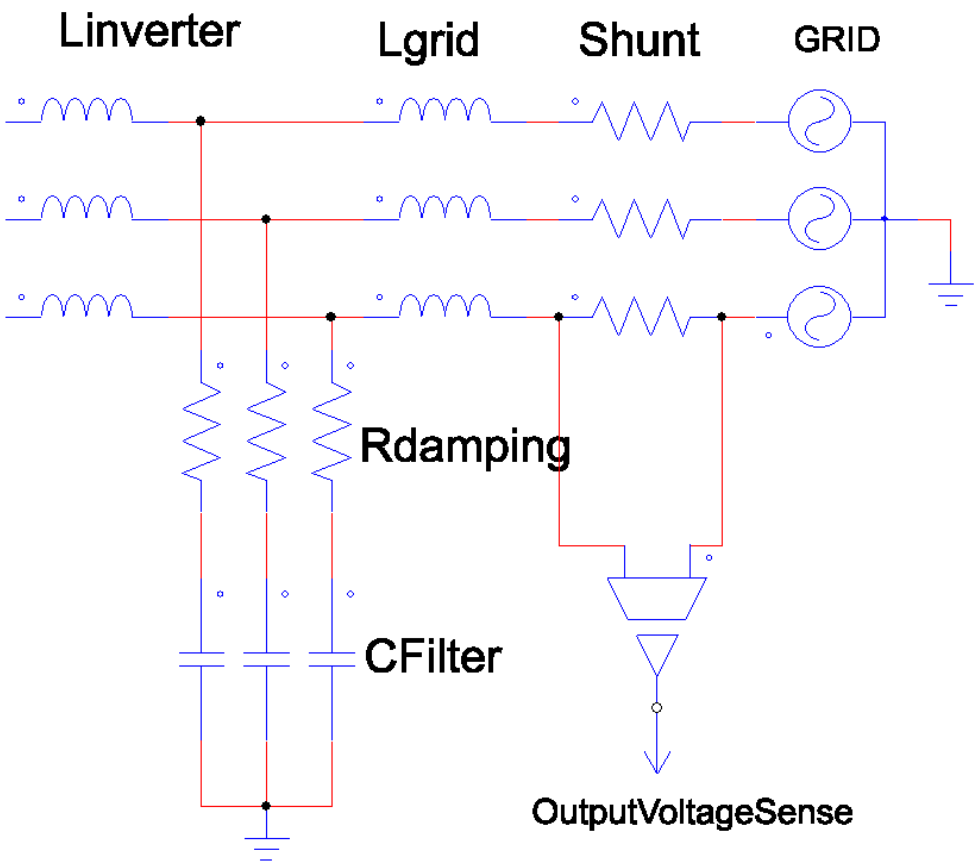


Figure 1. 4. Capacitor Connection

Output Filter Design and Inductor Design



Şekil 1.5. Filter Design

One of the key benefits of using SiC MOSFETs is the ability to increase the switching frequency of the power stage significantly versus traditional Si-based switching elements. This increased switching frequency has a direct impact on the inverter's output filter resonant design, which needs to be accounted for. To ensure that the filter is designed correctly around this switch frequency, this known mathematical model is used in this design. The primary component is the inverter inductor, or L inv, which can be derived using

$$L_{inv} = \frac{V_{dc}}{8 \times f_{sw} \times I_{grid\_rated} \times \%ripple}$$

$$L_{inv} = \frac{1000}{8 \times 30kHz \times 39A \times \%40} = 267\mu H$$

The sizing of the primary filter capacitor is handled in a similar fashion using

$$C_f = \frac{\%x \times Q_{rated}}{2 \times \pi \times 50Hz \times \frac{380^2}{\sqrt{3}^2}}$$

$$C_f = \frac{\%5 \times \frac{20kW}{3}}{2 \times \pi \times 50Hz \times \frac{380^2}{\sqrt{3}^2}} = 22\mu F$$

For the remainder of the filter design, determine the values by defining the attenuation factor between the allowable ripple in grid inductor and the inverter inductor. This factor needs to be minimized while still maintaining a stable and cost effective total filter. By assuming an attenuation factor, an r value, which defines the ratio between the two inductors, is determined using

$$I_{att} = \frac{1}{|1 + r \times (1 - L_{inv} \times C_f \times (2 \times \pi \times f_{sw})^2 \times x)|} \times 100$$

To obtain an attenuation factor of 10%, and using the earlier derived values, the value of r can be evaluated by rewriting this to be:

$$r = \left| \frac{\frac{1}{\%10} - 1}{1 - 267\mu H \times 22\mu F \times (2 \times \pi \times 30kHz)^2 \times \%5} \right| = \sim\%5.4$$

The resultant value for L grid is then

$$L_{grid} = r \times L_{inv}$$

$$L_{grid} = \sim\%5.4 \times 267\mu H = 14.4\mu H$$

The filter design can be validated by determining its resonant frequency (Fres). A good criteria for ensuring a stable Fres is that it is an order of magnitude above the line

frequency and less than half the switching frequency. This criteria avoids issues in the upper and lower harmonic spectrums. The resonant frequency of the filter is defined using

$$F_{res} = \frac{\frac{1}{\sqrt{C_f \times \frac{L_{grid} \times L_{inv}}{L_{grid} + L_{inv}}}}}{2 \times \pi}$$

$$F_{res} = \frac{\frac{1}{\sqrt{22uF \times \frac{14.4\mu H \times 267uH}{14.4\mu H + 267uH}}}}{2 \times \pi} = 9.179kHz$$

The remaining value to determine is the passive damping that must be added to avoid oscillation. Generally, a damping resistor at the same relative order of magnitude as the C f impedance at resonance is suitable. This impedance is easily derived using

$$R_d = \frac{1}{6 \times \pi \times F_{res} \times C_f}$$

$$R_d = \frac{1}{6 \times \pi \times 9.179kHz \times 22uF} = 0.262ohm$$

With the filter being one of the major contributors to the size and weight of a solar inverter, ensure that the individual components are correctly sized. The increase in the system switching speed provided by the SiC MOSFETs has already resulted in an inverter inductor that is of much smaller value than normal. In Equation , the switching frequency is in the denominator. Any increase in switch frequency, all else being the same, results in an inverse relationship. Looking at the simplified equation for the inductance of a given inductor, there is a positive relationship between inductance and inductor cross sectional area by a number of turns. Both have a direct effect on the size of the component.

$$L = \frac{0.4 \times \pi \times \mu \times N^2 \times A \times 10^{-2}}{l}$$

where

• μ is core permeability

• N is the number of turns

• A is the cross sectional area

• l is the mean magnetic path length

The starting point for evaluating a solution to the variables in Equation is to determine a valid core material and subsequent permeability. The core manufacturer typically has a range of suitable materials with selection criteria based on the design inductance and the inductor current. For this design, the nominal inductor current (with an overload factor of 105%) is defined as:

$$I_{ind\_nom} = \frac{KVA_{out} \times \%105}{\sqrt{3}V_{grid}}$$

$$I_{ind\_nom} = \frac{20kVA \times \%105}{\sqrt{3} \times 380} = 31.9\ Amper$$

Using a selection guide for a toroidal inductor core manufacturer, at 267 μH, the core permeability comes to 20 μH. The core also provides a value for the inductance factor, AL , which enables a quick path to selecting the number of turns.

$$N = \sqrt{\frac{L \times 10^3}{A_L}}$$

$$N = \sqrt{\frac{267 \times 10^3}{49}} = 74$$

One last piece of information required for the inductor design is the winding wire size. This size is easily computed using the nominal inductor current rating. Using copper, with a current carrying density of 4 A/mm, this inductor requires a cross sectional area of:

$$A_w = \frac{I_{ind\_nom}}{4} = \frac{31.9}{4} = 7.97mm^2$$

This area is an equivalent to American Wire Gauge #8, which has a cross sectional area of 8.37 mm2 . With the flat 8 AWG winding, the total length of each winding is determined to be 68 mm. At this point, the DC resistance of the inductor can be calculated using Pouillet's Law:

$$R_{DC} = p\frac{l}{A}$$

$$R_{DC} = (10^{-9} \times 17) \times \frac{74 \times 68\,mm \times 10^{-3}}{7.97mm^2 \times 10^{-6}} = 0.0107ohm$$

To determine the AC resistance, first calculate the skin depth at the inverter switching frequency:

$$S_d = 1000 \times \sqrt{\frac{p}{\pi \times f_{sw} \times \mu_0}}$$

$$S_d = 1000 \times \sqrt{\frac{10^{-9} \times 17}{\pi \times 30kHz \times 4 \times \pi \times 10^{-7}}} = 0.37mm$$

RAC is then determined by RDC, Sd , and Ss , which is the equivalent square conductor width.

$$R_{AC} = R_{DC} \times \frac{1}{2} \times (\frac{S_s}{S_d}) \times (\frac{sinh\left(\frac{S_s}{S_d}\right) + sin\left(\frac{S_s}{S_d}\right)}{cosh\left(\frac{S_s}{S_d}\right) - cos\left(\frac{S_s}{S_d}\right)}) = 0.033ohm$$

This determination of RAC helps determine total system losses.

Sic Mosfet Selection

We choose LSIC1MO120E0080 part number silicon carbide mosfet from littelfuse company, Features and application area of this switch

• Optimized for highfrequency, high-efficiency applications

• Extremely low gate charge and output capacitance

• Low gate resistance for high-frequency switching

• Normally-off operation at all temperatures • Ultra-low on-resistance

• High-frequency applications

• Solar Inverters

• Switch Mode Power Supplies

• UPS • Motor Drives

• High Voltage DC/DC Converters

• Battery Chargers

• Induction Heating

Characteristics	Value
Drain Source Voltage	1200 Volt
Drain Source Open Resistance	80 mOhm
Continuous Drain Current	39 Amper at 25℃
Pulsed Drain Current	80 Amper at 25℃
Power Dissipation	179 W
Operating Junction Temperature	-55 to 155℃
Gate-source Voltage	-5 to 20 Volt

Gate Driver Selection and Dedicated Gate Driver Board

We choose TLP152 part number photocoupler gate driver from Toshiba brand, this gate driver will make signal isolation between control and Power Circuit.

Characteristics	Value
Output peak current	±2.5 A (max)
Operating temperature	-40 to 100 ℃
Supply current	3.0 mA (max)
Supply voltage	10 to 30 V
Threshold input current	7.5 mA (max)
Isolation voltage	3750 Vrms (min)

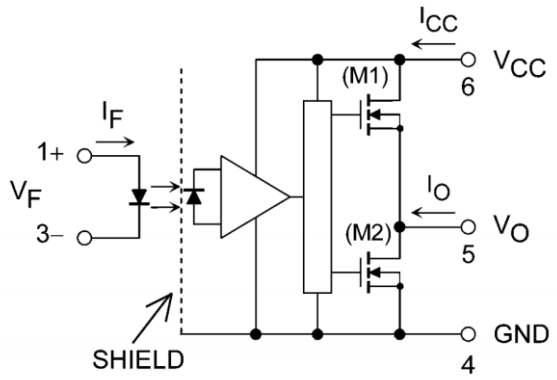
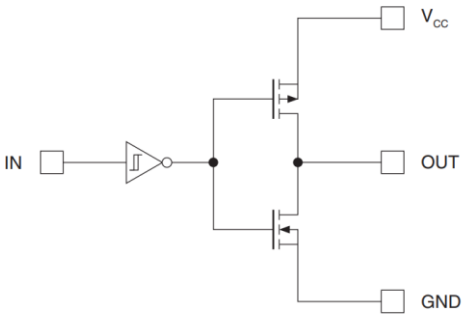


Figure 1. 4. TLP 152 Internal Structure

SiC Mosfets can be driven at very high frequencies and gate resistor requirement is very low according to the traditional ones. In this inverter gate resistors will be 2 ohm and the total gate to source voltage will be +20/-5 if we make a rough calculation for 2 ohm gate resistance we need 25/2=12.5 Amper gate current driver So we choose non isolated ultra fast 14 Amper gate driver from IXDN brand it name is ixdn614si

Characteristics	Value
Output peak current	±14 A (max)
Operating temperature	-55 to 150 ℃
Supply current	2.0 mA (max)
Supply voltage	0 to 40 V
Threshold input current	10 uA (max)
Isolation voltage	0



IN	OUT
0	0
1	1

Figure 1. 5. Internal Structure of IXDN 614

An additional PCB board had designed with combination of this gate drivers it has isolated DC/DC converter for supplying gate drivers, gate resistances and decoupling capacitors, also it has double circuit, in figures shown schematic and PCB drawings are given

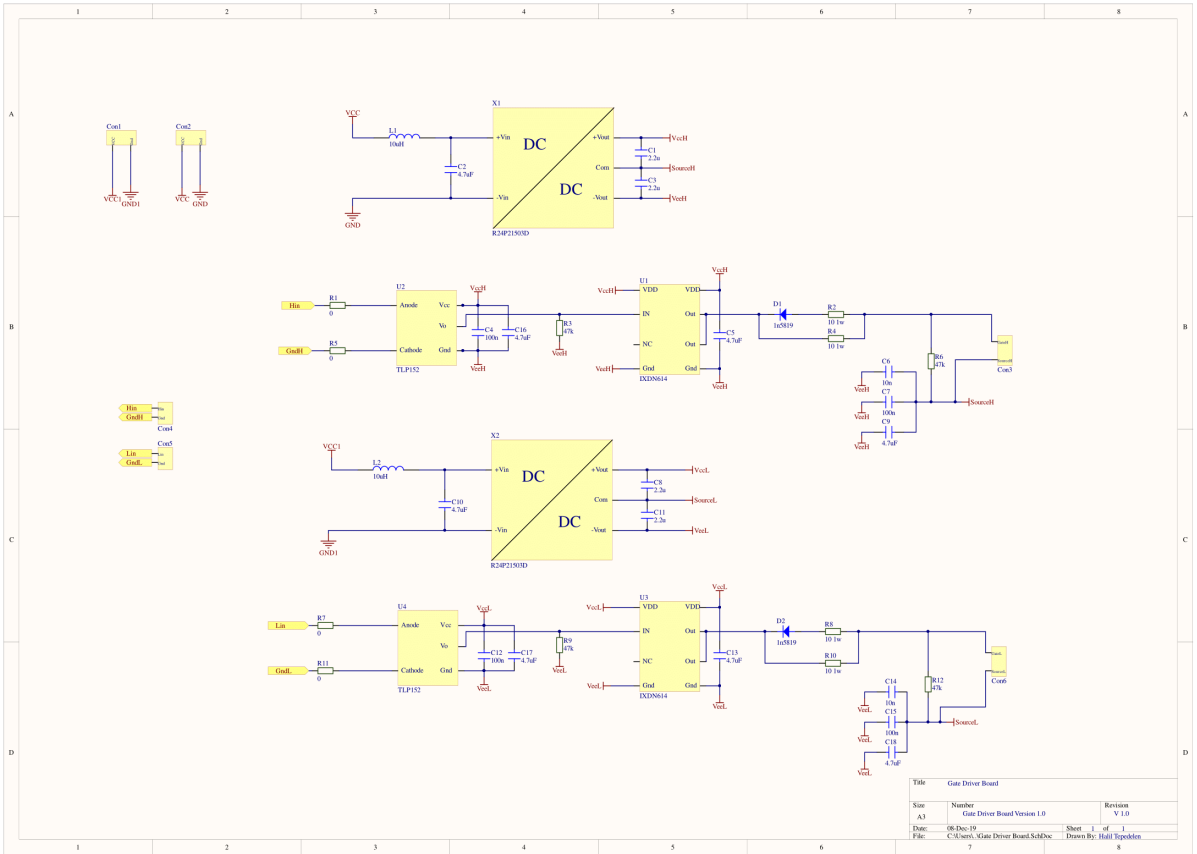


Figure 1. 6. Schematic of Gate Driver Board

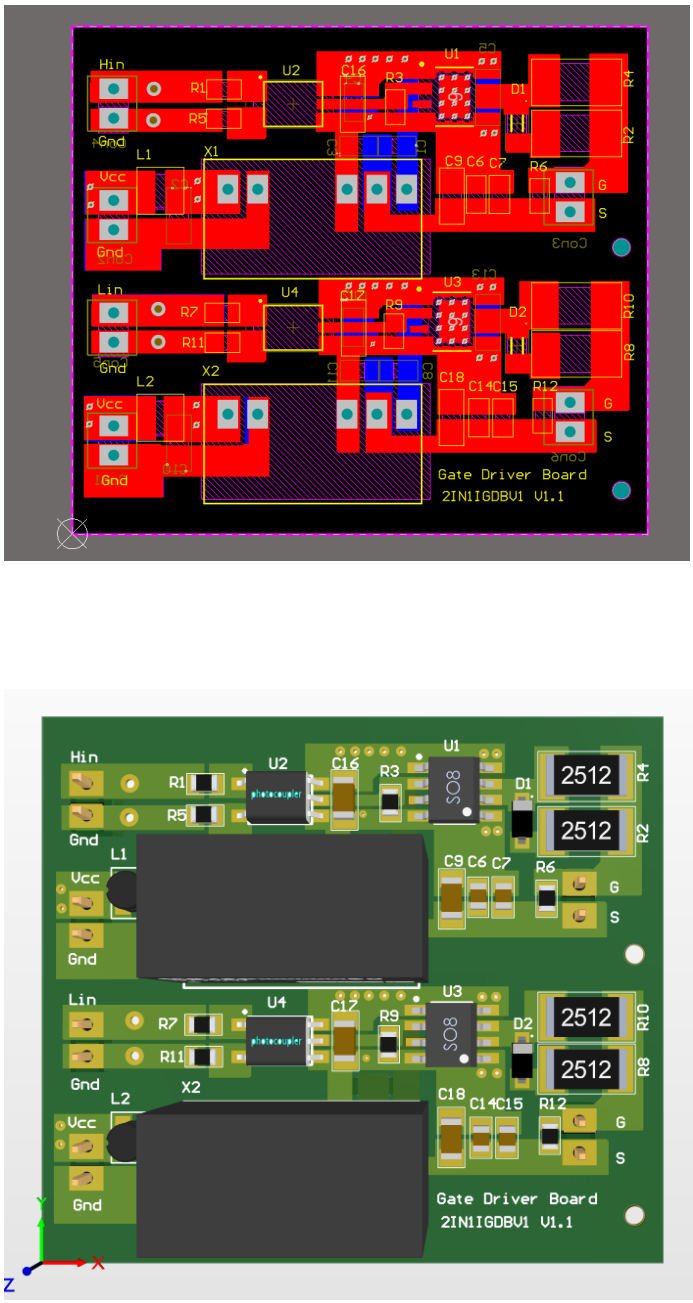


Figure 1. 7.Gate Driver Board PCB and 3D View

For supplying each gate driver we choose rkz-122005d part number DC/DC converter from recom brand it has 2W of continious power and 3kV isolation voltage also we made isolated DC/DC converter back up, figures are presence schematic and 3D view of our circuit.

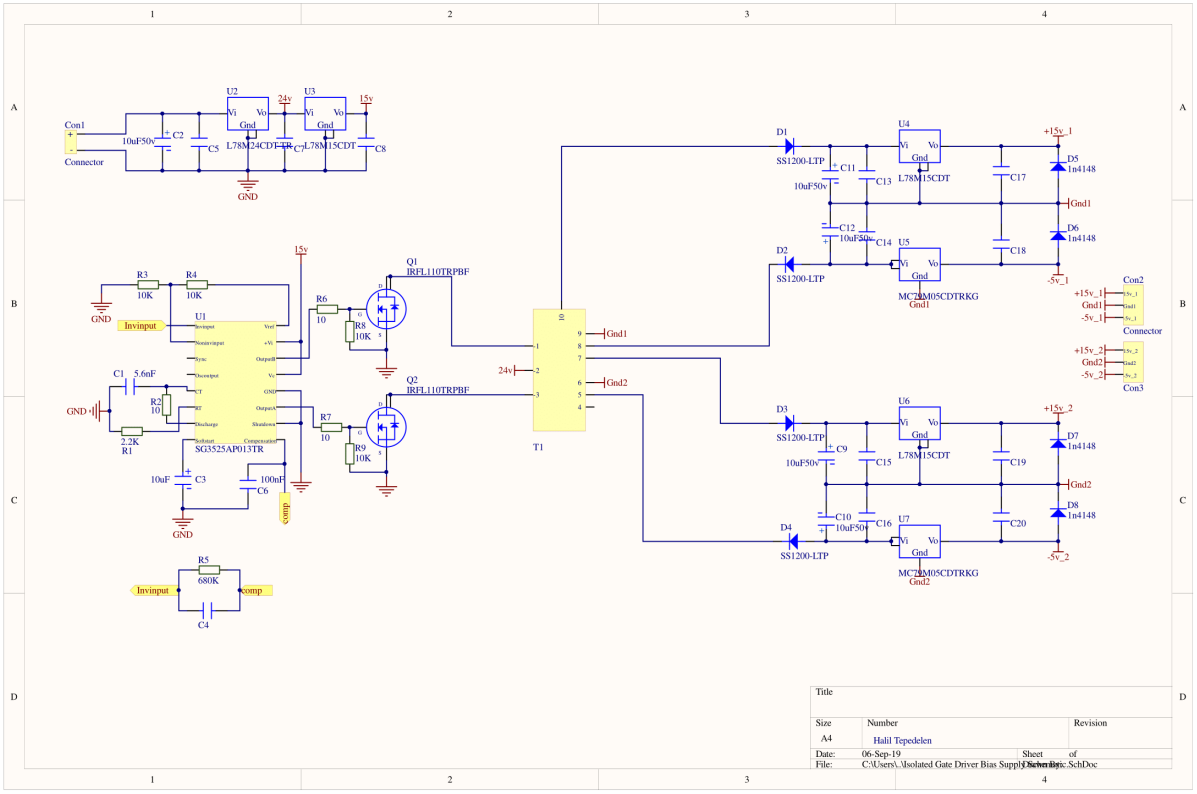
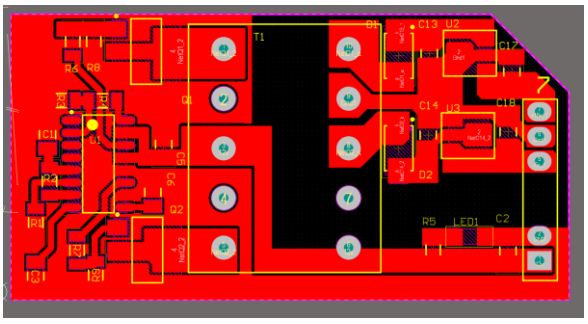


Figure 1. 8. Schematic Of DC/DC Converter



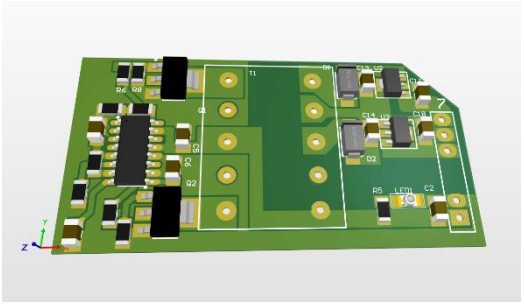


Figure 1. 9. PCB Drawings and 3D View of Circuit

Theoretical Loss Calculation

The primary source of lost efficiency in any inverter is going to be a result of the losses incurred in the switching devices. These losses are broken into three categories for each device:

• Conduction loss: When the device is on and conducting normally

• Switching loss: When the device is switching between states

• Diode conduction loss: Related to voltage drop and current when in conduction Each of these are dictated by their own equation, and can be determined from the device data sheet and design parameters that have already been set. Conduction loss is driven by the on-time of the FET, the switched current, and the on-resistance:

$$P_{cond\_lost} = \frac{1}{T}\int_0^T V_{ce}(t) \times I_c(t) \times D_D(t)dt$$

$$P_{cond\_lost} = \frac{1}{T}\int_0^T 3.12 \times 39 \times 0.9dt$$

where

• Vce is the conduction voltage drop

• Ic is the conduction current

• DD is the duty cycle

• T represents one modulation cycle

Switching loss is determined by the switching energy of the device and the switching voltage at a selected test point. Determine the value of the switching energy from the device data sheet using the value of the designed external gate resistor. The remainder of the values needed were determined earlier in the design phase.

$$P_{sw\_loss} = \frac{(E_{on} + E_{off}) \times I_{peak} \times f_{sw} \times V_{DC}}{\pi \times I_{avg} \times V_{nom}}$$

$$P_{sw\_loss} = \frac{(280\mu j + 80\mu j) \times 39 \times 30kHz \times 350}{\pi \times 39 \times 1000} = 1.203W\ Per\ Switch$$

Figure shows an example of the graph used to extract the switching energy values from the device data sheet is shown for an LSIC1MO120E0080 SiC MOSFET. Even at this stage, it is easy to see how the higher electron mobility in SiC results in reduced switch loss.

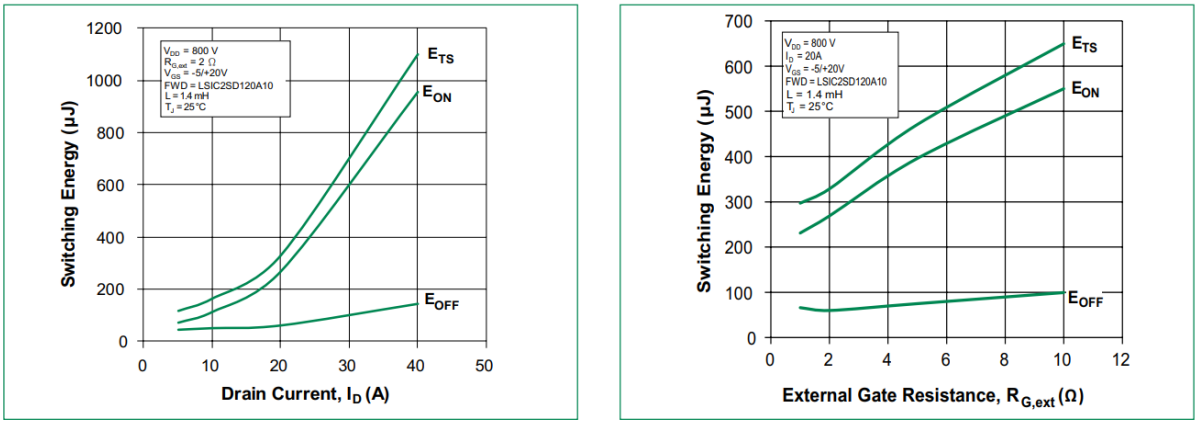


Figure 1.10.Switching Energy vs Gate Resistance and Drain Current for LSIC1MO120E0080

The diode conduction loss is similarly calculated using known values:

$$P_{sw\_diode} = \frac{1}{T}\int_0^T V_f(t) \times I_f(t) \times D_d(t)dt$$

where

• Vf is the voltage drop

• If is the diode current

• DD is the duty cycle

• T represents one modulation cycle

Inductor losses can be calculate with this equation;

$$P_{ind\_loss} = I^2_{ind\_ac\_rms} \times R_{DC} \times I^2_{ind\_ripple\_rms} \times R_{AC}$$

$$P_{ind\_loss} = 1 \times 0.0107 + 31.9^2 \times 0.033 = 11.1W$$

Total İnverter Losses can be calculate with this equation;

$$P_{total\_loss} = 6 \times P_{total\_sic\_mosfet\_loss} + 3 \times P_{ind\_loss}$$

This Equation can be in calculating therotical inverter efficiency

Conduction Loss	4.095×6= 24.57W
Switching Loss	1.203W×6= 7.21W
Diode Loss	2.1W×6= 12.6W
Inductor Loss	11.1W×3= 33.3W
TOTAL LOSS	77.68W

$$Efficiency_{inverter} = \frac{P_{Out}}{P_{Out} + P_{loss\_total}}$$

$$Efficiency_{inverter} = \frac{20kW}{20kW + 77.68W} = \%99.6$$

Power Board Design Criteria

When designig a printed circuit board there is many criteria to follow

- If board will carry high currents tracks has to be thick enough to carry this current
- Component placement should be properly choose for eliminate parasitic inductance
- If circiut board contains both power and signal circuit 4 or more layer will be good choise
- If there is no chance to make multilayer board seperated boards can be made for each purpose
- Termal management should be consider before design and proper heatsinks should be place
- For driving FETs gate drivers should place close enough to Gates so this will prevent gate ringing on FETs
- If there is snubber snubber network on circuit, snubber networks component properly placed in board to prevent voltage spakes, this will eliminate overshoot
- Each components has to have proper footprints
- Gate resistors should be well calculated and it has to be in good quality Melf package can be consider
- Bleeding resistors sholud be placed parallel with high voltage capacitors
- There has to be proper isolation between high voltage and low voltage areas
- There should be some test points for prototype boards