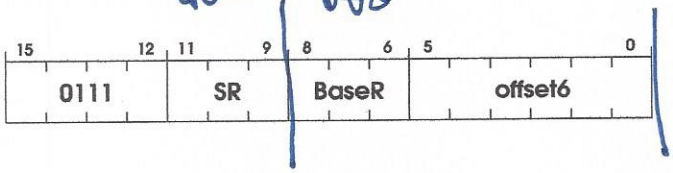
STW Store Word

Assembler Format

STW SR, BaseR, offset6

Encoding



Operation

MEM[BaseR + LSHF(SEXT(offset6), 1)] = SR;

Description

The contents of SR are stored into the word-aligned memory location whose address is obtained by sign-extending offset6 to 16 bits, left-shifting the result by one bit and adding this to the contents of the base register.

Example

STW R4, R2, #10 ; MEM[R2 + 20] ← R4

Note

The base register must contain a word address (i.e., its contents must be even). If the base register contains an odd address, an illegal operand address exception occurs.

BaseR → ARF] 2?

~~R RF~~

$I_{\wedge}$ MAR

$I_{\wedge}$ OFF MAR

R RF OFF

MAR Loaded

SR → ARF

R RF

I_{8-15} ON

I_{0-7} ON

I_{8-15} OFF

I_{0-7} OFF

R RF OFF

MDR Loaded

MDR $\overline{O_1}$ ON

MEM $\overline{W}$ ON

MEM $\overline{W}$ OFF

MDR $\overline{O_1}$ OFF

MDR $\overline{O_2}$ ON

MDR 3S ON

MDR 3S ~~ENABLE~~ High

MEM $\overline{W}$ ON

← {increment MAR

MEM $\overline{W}$ OFF

MDR $\overline{O_2}$ OFF

MDR 3S OFF

STW

0111

STW R4, R2, #10 MEM[R2+20] ← R4

D, L, #

LOAD MAR

Write MDR

Out Reg to Bus

~~In MAR~~ RF

Base R → RF A_{0-2}

Output RF

In MAR

OFF MAR

OFF RF