imm5 + SR1 → DR

1. 3S Dir (L-down) (MDR)
2. 3S EN (MDR)
3. O8-15 (MDR)
4. O0-7 (MDR)
5. I8-15 (MDR)
6. I0-7 (MDR)
7. O (MEM) R
8. W (MEM) W
9. In (MAR)
10. ~~In (Clock)~~
11. ~~Out(Clock)~~
12. ~~En (MPlex)(Halt) (Clock)~~
13. A0 (RF)
14. A1 (RF)
    a. a0 (RF)
    b. a1 (RF)
    c. a2 (RF)
15. r (RF)
16. w (RF)
17. ~~r (RF)~~
18. s0 (ALU)
19. s1 (ALU)
20. s2 (ALU)
21. s3 (ALU)
22. oe (ALU)
23. r2ie (ALU)
24. ce (ALU)

A0, A1 = SR1 (10) Load Imm5 in SR

PC In
PC EN
PC OUT
CLK EN (HALT)

00 DR
01 SR1
10 SR2

I (Stack)
O BA

I/O

Imm 0-3

0.35 DiR (LV)

1. 3S EN (MDR)
2. O8-15 (MDR) $\overline{O_2}$
3. O0-7 (MDR) $\overline{O_1}$
4. I8-15 (MDR) W_1
5. I0-7 (MDR) W_0
6. O (MEM) $\overline{R}$
7. W (MEM) $\overline{W}$
8. In (MAR)
9. In (Clock) PC
10. Out(Clock)
11. En (MPlex)(Halt) (Clock)
12. a0 (RF)
13. a1 (RF)
14. a2 (RF) → 2 a_0 a_1
15. r (RF)
16. w (RF)
17. ~~M~~(RF) M (ALU)
18. s0 (ALU)
19. s1 (ALU)
20. s2 (ALU)
21. s3 (ALU)
22. oe (ALU)
23. r2ie (ALU)
24. ce (ALU)

25 IR R
26 IR W XL 28 <16 15> -

9720

MEM: 8
CIK: 3
Reg: 6
ALU: 7

Write Microcode
Choose Opcode to Do 1st

Memory:

MDR:
- 3S: EN
- 3S Dir (L↓)
- $\overline{O_{8-15}}$
- $\overline{O_{0-7}}$
- I_{8-15}
- $I_{0:7}$

Mem
- $\overline{O.}$
- $\overline{W.}$

MAR
- $\overline{In}$

Clock
- $\overline{In}$
- $\overline{Out}$
- $\overline{En}$ (Multiplex) (Halt)

8 Reg:
- a_0
- a_1
- a_2
- R
- W

ALU
- M
- S_0
- S_1
- S_2
- S_3
- $\overline{OE}$
- R_2IE
- CE