I1	I0	O1N	O0N	RN	WN	3DIR	3SN	
0	0	0	0	1	1	-	0	MDR TO BUS
0	0	0	1	1	0	1	1	R1 TO MEM
0	0	1	0	1	0	-	0	R0 TO MEM
0	0	1	1	1	1	-	0	DEFAULT (off)
0	1	0	0	1	1	-	0	
0	1	0	1	1	1	-	0	
0	1	1	0	1	1	-	0	
0	1	1	1	0	1	-	0	MEM TO R0
1	0	0	0	1	1	-	0	
1	0	0	1	1	1	-	0	
1	0	1	0	1	1	-	0	
1	0	1	1	0	1	0	1	MEM TO R1
1	1	0	0	1	1	-	0	
1	1	0	1	1	1	-	0	
1	1	1	0	1	1	-	0	
1	1	1	1	1	1	-	0	BUS TO MDR

```
0000    11-0
0001    1011
0010    10-0
0011    11-0
0100    11-0
0101    11-0
0110    11-0
0111    01-0
1000    11-0
1001    11-0
1010    11-0
1011    0101
1100    11-0
1101    11-0
1110    11-0
1111    11-0
```

Memory Space

2^{16} locations

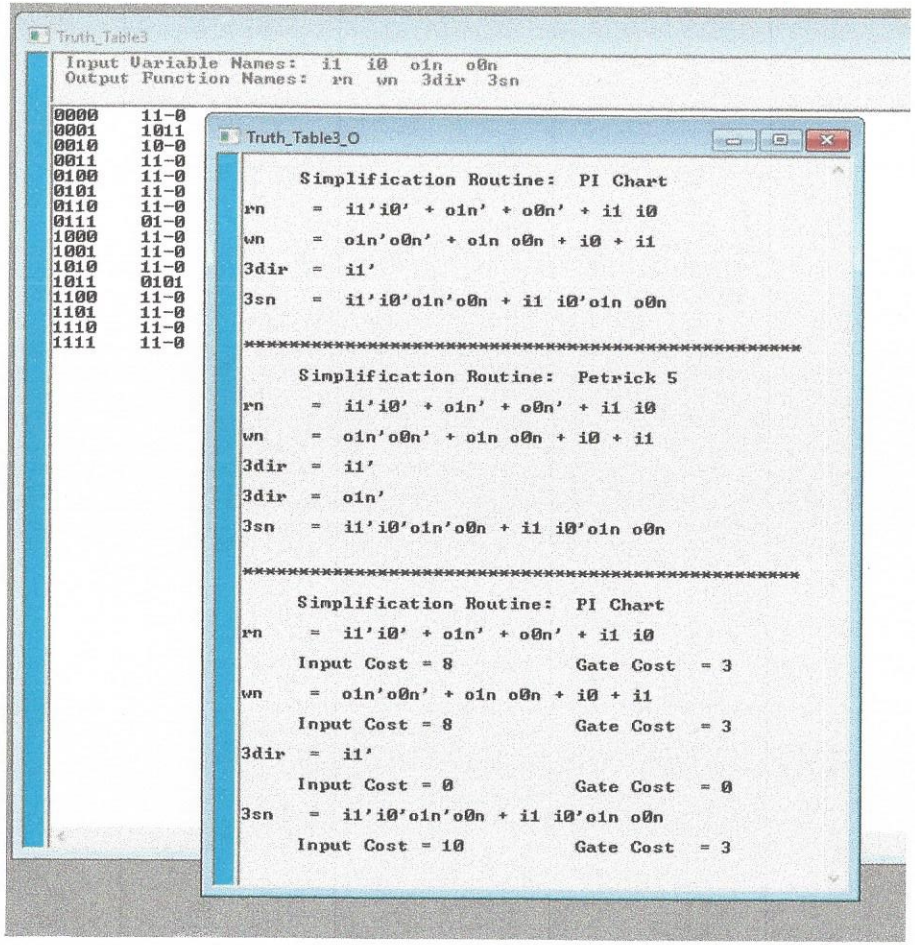
65,536

8 bits

520Kb Total

Word = 16 bits

1 2 4 8 16 32 64 128 256



2:1 OR

2:1 NAND

4:1 AND

LED

n0	n1	n2	n3	mar in	pc in	pc count	pc out	I8-15 (MdR)	I0-7 (MdR)	MDR R	3S dir	3S En	IR R	IR W			
1	0	1	0		0 1		1 1										write num to pc
				0 1			0 1										pc to mar
						1 0											increment pc
								0	1 0								write first byte
				0 1			0 1										pc to mar
						1 0											increment pc
								1 0	0		0	1 0					write second byte
										1		0	1 1	1 0			mdr to ir

Rd ~~wdg~~

~~Al~~ Always low?

3S En = byte2

MDR R0

W2 R2

R2=0 R2=1

W2=1. V2=0

~~Tie 3S DiR + MDR R1~~

3S EN = R1 OR W1

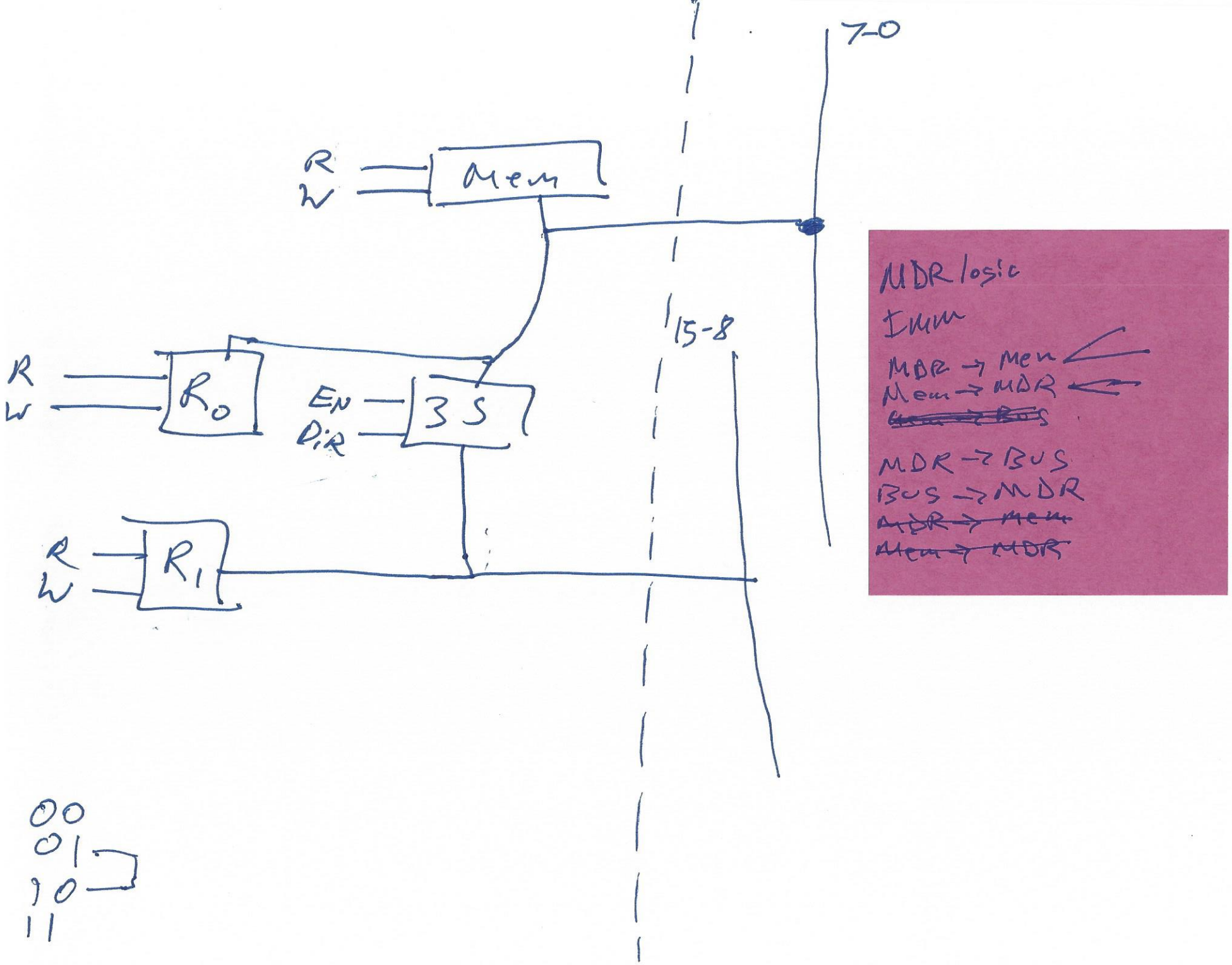
← Mar - -

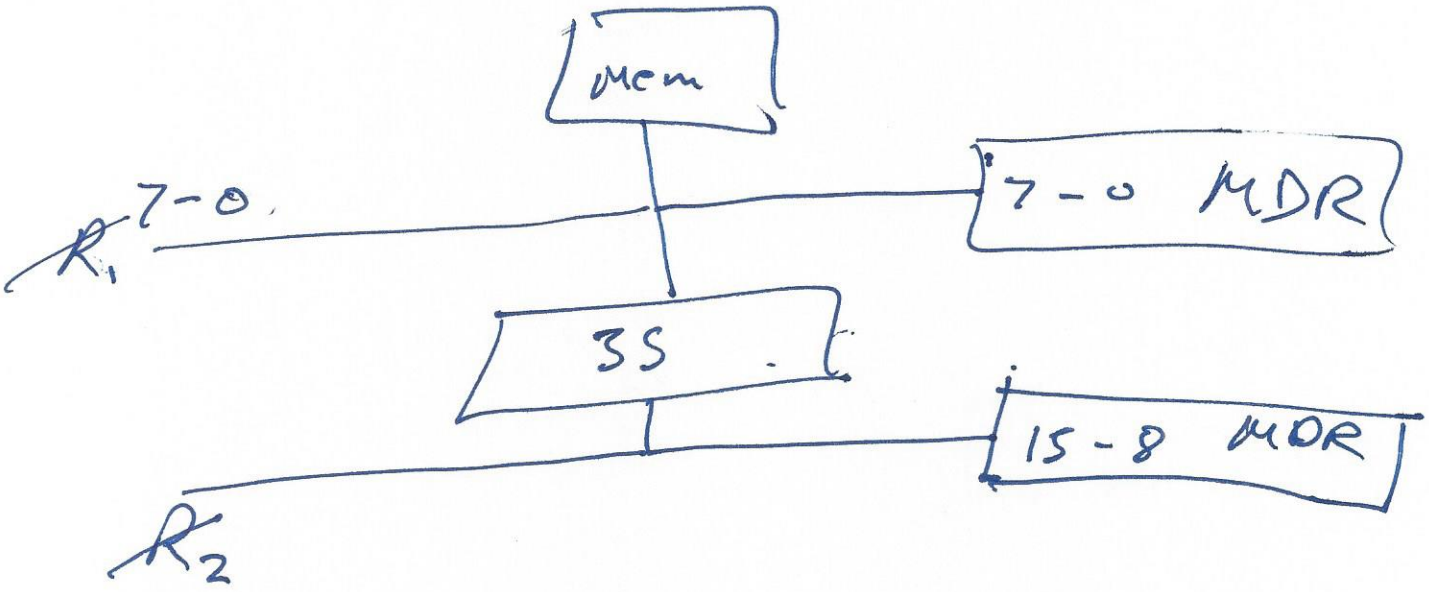
Connect MBR out Together

~~3S Dir = Always Same?~~

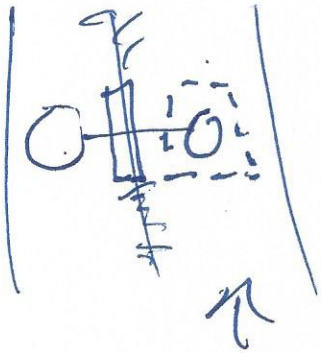
3S En ~~Tie to I8-15?~~

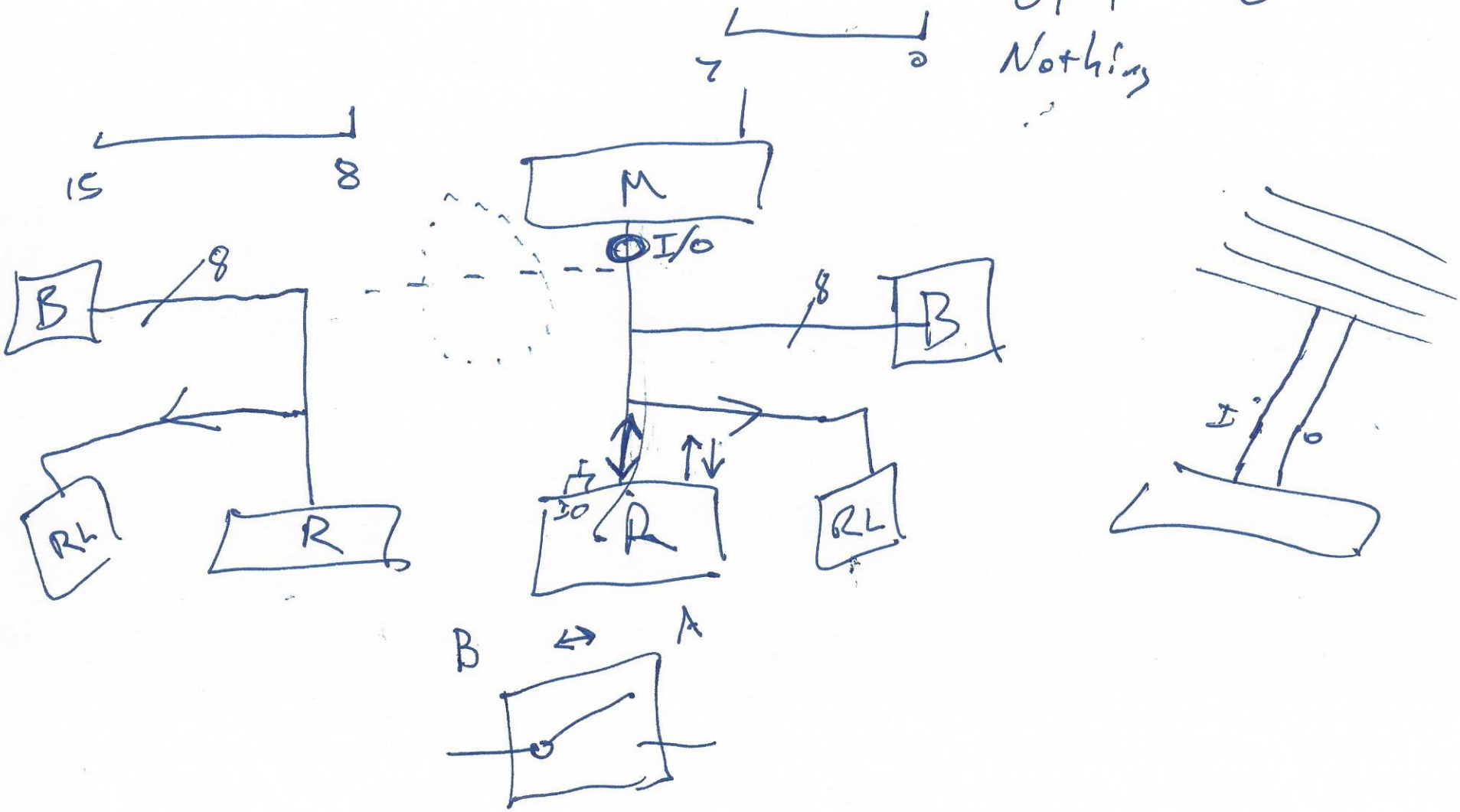
R1	W1	3S DiR
0	0	X
0	1	0
1	0	1
1	1	X


7-0
R
W
Mem
15-8
R
W
R_0
EN
DiR
3S
R
W
R_1
MDR logic
Imm
MDR → Mem
Mem → MDR
MDR → BUS
BUS → MDR
00
01
10
11

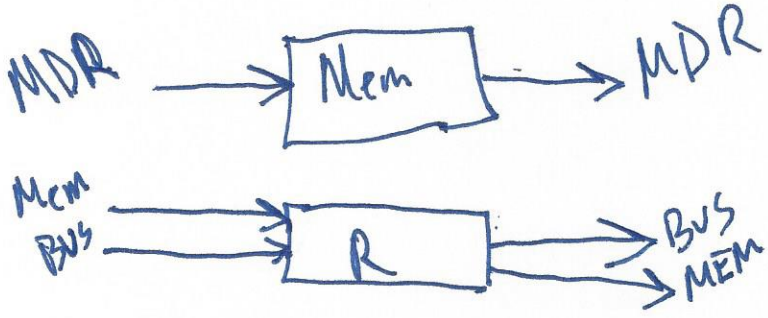


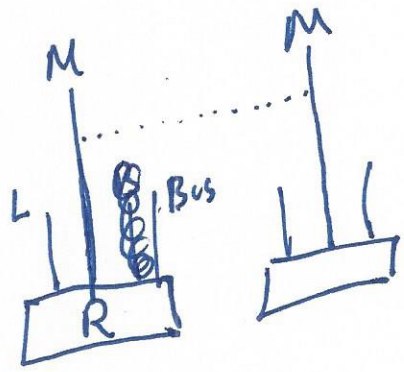
MDR → Mem

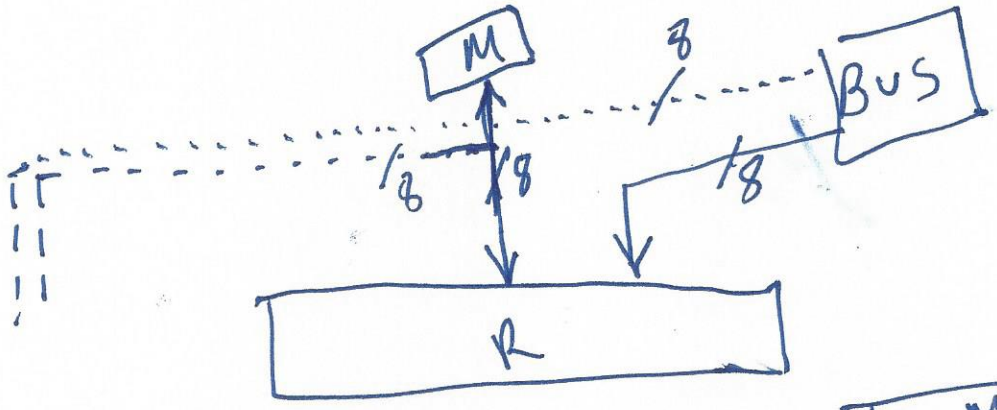


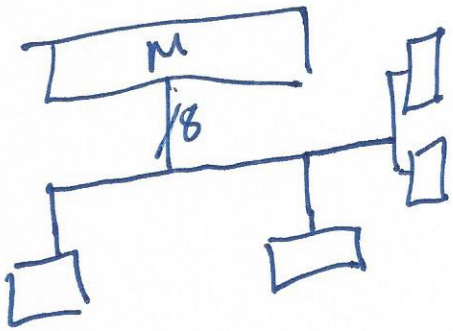


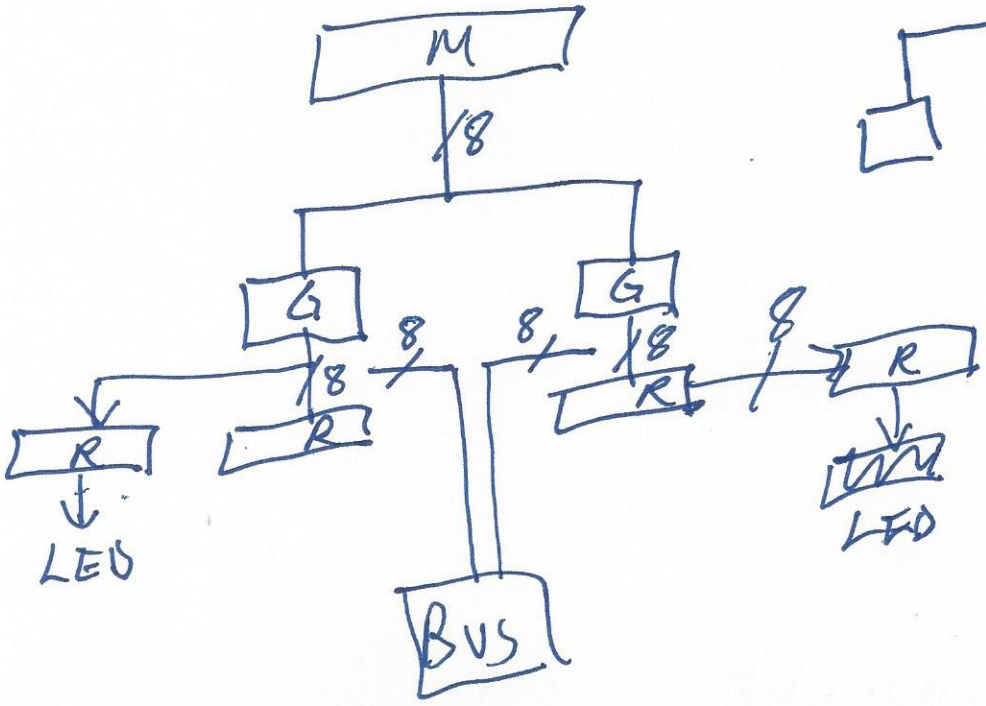
MEM $\overline{OE}$	MEM $\overline{WE}$	MDR I_1	MDR I_0	MDR $\overline{O_2}$	MDR $\overline{O_1}$	3S DIR	3S EN
						LH	


MDR
Mem
MDR
Mem
BUS
R
BUS
MEM

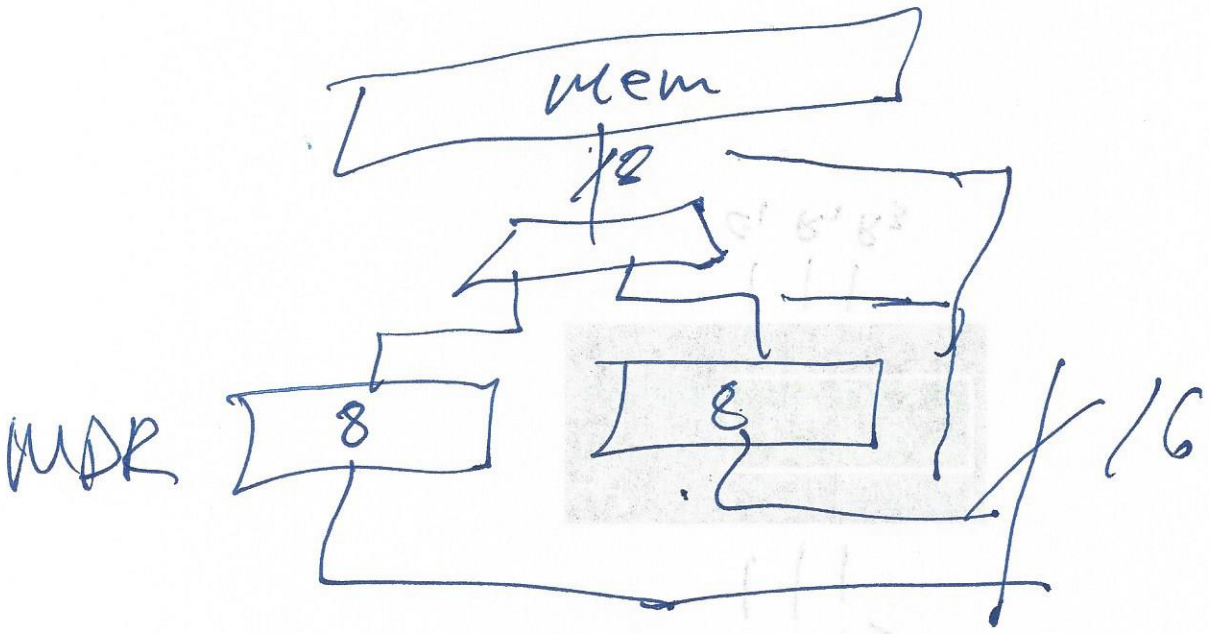

M
M
L
BUS
R

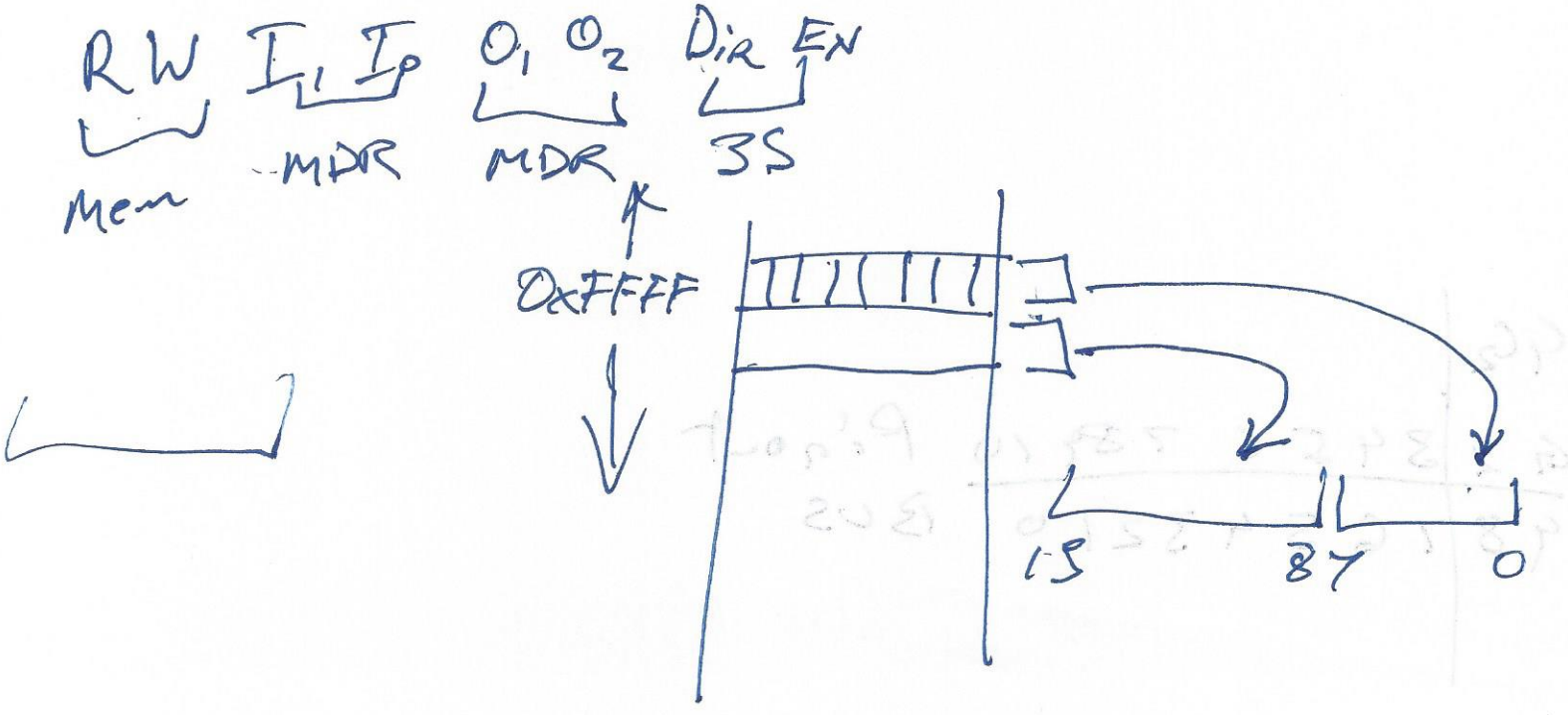

M
8
BUS
8
8
8
R

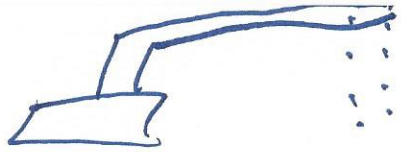

M
8

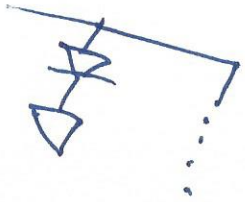

M
8
G
G
8
8
8
8
8
R
R
R
R
LED
LED
BUS

Mem: I/O = 1 pin

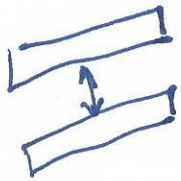








Microinstruction counter

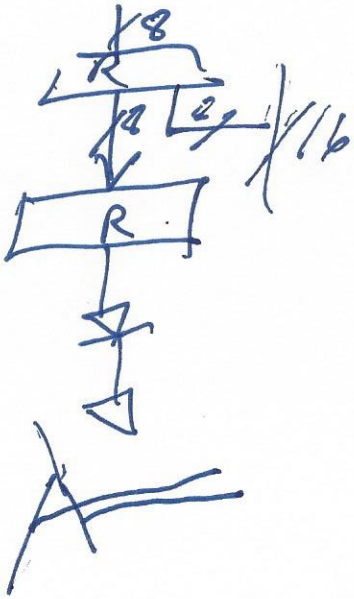


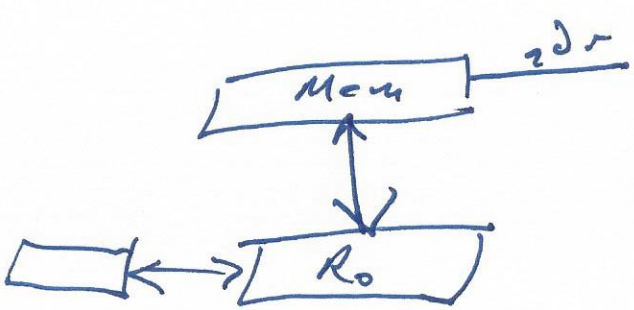
Decoder

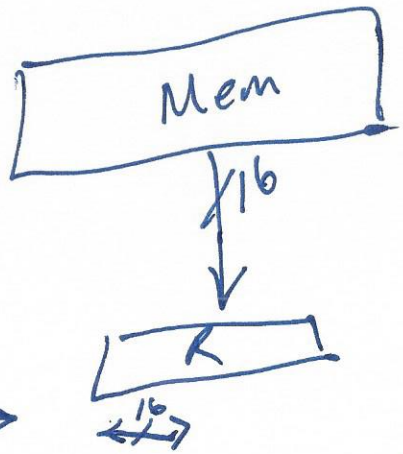
IR

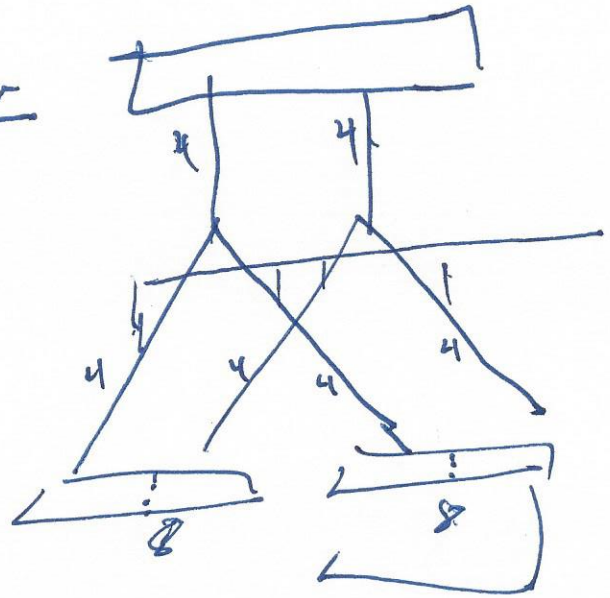
- Gym
- Comp
- Moving
- SD
- 460

Mem









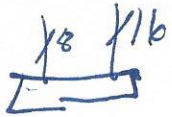
R I BUS MEM

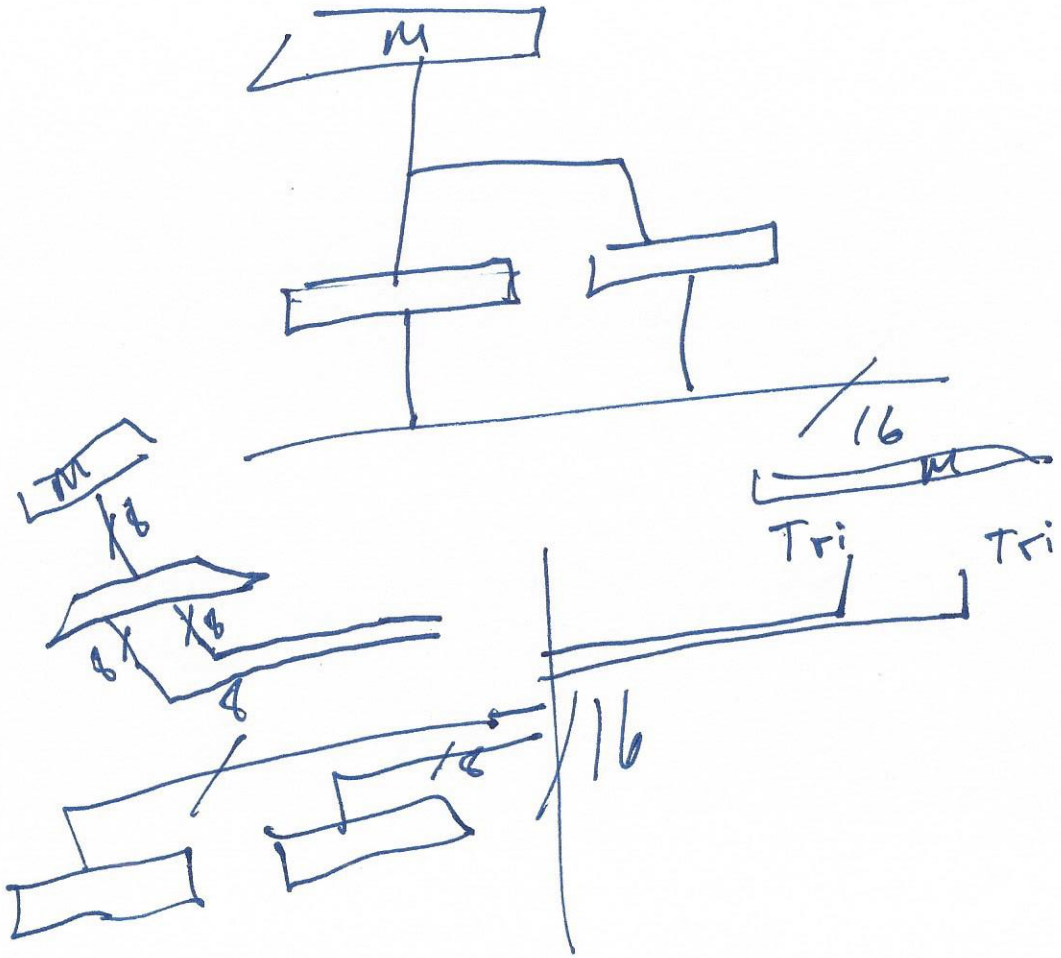
R O BUS MEM R2 RLED

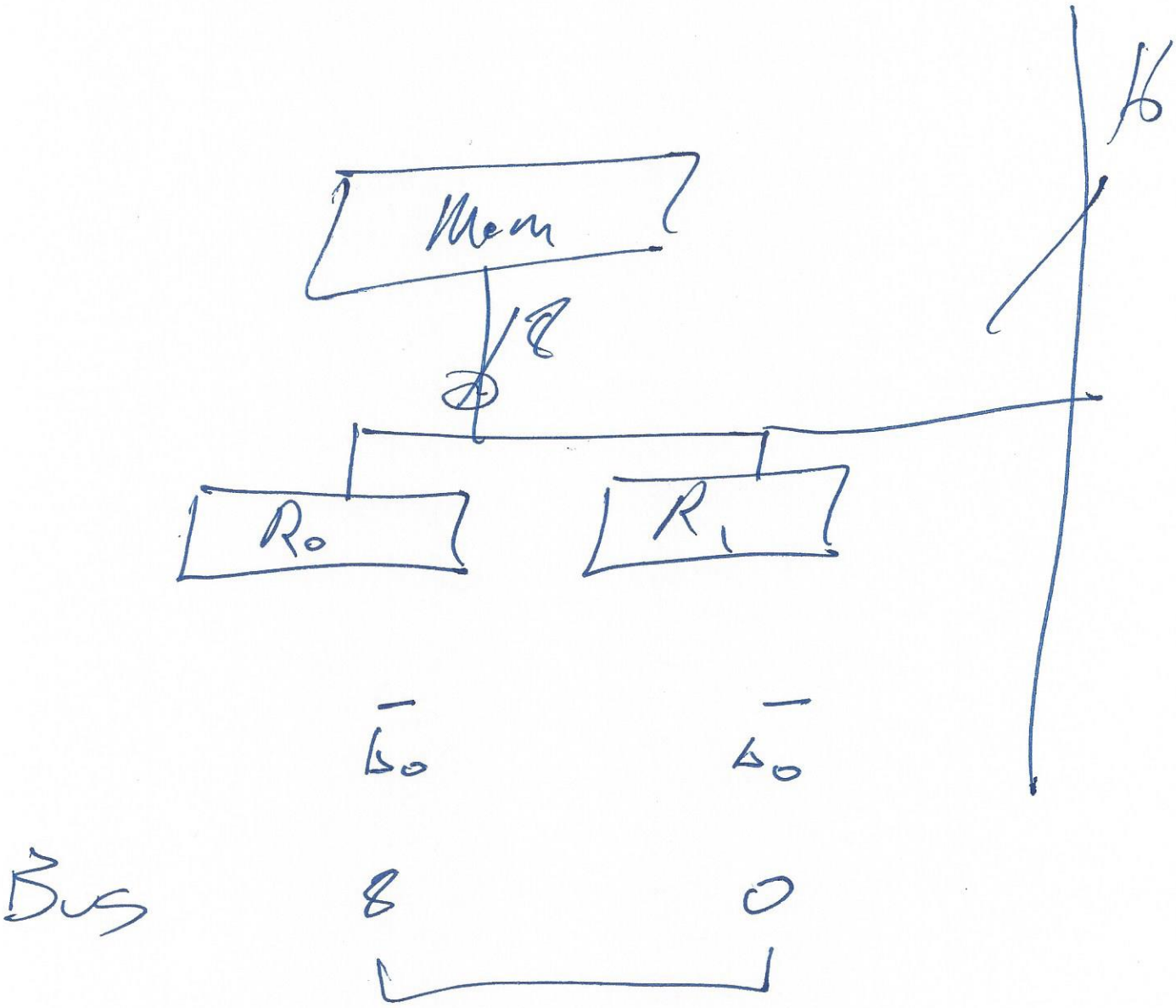
Mem ↔ R ↔ BUS

R

LED




M
16
M
8
8
8
8
Tri
Tri
16
16


Mem
R0
R1
Bus
8
0