Quad NANDs?

Time
Register
ALU
RAM

10 1x 74LS00 (Quad NAND gate)
~~8x 74LS02 (Quad 2-input NOR gate)~~
6 7x 74LS04 (Hex inverter)
~~7x 74LS08 (Quad 2-input AND gate)~~
~~2x 74LS11 (Triple 3-input AND gate)~~
~~3x 74LS32 (Quad two-input OR gate)~~
1x 74LS74 (Dual D flip-flop)
5x 74LS76 (Dual master-slave JK flip-flops)
~~2x 74LS86 (Quad XOR gate)~~
1x 74LS137 3:8 decoder
1x 74LS139 (Dual 2-line to 4-line decoder)
4x 74LS157 (Quad 2-to-1 line data selector)
1x 74LS161 (4-bit synchronous binary counter)
10 9x 74LS173 (4-bit D-type register)
~~2x 74LS189 (64-bit random access memory)~~
4 7x 74LS245 (Octal bus transceiver)
1x 74LS273 (Octal D flip-flop with clear)
2x 74LS283 (4-bit binary full adder)

2x 74HC595 8 bit shift reg
1x Common Anode 7-segment display
2 (10) 3x 28C16 EEPROM (should also work for 28C64 or 28C256)
1x 555 timer IC
Red gel (e.g., https://www.amazon.com/dp/B004GE19E2)

2, 1, 0, 7, 6, 5, 4, 3

ee teen
0 2
1 1
2 0
7 3
6 4
5 5
4 6
3 7

~~[10] 74170 4x4 Reg OC~~
(1) 61512 64k x 8 SRAM
(10) 74670 4x4 3state

— 2? 4

1Hz

$R_A + 2R_B = 10M$

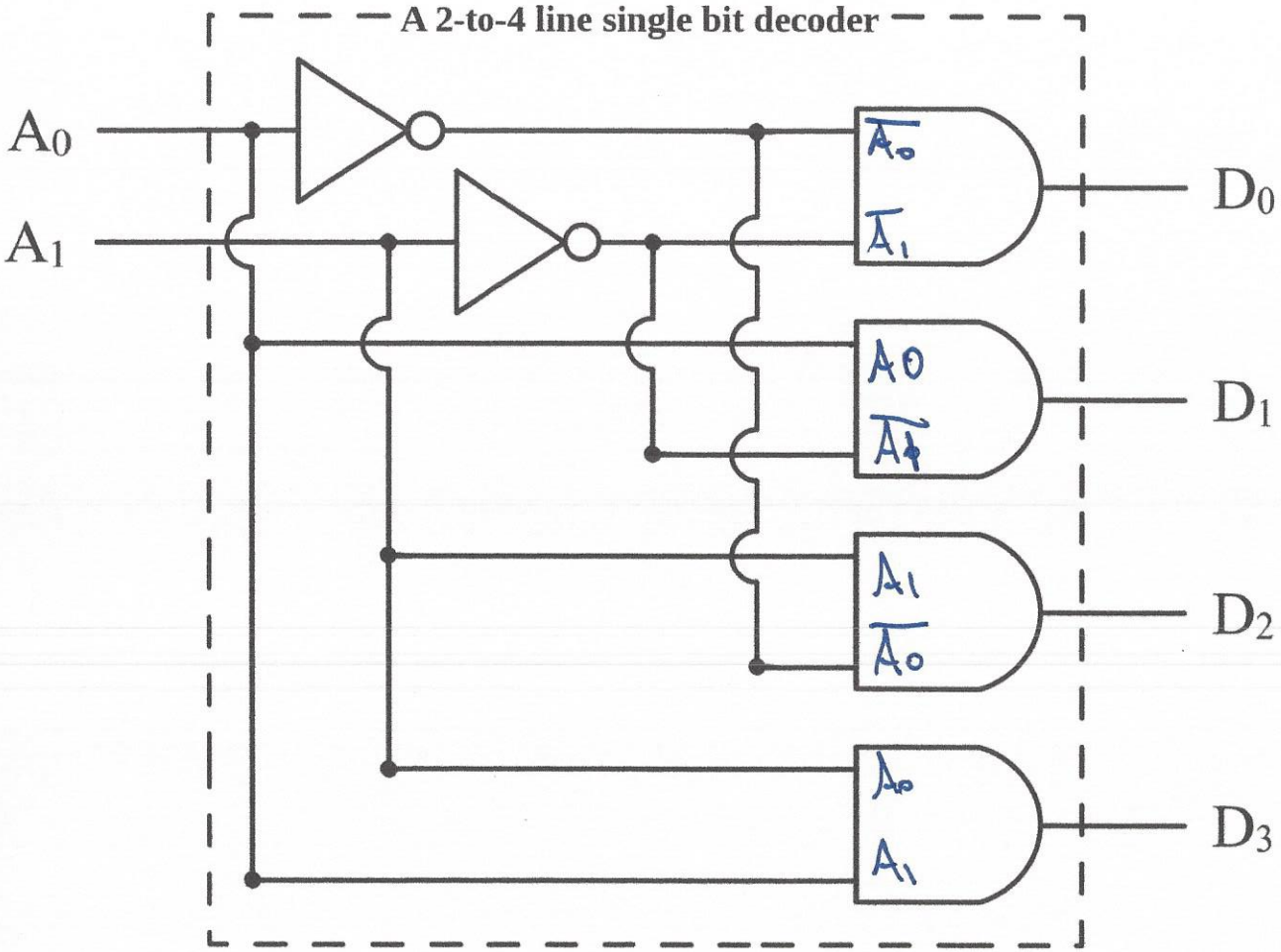
$0.1 < C < 1\ \mu F$

ALU Adder (283)
(Quad)

$R_A \times 2000 = 10M$

$10M = R_A + 2R_B$

$.5 = \frac{R_B}{R_A + 2R_B}$



Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

$$D_0 = \overline{A_1} \cdot \overline{A_0}$$

$$D_1 = \overline{A_1} \cdot A_0$$

$$D_2 = A_1 \cdot \overline{A_0}$$

$$D_3 = A_1 \cdot A_0$$

R B $\overline{A_0}\ \overline{A_1}$ A_0 Green

G B $A_0\ \overline{A_1}$ A_1 White

R W $\overline{A_0}\ A_1$ $\overline{A_0}$ Red

G W $A_0\ A_1$ $\overline{A_1}$ Black

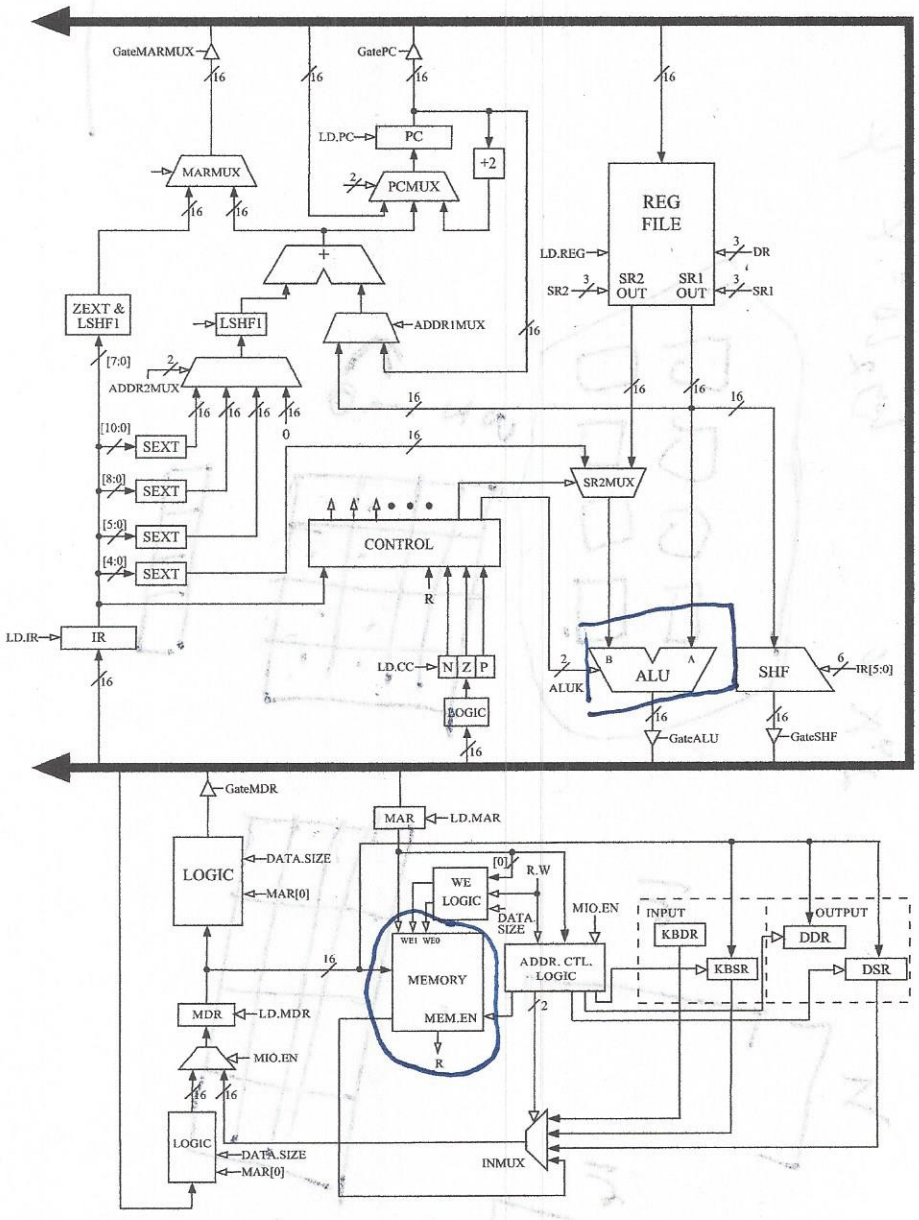


Figure C.3: The LC-3b data path

provide you with the additional flexibility of more states, so we have selected a control store consisting of 2^6 locations.