ADNS-4005

Low Power Optical Mouse Sensor

Data Sheet

Description

The Avago Technologies ADNS-4005 is a low power, small form factor optical mouse sensor. It has a new low-power architecture and automatic power management modes, making it ideal for battery, power-sensitive applications – such as cordless input devices.

The ADNS-4005 is capable of high-speed motion detection – up to 30 ips and 20 g. In addition, it has an on-chip oscillator and requires an external resistor to set the LED current.

The ADNS-4005 along with the ADNS-5110-001 lens, LED clip, and HLMP-CB3A form a complete and compact mouse tracking system. There are no moving parts and this translates to high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through a four-wire serial port. It is housed in an 8-pin staggered dual in-line package (DIP).

NOTE: The Avago Technologies' ADNS-4005 is a low power, small form factor optical mouse sensor that is licensed for blue LED mouse application. Using patented technologies, this mouse sensor tracks on virtually any surface.

Features

- Low Power Architecture
- Small Form Factor
- Programmable Periods / Response Times and Downshift Times from one mode to another for the Power-saving Modes
- High Speed Motion Detection up to 30 ips and 20 g
- External Interrupt Output for Motion Detection
- Internal Oscillator – no clock input needed
- Selectable Resolution of up to 2000 cpi
- Operating Voltage: as low as 1.7 V
- Four-wire Serial Port Interface

Applications

- Optical mice and optical trackballs
- Integrated input devices
- Battery-powered input devices

Theory of Operation

The ADNS-4005 is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

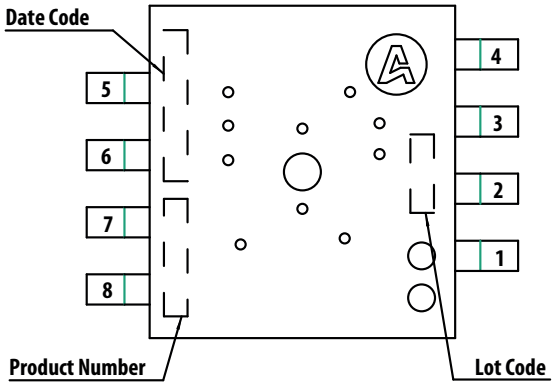
The ADNS-4005 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Dx and Dy relative displacement values

An external microcontroller reads and translates the Dx and Dy information from the sensor serial port into PS2, USB, or RF signals before sending them to the host PC.

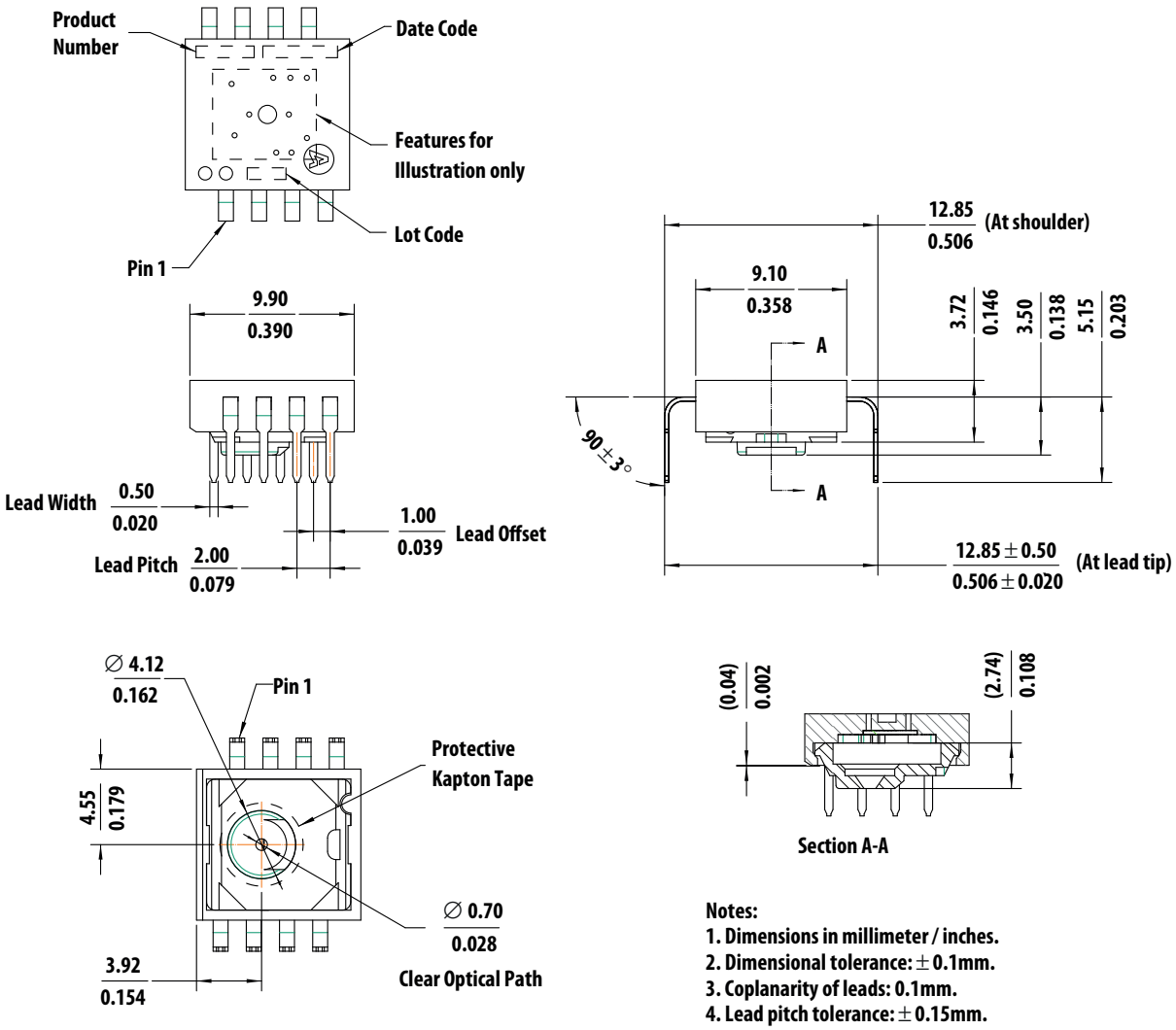
Pinout of ADNS-4005 Optical Mouse Sensor

Pin	Name	Input/ Output	Description
1	MISO	O	Serial Data Output (Master In/Slave Out)
2	LED	I	LED Illumination
3	MOTION	O	Motion Interrupt Output (Default active low, edge triggered)
4	NCS	I	Chip Select (Active low input)
5	SCLK	I	Serial Clock
6	GND	I	Ground
7	VDD	I	Supply Voltage
8	MOSI	I	Serial Data Input (Master Out/Slave In)



Item	Marking	Remarks
Product Number	A4005	
Date Code	XYYWWZ	X = Subcon Code YYWW = Date Code Z = Sensor Die Source
Lot Code	VVV	Numeric

Figure 1. Package Outline Drawing (Top View)



Notes:
1. Dimensions in millimeter / inches.
2. Dimensional tolerance: ±0.1mm.
3. Coplanarity of leads: 0.1mm.
4. Lead pitch tolerance: ±0.15mm.
5. Non-cumulative pitch tolerance: ±0.15mm.
6. Angular tolerance: ±3°
7. Maximum flash: 0.2mm.
8. Brackets () indicate reference dimension.
9. Document Number: LED_SPC_8C_PKG_002

Figure 2. Package Outline Drawing

CAUTION: It is advised that normal static precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

Overview of Optical Mouse Sensor Assembly

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment. The ADNS-4005 sensor is designed for mounting on a through-hole PCB, looking down. There is an aperture stop and features on the package that align to the lens. The ADNS-5110-001 lens provides optics for the imaging of the surface as well as the illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED. The LED clip holds the LED in relation to the lens. The LED must be inserted into the clip and the LED's leads formed prior to loading on the PCB. The HLMP-CB3A Blue LED is recommended for illumination.

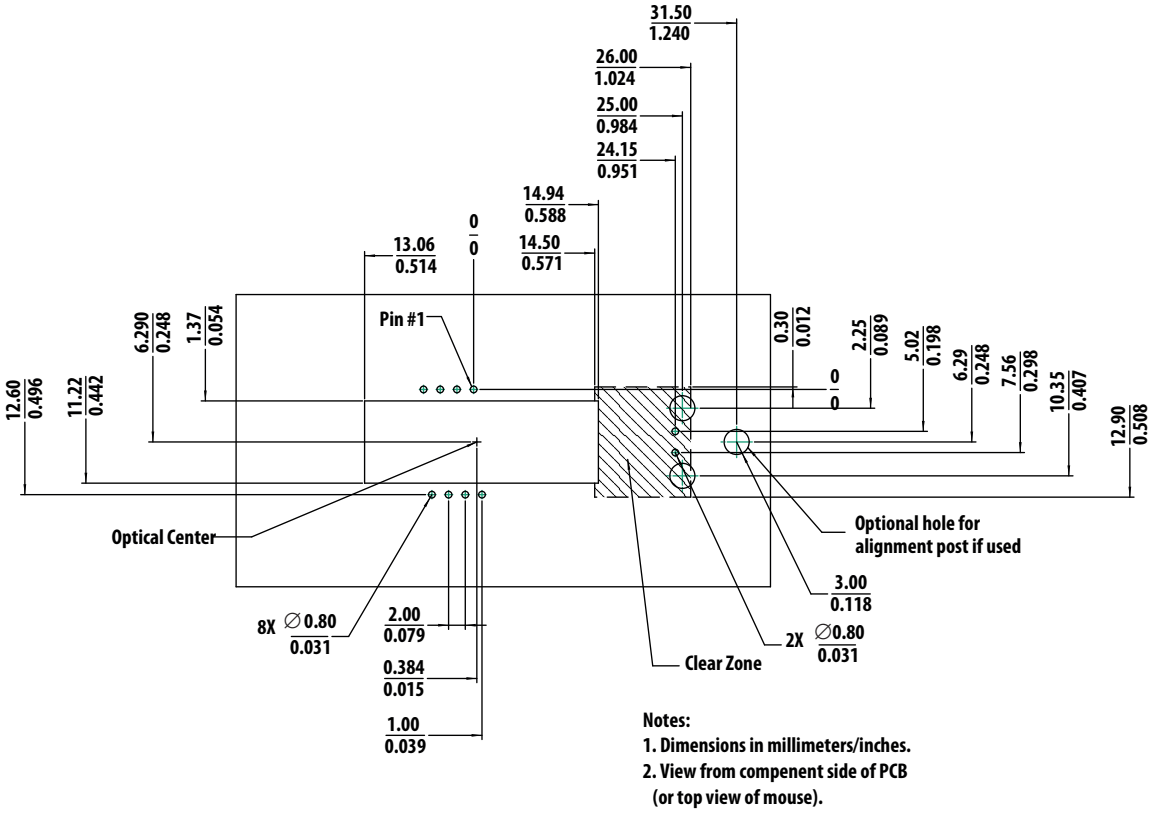
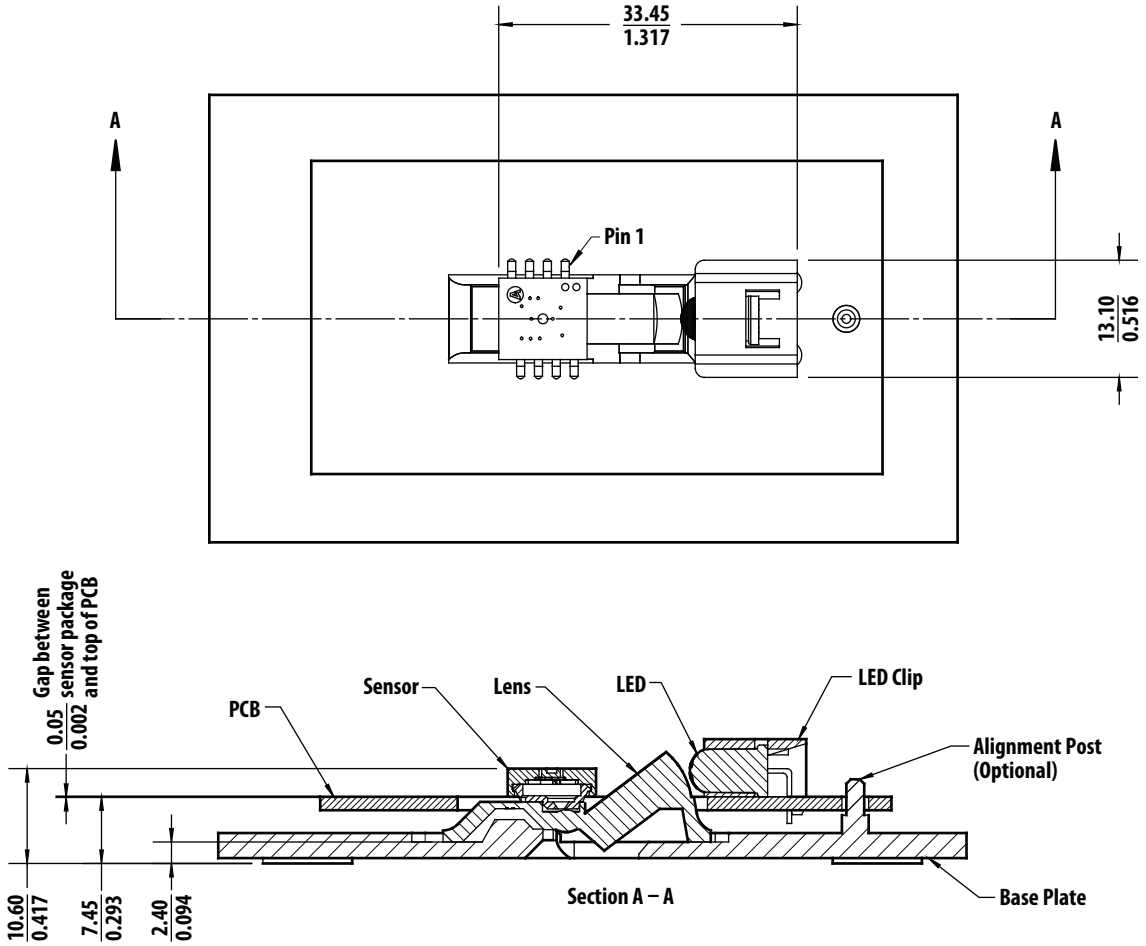
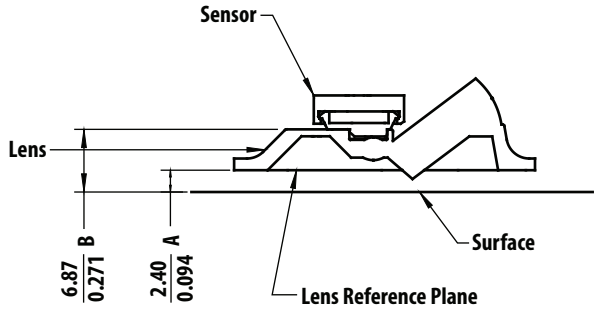


Figure 3. Recommended PCB Mechanical Cutouts and Spacing



Important Note: Pin 1 of sensor should be located nearest to the LED

Figure 4. 2D Assembly drawing of ADNS-4005 (Top and Side View)



Note:
A – Distance from object surface to lens reference plane
B – Distance from object surface to sensor reference plane

Figure 5. Distance from lens reference plane to tracking surface (Z)

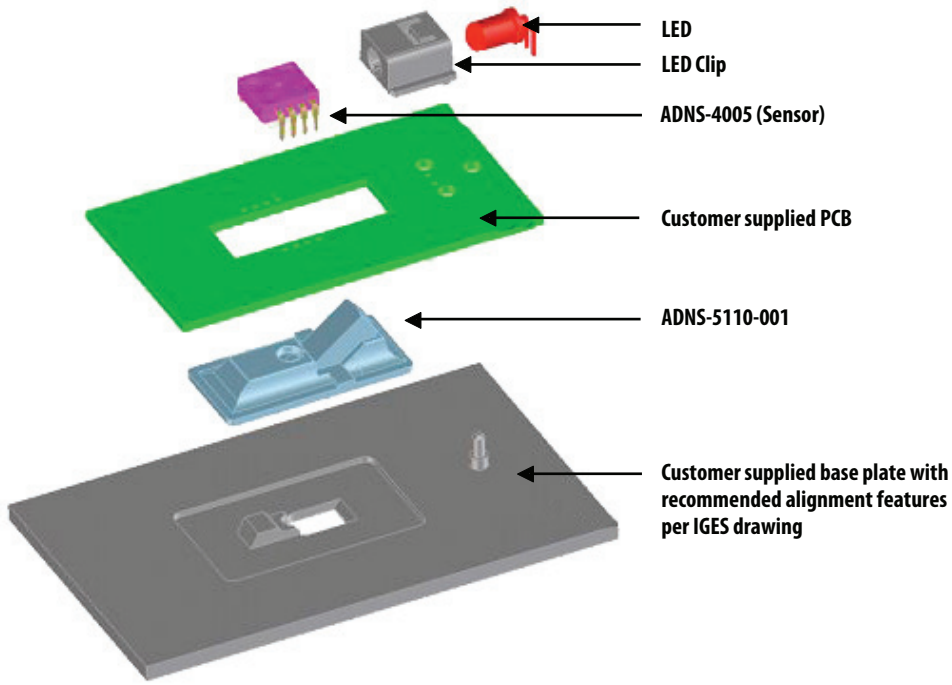


Figure 6. Exploded View of Assembly

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Insert the LED into the assembly clip and bend the leads 90 degrees.
3. Insert the LED clip assembly into PCB.
4. This sensor package is only qualified for wave-solder process.
5. Wave solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to-PCB distance as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
6. Place the lens onto the base plate.
7. Remove the protective Kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire mouse assembly process. Recommend to hold the PCB first vertically for the Kapton removal process.
8. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The sensor aperture ring should self-align to the lens.
9. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
10. Install mouse top case. There MUST be a feature in the top case to press down onto the PCB assembly to ensure all components are interlocked to the correct vertical height.

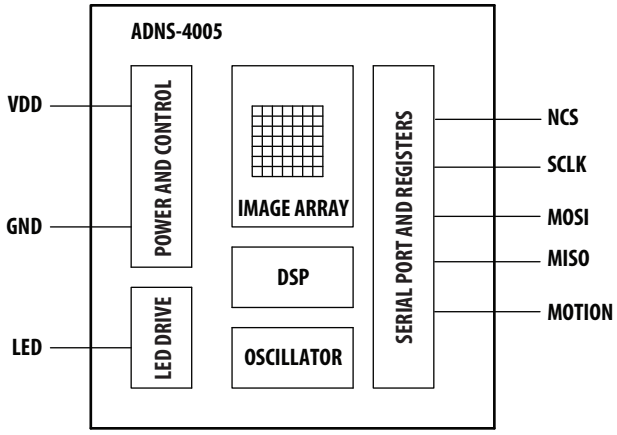


Figure 7. Block diagram of ADNS-4005 optical mouse

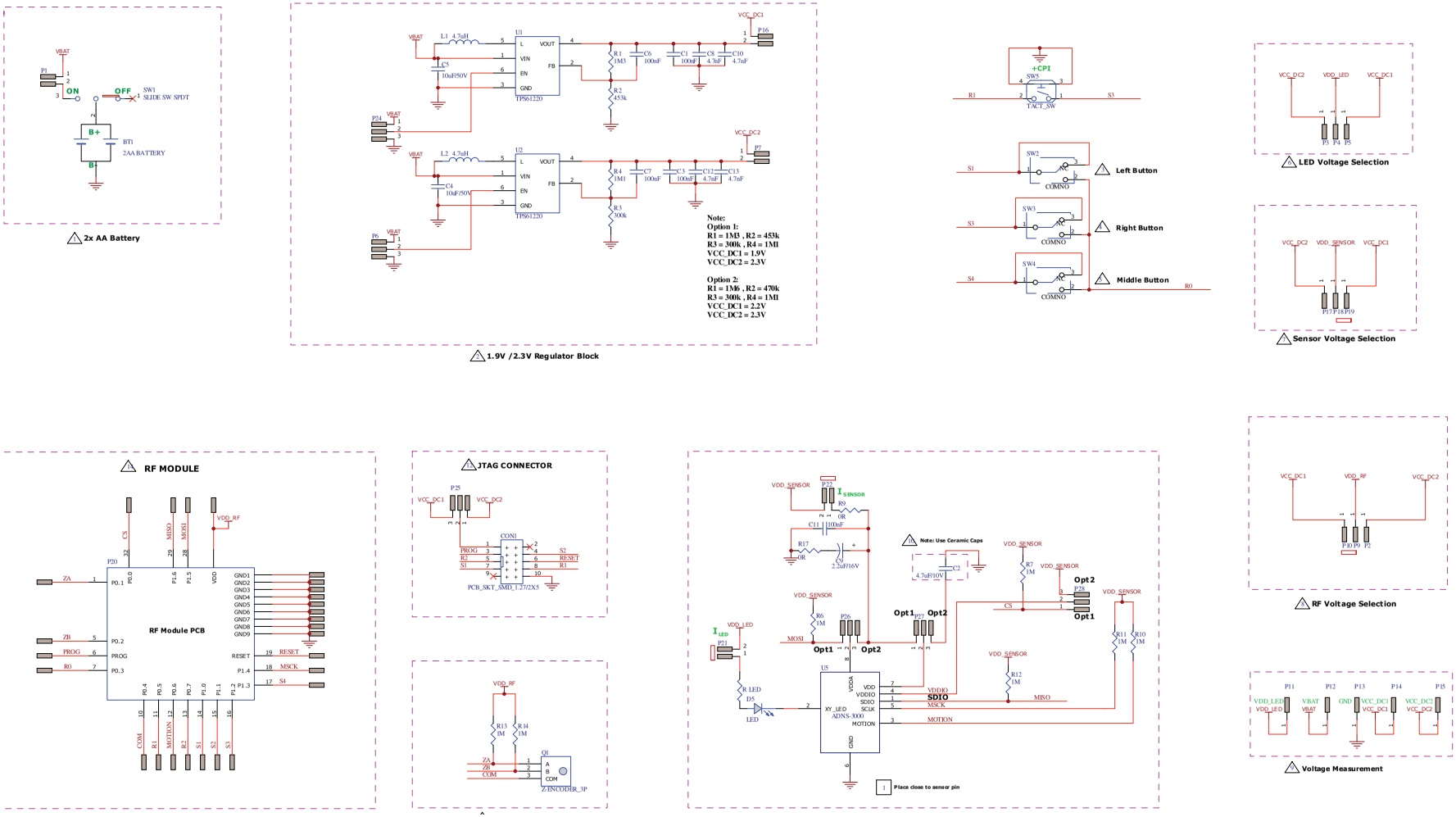


Figure 8a. Schematic diagram of the mouse (cordless application)

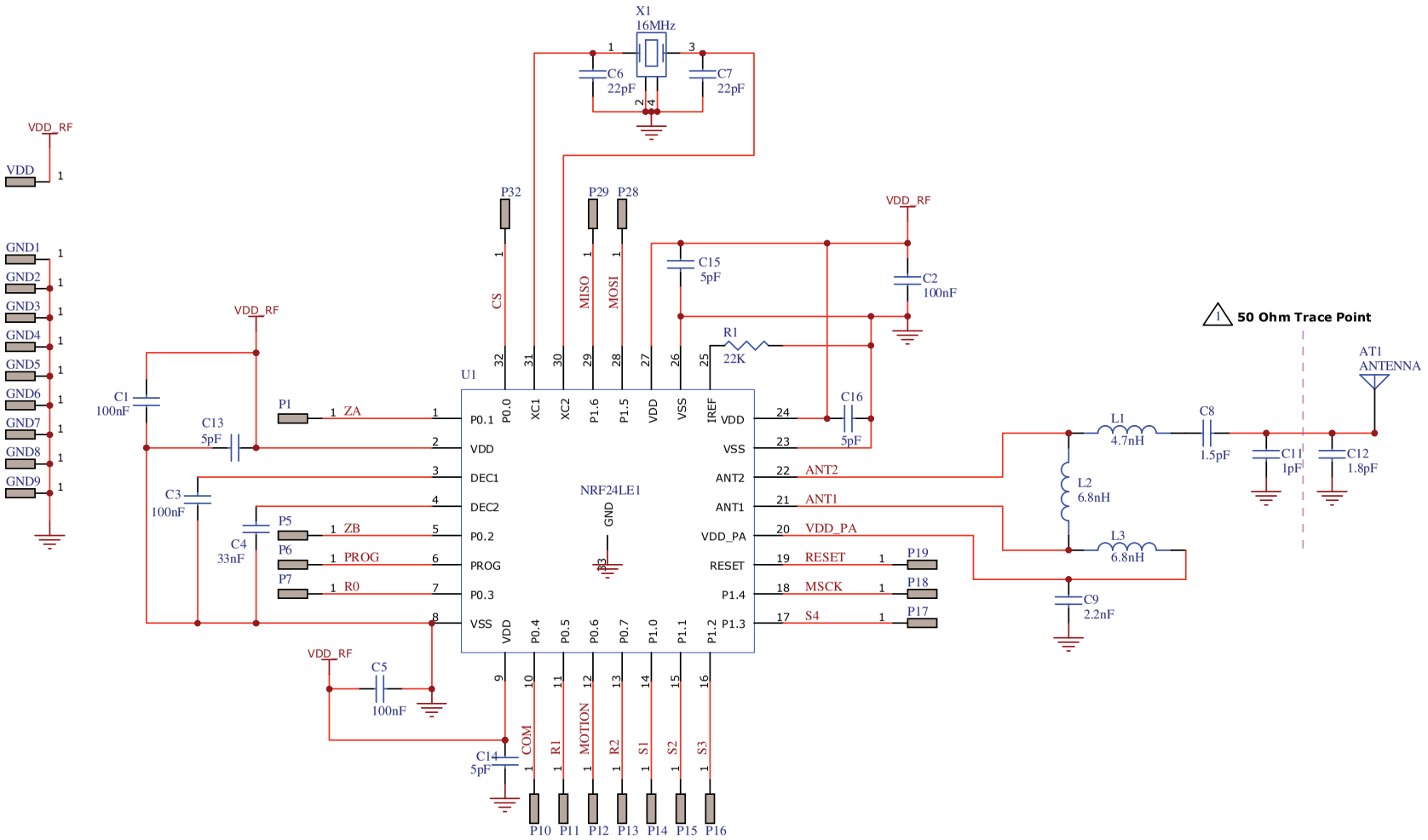


Figure 8b. Schematic diagram of the RF module on the mainboard

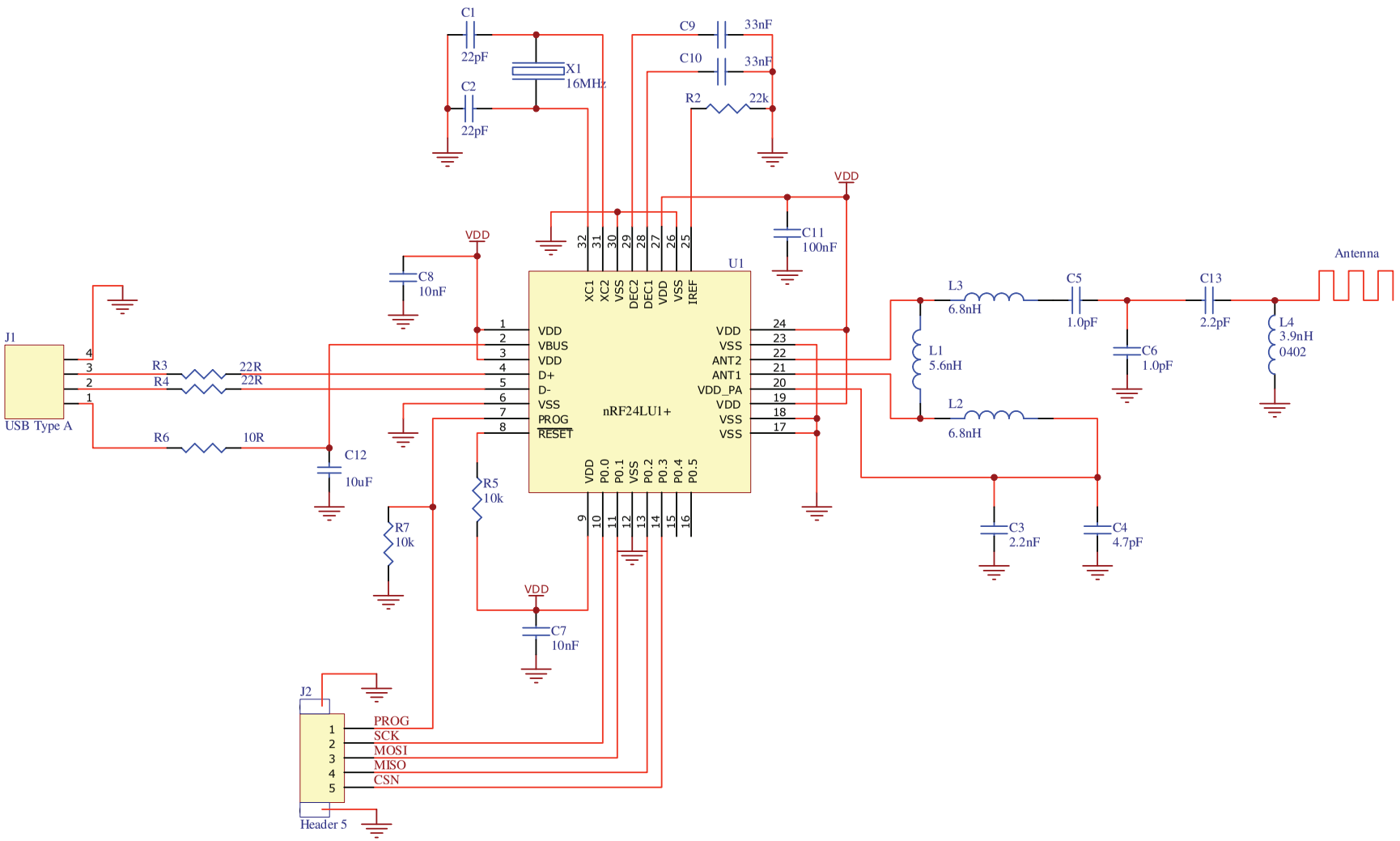


Figure 8C. Schematic diagram of the dongle

Design Considerations for Improved ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction is as per the Avago Technologies supplied IGES file and ADNS-5110-001 lens. Note that the lens material is polycarbonate or polystyrene HH30. Therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should **NOT** be used.

Typical	Distance (mm)
Creepage	16.0
Clearance	2.0

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 V-0.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Operating Temperature	T_A	-15	55	°C	
Lead Solder Temperature	V_O		260	°C	For 10 seconds, 1.6 mm below seating plane.
Supply Voltage	V_{DD}	-0.5	2.2	V	
ESD			2	kV	All pins, human body model JESD22-A114
Input Voltage	V_{IN}	-0.5	2.1	V	All I/O pins

Table 2. Recommended Operating Condition

Parameter	Symbol	Min	Typ.	Max	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	1.7	1.8	2.1	V	
Power Supply Rise Time	T_{RT}	0.15		20	ms	0 to V_{DD} min
Supply Noise (Sinusoidal)	V_{NA}			100	mVp-p	10 kHz –50 MHz
Serial Port Clock Frequency	f_{SCLK}			1	MHz	50% duty cycle
Distance from Lens Reference Plane to Tracking Surface (Z)	Z	2.3	2.4	2.5	mm	
Speed [1]	S	0		30	ips	At default frame rate
Acceleration	a			20	g	At run mode
Load Capacitance	C_{out}			100	pF	MISO and MOTION

Note:
1. For higher than 500 dpi setting, use 12-bit motion reporting to achieve the maximum speed

Table 3. AC Electrical Specifications

Electrical characteristics over recommended operating conditions. Typical values at 25° C, VDD = 1.9 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Motion Delay after Reset	$t_{MOT-RST}$			50	ms	From RESET register write to valid motion
Forced Rest Enable	$t_{REST-EN}$			1	s	From Rest Mode (RM) bits set to target rest mode
Wake from Forced Rest	$t_{REST-DIS}$			1	s	From Rest Mode (RM) bits cleared to valid motion
Power Down	t_{PD}			50	ms	From PD active (when bit 1 of register 0 x 0d is set) to low current
Wake from Power Down	t_{WAKEUP}			55	ms	Through RESET register 0 x 3a. From PD inactive to valid motion
MISO Rise Time	t_{r-MISO}		60	200	ns	C_L = 100 pF
MISO Fall Time	t_{f-MISO}		40	200	ns	C_L = 100 pF
MISO Delay after SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold-MISO}$	250		$1/f_{SCLK}$	ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time between Write Commands	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, Commands to rising SCLK for last bit of the second data byte
SPI Time between Write and Read Commands	t_{SWR}	20			µs	From rising SCLK f or last bit of the first data byte, to rising SCLK for last bit of the second address byte
SPI Time between Read and Subsequent Commands	t_{SRW} t_{SRR}	250			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the next address
SPI Read Address-Data Delay	t_{SRAD}	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read
NCS Inactive after Motion Burst	t_{BEXIT}	250			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK Active	$t_{NCS-SCLK}$	120			ns	From NCS falling edge to first SCLK falling edge
SCLK to NCS Inactive (For Write Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS Inactive (For Read Operation)	$t_{SCLK-NCS}$	20			µs	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
NCS to MISO high-Z	$t_{NCS-MISO}$			250	ns	From NCS rising edge to MISO high-Z state
Transient Supply Current	I_{DDT}			60	mA	Max supply current during a VDD ramp from 0 to VDD with min 150 µs and max 20 ms rise time. (Does not include charging currents for bypass capacitors.)

Table 4. DC Electrical Specifications

Electrical characteristics over recommended operating conditions. Typical values at 25° C, VDD = 1.9 V, VDD_{LED} = 3.6 V, HLMP-CB3A, R_{LED} = 47 Ω.

Parameter	Symbol	Min	Typ.	Max	Units	Notes
DC Supply Current in Various Mode	I_{DD_AVG}		1.44		mA	Average sensor current at max frame rate. No load on MISO
	I_{DD_REST1}		108		µA	
	I_{DD_REST2}		28		µA	
	I_{DD_REST3}		12		µA	
	I_{DDLED_AVG}		0.9		mA	
	I_{DDLED_REST1}		90		µA	
	I_{DDLED_REST2}		28		µA	
	I_{DDLED_REST3}		5.9		µA	
Power Down Current			10		µA	
Input Low Voltage	V_{IL}			0.3* V_{DD}	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7* V_{DD}			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		200		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{leak}		+/-1	+/-10	µA	Vin = VDD or 0 V
Output Low Voltage	V_{OL}			0.45	V	Iout = 1 mA, MISO, MOTION
Output High Voltage	V_{OH}	V_{DD} -0.45			V	Iout = -1 mA, MISO, MOTION
Input Capacitance	C_{in}		50		pF	MOSI, NCS, SCLK

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-4005, and to read out the motion information. The port is a four wire serial port. The host micro-controller always initiates communication; the ADNS-4005 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is at tri-state.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Power Management Modes

The ADNS-4005 has three power-saving modes. Each mode has a different motion detection period with its respective response time to mouse motion. Response Time is the time taken for the sensor to 'wake up' from rest mode when motion is detected. When left idle, the sensor automatically changes or downshift from Run mode to Rest1, to Rest2 and finally to Rest3 which consumes the least current. Do note that current consumption is the lowest at Rest3 and highest at Rest1, however time required for sensor to respond to motion from Rest1 is the shortest and longest from Rest3. Downshift Time is the elapsed time (under no motion condition) from current mode to the next mode for example, it takes 10s for the sensor that is in Rest1 to change to Rest2. The typical response time and downshift time for each mode is shown in the following table. However, user can change the default time setting for each mode via register 0x0e through 0x13.

Mode	Response Time (Typical)	Downshift Time (Typical)
Rest 1	20 ms	<1 s
Rest 2	100 ms	10 s
Rest 3	500 ms	600 s

Note:
These default timings are subject to changes after characterization.

Another feature in ADNS-4005 that can be used to optimize the power consumption of the optical mouse system is the Motion Interrupt Output or MOTION pin (pin 3). It allows the host controller to be in sleep mode (or lowest operating current mode) when there is no motion detected after some time instead of consistently be in active mode and polling motion data from the sensor. When motion is detected, the sensor will send the motion interrupt signal through pin 3 to the controller to wake it up from sleep mode to resume its motion detection routine for navigation position and direction update.

MOTION Detection Routine

Typically in the motion detection routine, MCU will poll the sensor for valid motion data by checking on the MOTION_ST bit in MOTION_ST register. If MOTION_ST bit is set, motion data in DELTA registers is valid and ready to be read by the MCU. For 8-bit motion reporting the DELTA registers are DELTA_X and DELTA_Y and for 12-bit motion reporting the DELTA registers are DELTA_X, DELTA_Y and DELTA_XY_HIGH.

MOTION Function

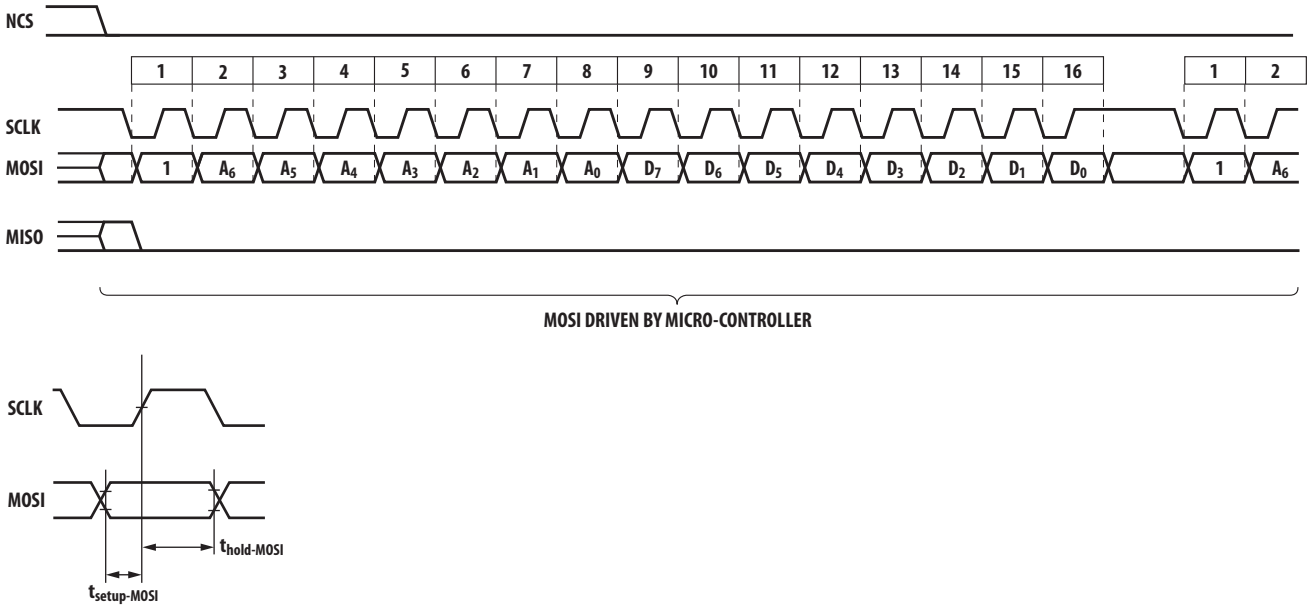
MOTION output signal (pin 3) can be used as interrupt input to the microcontroller of the mouse to trigger the controller to read the motion data from the sensor whenever there is motion detected by the sensor. The MOTION signal can be configured to be level or edge triggered, active high or low by setting the bits in MOTION_CTRL register.

For active high level-triggered configuration, the MOTION pin level will be driven high as long the MOTION bit in register 0x02 is set and there is motion data in DELTA registers ready to be read by the microcontroller. Once all the motion data has been read, DELTA registers value become zero, MOTION bit is reset and the MOTION pin level is driven low.

For active high edge-triggered configuration, a pulse of 380ns (typical) will be sent through the MOTION pin when there is motion detected by the sensor during rest modes. The pulse can be used as interrupt input to activate the microcontroller from its sleep mode to enter into run mode to start polling the sensor for motion data by monitoring MOTION_ST bit (set whenever there is valid motion data) in MOTION register (0x02) and reading DELTA registers until MOTION_ST bit is reset.

Write Operation

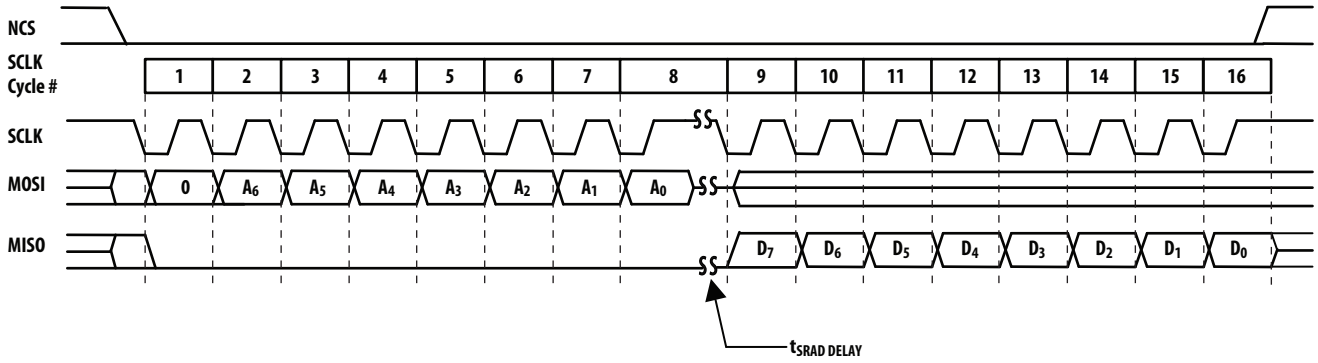
Write operation, defined as data going from the micro-controller to the ADNS-4005, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate write sequence. The second byte contains the data. The ADNS-4005 reads MOSI on rising edges of SCLK.

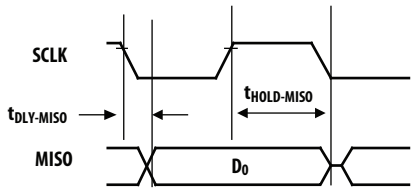


MOSI setup and hold time during write operation

Read Operation

A read operation, defined as data going from the ADNS-4005 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-4005 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.



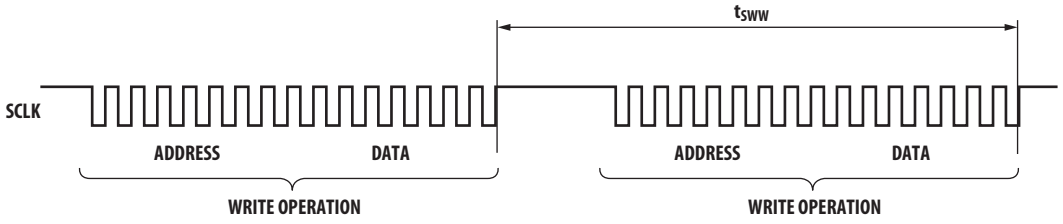


MOSI delay and hold time during read operation

Note: The 500 ns minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-4005. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-4005 will hold the state of data on MISO until the falling edge of SCLK.

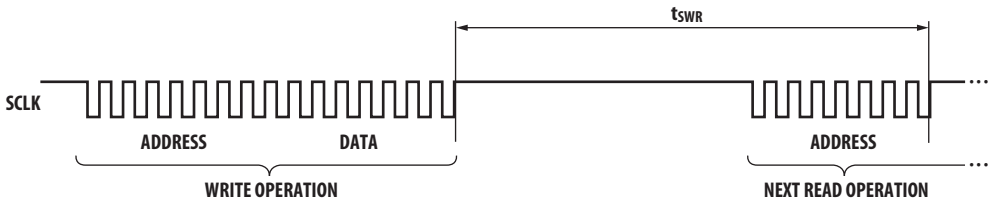
Required Timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.



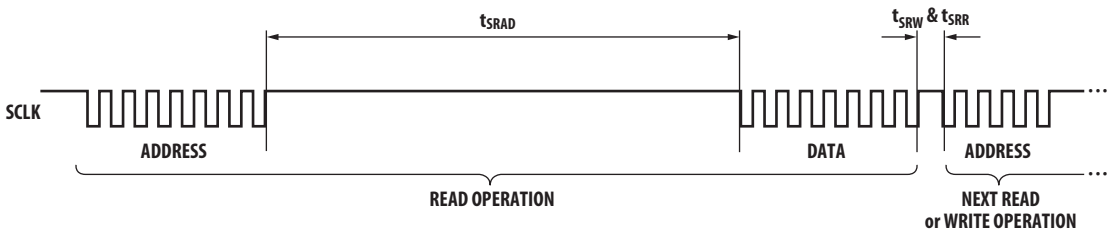
Timing between Two Write Commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.



Timing between Write and Read Commands

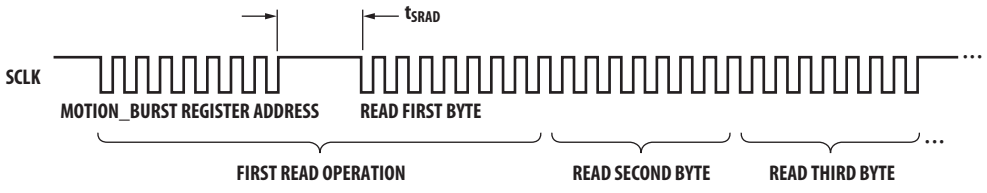
If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.



Timing between Read and Subsequent Write or Read Commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADNS-4005 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Motion Burst Timing



Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is initiated by reading the MOTION_BURST register (0x63). The ADNS-4005 will respond with the contents of the DELTA_X, DELTA_Y, SQUAL, SHUT_HI, SHUT_LO, and PIX_MAX and PIX_ACCUM registers in that order. The burst transaction can be terminated anywhere in the sequence after the DELTA_Y value by bringing the NCS pin high. The default value in BURST_READ_FIRST register (0x42) is the address of the DELTA_X register. The address that is specified in the BURST_READ_FIRST register can be changed to address 0x00 – 0x02 (PROD_ID – MOTION_ST) or 0x05 – 0x08 (SQUAL – PIX_MAX).

In 12-bit motion reporting there will be an extra content in DELTA_XY_HIGH (register 0x0c), to be read out in the order of DELTA_X, DELTA_Y, DELTA_XY_HIGH, SQUAL, SHUT_HI, SHUT_LO, PIX_MAX and PIX_ACCUM. The rest of the burst mode operation is the same as 8-bit motion reporting.

After reading the MOTION_BURST address (0x63), the microcontroller must wait t_{SRAD} before starting to read the continuous data bytes. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Reset

During power-up, the ADNS-4005 does not need a power on reset as there is an internal circuitry that performs power on reset in the sensor. However it can be reset by writing 0x5a to register 0x3a. A full reset will thus be executed and any register settings must be reloaded.

Power Down

The ADNS-4005 can be set to Power Down mode by writing 0x02 to register 0x0d to disable the sensor. In addition, the SPI port should not be accessed during power down. Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted. The table below shows the state of various pins during power down. To exit Power Down, write 0x5a to register 0x3a to reset the sensor in order to wake it up. A full reset will thus be executed. Wait t_{WAKEUP} before accessing the SPI port. Any register settings must then be reloaded.

Pin	During Power Down
MOTION	Undefined
NCS	Functional[1]
MISO	Undefined
SCLK	Functional[2]
MOSI	Functional[2]
XY_LED	Low current

Notes:
1. NCS pin must be held to 1 (HIGH) if SPI bus is shared with other devices. It can be in either state if the sensor is the only device in connected to the host micro-controller.
2. Reading of registers should only be performed after exiting from the power down mode. Any read operation during power down will not reflect the actual data of the registers.

Power and Reset Sequence

Please set the following setting upon power up and reset.

1. Set register 0x0D, to 0x81.
2. Set register 0x6D, to 0x41.
3. Set register 0x6E, to 0xBE.
4. Set register 0x70, to 0x69.
5. Set register 0x71, to 0x55.
6. Set register 0x72, to 0x46.
7. Set register 0x73, to 0x23.
8. Set register 0x74, to 0x2D.
9. Set register 0x75, to 0x1E.
10. Set register 0x76, to 0x0F.
11. Set register 0x77, to 0x05.

Registers

The ADNS-4005 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register Name	Register Description	Read/Write	Default Value
0x00	PROD_ID	Product ID	R	0x2A
0x01	REV_ID	Revision ID	R	0x00
0x02	MOTION_ST	Motion Status	R	0x00
0x03	DELTA_X	Lower byte of Delta_X	R	0x00
0x04	DELTA_Y	Lower byte of Delta_Y	R	0x00
0x05	SQUAL	Squal Quality	R	0x00
0x06	SHUT_HI	Shutter Open Time (Upper 8-bit)	R	0x00
0x07	SHUT_LO	Shutter Open Time (Lower 8-bit)	R	0x64
0x08	PIX_MAX	Maximum Pixel Value	R	0xD0
0x09	PIX_ACCUM	Average Pixel Value	R	0x80
0x0a	PIX_MIN	Minimum Pixel Value	R	0x00
0x0b	PIX_GRAB	Pixel Grabber	R/W	0x00
0x0c	DELTA_XY_HIGH	Upper 4 bits of Delta X and Y displacement	R	0x00
0x0d	MOUSE_CTRL	Mouse Control	R/W	0x01
0x0e	RUN_DOWNSHIFT	Run to Rest1 Time	R/W	0x08
0x0f	REST1_PERIOD	Rest1 Period	R/W	0x01
0x10	REST1_DOWNSHIFT	Rest1 to Rest2 Time	R/W	0x1f
0x11	REST2_PERIOD	Rest2 Period	R/W	0x09
0x12	REST2_DOWNSHIFT	Rest2 to Rest3 Time	R/W	0x2f
0x13	REST3_PERIOD	Rest3 Period	R/W	0x31
0x22	PERFORMANCE	Performance	R/W	0x00
0x3a	RESET	Reset	W	0x00
0x3f	NOT_REV_ID	Inverted Revision ID	R	0xff
0x40	LED_CTRL	LED Control	R/W	0x00
0x41	MOTION_CTRL	Motion Control	R/W	0x40
0x42	BURST_READ_FIRST	Burst Read Starting Register	R/W	0x03
0x45	REST_MODE_CONFIG	Rest Mode Configuration	R/W	0x00
0x63	MOTION_BURST	Burst Read	R	0x00

PROD_ID Address: 0x00

Product ID Register

Access: Read Reset Value: 0x2A

Bit	7	6	5	4	3	2	1	0
Field	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0

Data Type: 8-Bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-4005. The value in this register does not change; it can be used to verify that the serial communications link is functional.

REV_ID Address: 0x01

Product ID Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0

Data Type: 8-Bit unsigned integer

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

MOTION_ST Address: 0x02

Motion Status Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MOTION_ST	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Data Type: Bit field.

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOTION_ST bit is set, then the user should read registers 0x03 (DELTA_X) and 0x04 (DELTA_Y) to get the accumulated motion data. Read this register before reading the DELTA_X and DELTA_Y registers. Writing any data into this register clears MOTION_ST bit, DELTA_X and DELTA_Y registers. However the written data byte will not be saved.

Bit	Field Name	Description
7	MOTION_ST	Motion detected since last report **0 = No motion (default)** 1 = Motion occurred, data in DELTA_X and DELTA_Y registers ready to be read
6-0	RSVD	Reserved

DELTA_X Address: 0x03

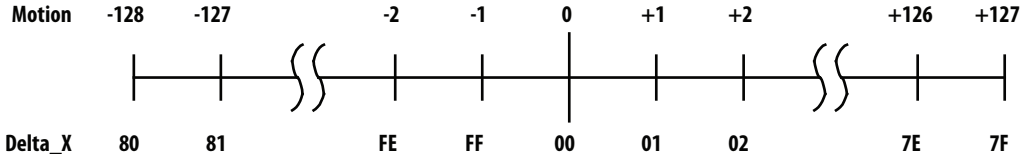
X Displacement Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X7	X6	X5	X4	X3	X2	X1	X0

Data Type: Eight bit 2's complement number.

USAGE: X-axis movement in counts since last report. Absolute value is determined by resolution. Reading this register clears the content of this register.



NOTE: Avago RECOMMENDS that registers 0x03, 0x04 and 0x0c be read consecutively in 12-bit motion reporting.

DELTA_Y Address: 0x04

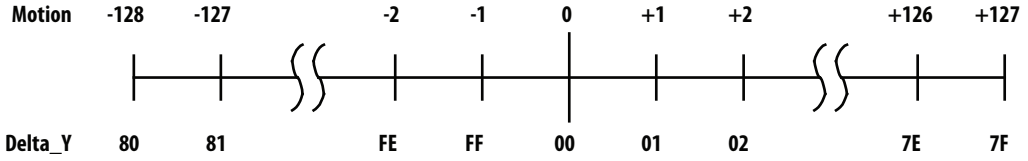
Y Displacement Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Data Type: Eight bit 2's complement number.

USAGE: Y-axis movement in counts since last report. Absolute value is determined by resolution. Reading this register clears the content of this register.



NOTE: Avago RECOMMENDS that registers 0x03, 0x04 and 0x0c be read consecutively in 12-bit motion reporting.

SQUAL Address: 0x05

Squal Quality Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SQ7	SQ6	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

Data Type: Upper 8 bits of a 9-bit unsigned integer.

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.

The maximum SQUAL register value is 180. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 250 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

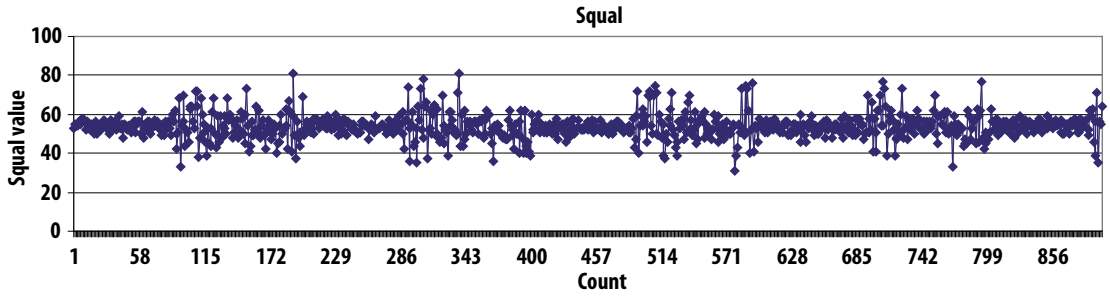


Figure 9. Squal values (white paper)

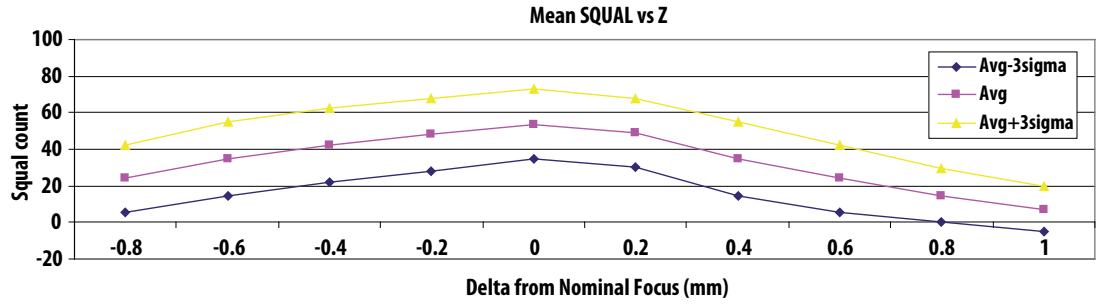


Figure 10. Mean squal vs. Z (White Paper)

SHUT_HI Address: 0x06

Shutter Open Time (Upper 8-bits) Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	S15	S14	S13	S12	S11	S10	S9	S8

SHUT_LO Address: 0x07

Shutter Open Time (Lower 8-bits) Register

Access: Read Reset Value: 0x64

Bit	7	6	5	4	3	2	1	0
Field	S7	S6	S5	S4	S3	S2	S1	S0

Data Type: Sixteen bit unsigned integer.

USAGE: Units are in clock cycles. Read SHUT_HI first, then SHUT_LO. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

PIX_MAX Address: 0x08

Maximum Pixel Value Register

Access: Read Reset Value: 0xD0

Bit	7	6	5	4	3	2	1	0
Field	MP7	MP6	MP5	MP4	MP3	MP2	MP1	MP0

Data Type: Eight-bit number.

USAGE: Store the highest pixel value in current frame. Minimum value = 0, maximum value = 254. The highest pixel value may vary with different frame.

PIX_ACCUM Address: 0x09

Average Pixel Value Register

Access: Read Reset Value: 0x80

Bit	7	6	5	4	3	2	1	0
Field	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0

Data Type: High 8-bits of an unsigned 17-bit integer.

USAGE: This register stores the accumulated pixel value of the last image taken. This register can be used to find the average pixel value, where Average Pixel = (register value AP[7:0])* 1.058

The maximum accumulated value is 122936 but only bits [16:9] are reported, therefore the maximum register value is 240. The minimum is 0. The PIX_ACCUM value may vary with different frame.

PIX_MIN Address: 0x0a

Minimum Pixel Value Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP7	MP6	MP5	MP4	MP3	MP2	MP1	MP0

Data Type: Eight-bit number.

USAGE: Store the lowest pixel value in current frame. Minimum value = 0, maximum value = 254. The minimum pixel value may vary with different frame.

PIX_GRAB Address: 0x0b

Pixel Grabber Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	PG_VALID	PG6	PG5	PG4	PG3	PG2	PG1	PG0

Data Type: Eight bit word.

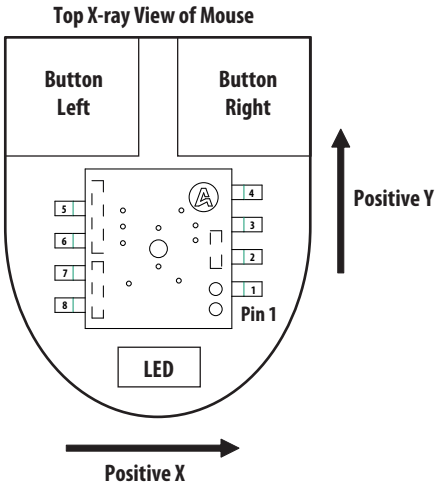
USAGE: The pixel grabber captures 1 pixel per frame. Bit-7 (MSB) of this register will be set to indicate that the 7-bit pixel data (PG[6:0]) is valid for grabbing. In a 22x22 pixel array, it will take 484 read operations to grab all the pixels to form the complete image.

Bit(s)	Field Name	Description
7	PG_VALID	Pixel Grabber Valid
6:0	PG[6:0]	Pixel Data

NOTE: Any write operation into this register will reset the grabber to origin (pixel 0 position). The sensor should not be moved before the 484 read operations are completed to ensure original data is grabbed to produce good (uncorrupted) image.

22X22 Pixel Array Address Map – (View from top of sensor)

	462	440	418	396	374	352	330	308	286	264	242	220	198	176	154	132	110	88	66	44	22	0	First
	463	441	419	397	375	353	331	309	287	265	243	221	199	177	155	133	111	89	67	45	23	1	
	464	442	420	398	376	354	332	310	288	266	244	222	200	178	156	134	112	90	68	46	24	2	
	465	443	421	399	377	355	333	311	289	267	245	223	201	179	157	135	113	91	69	47	25	3	
	466	444	422	400	378	356	334	312	290	268	246	224	202	180	158	136	114	92	70	48	26	4	
	467	445	423	401	379	357	335	313	291	269	247	225	203	181	159	137	115	93	71	49	27	5	
	468	446	424	402	380	358	336	314	292	270	248	226	204	182	160	138	116	94	72	50	28	6	
	469	447	425	403	381	359	337	315	293	271	249	227	205	183	161	139	117	95	73	51	29	7	
	470	448	426	404	382	360	338	316	294	272	250	228	206	184	162	140	118	96	74	52	30	8	
	471	449	427	405	383	361	339	317	295	273	251	229	207	185	163	141	119	97	75	53	31	9	
	472	450	428	406	384	362	340	318	296	274	252	230	208	186	164	142	120	98	76	54	32	10	
	473	451	429	407	385	363	341	319	297	275	253	231	209	187	165	143	121	99	77	55	33	11	
	474	452	430	408	386	364	342	320	298	276	254	232	210	188	166	144	122	100	78	56	34	12	
	475	453	431	409	387	365	343	321	299	277	255	233	211	189	167	145	123	101	79	57	35	13	
	476	454	432	410	388	366	344	322	300	278	256	234	212	190	168	146	124	102	80	58	36	14	
	477	455	433	411	389	367	345	323	301	279	257	235	213	191	169	147	125	103	81	59	37	15	
	478	456	434	412	390	368	346	324	302	280	258	236	214	192	170	148	126	104	82	60	38	16	
	479	457	435	413	391	369	347	325	303	281	259	237	215	193	171	149	127	105	83	61	39	17	
	480	458	436	414	392	370	348	326	304	282	260	238	216	194	172	150	128	106	84	62	40	18	
	481	459	437	415	393	371	349	327	305	283	261	239	217	195	173	151	129	107	85	63	41	19	
	482	460	438	416	394	372	350	328	306	284	262	240	218	196	174	152	130	108	86	64	42	20	
Last	483	461	439	417	395	373	351	329	307	285	263	241	219	197	175	153	131	109	87	65	43	21	



DELTA_XY_HIGH Address: 0x0c

Upper 4 bits Delta-X/Y Displacement Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	DELTA_X_HI3	DELTA_X_HI2	DELTA_X_HI1	DELTA_X_HI0	DELTA_Y_HI3	DELTA_Y_HI2	DELTA_Y_HI1	DELTA_Y_HI0

Data Type: Eight bit 2's complement number.

USAGE: Concatenate the values to have a 12-bit reporting for the motion.

X motion = {DELTA_XY_HIGH[7:4], DELTA_X} , Y motion = DELTA_XY_HIGH[3:0], DELTA_Y}

Bit(s)	Field Name	Description
7:4	DELTA_X_HI	Upper 4 bits of DELTA_X displacement for 12-bit reporting
3:0	DELTA_Y_HI	Upper 4 bits of DELTA_Y displacement for 12-bit reporting

NOTE: Avago RECOMMENDS that registers 0x03, 0x04 and 0x0c be read consecutively in 12-bit motion reporting.

MOUSE_CTRL Address: 0x0d

Mouse Control Register

Access: Read/Write Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	BIT_REPORTING	RSVD	RES_EN	RES2	RES1	RES0	PD	RES_D

Data Type: Bit field.

USAGE: Resolution and chip reset information can be accessed or to be edited by this register.

Bit(s)	Field Name	Description
7	BIT_REPORTING	0x0: 8-bit motion reporting 0x1: 12-bit motion reporting. Read register 0x03, 0x04 and 0x0c.
6	RSVD	Reserved
5	RES_EN	Enable resolution settings set on MOUSE_CTRL [4:2]
4:2	RES [2:0]	Resolution 0x0: 1000 dpi 0x1: 250 dpi 0x2: 500 dpi 0x3: 1250 dpi 0x4: 1500 dpi 0x5: 1750 dpi 0x6: 2000 dpi
1	PD	Power Down
0	RES_D	0x0: 500 dpi 0x1: 1250 dpi (default)

NOTE: Setting MOUSE_CTRL [5] bit to '1' will supersede and ignore MOUSE_CTRL [0] setting.

RUN_DOWNSHIFT Address: 0x0e

Run to Rest1 Time Register

Access: Read/Write Reset Value: 0x08

Bit	7	6	5	4	3	2	1	0
Field	RUD7	RUD6	RUD5	RUD4	RUD3	RUD2	RUD1	RUD0

Data Type: Eight bit number.

USAGE: This register sets the Run to Rest1 mode downshift time. The time is the value of this register multiply by 8 times of position mode period.

Default downshift time = 8 * 8 * 4 = 256 ms

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 40 -> write 0x40H into register 0x22H prior to writing into this register
w 0e XX -> writing into this register
w 22 00 -> write 0x00H into register 0x22H after writing into this register

REST1_PERIOD Address: 0x0f

Rest1 Period Register

Access: Read/Write Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	RIP7	RIP6	RIP5	RIP4	RIP3	RIP2	RIP1	RIP0

Data Type: Eight bit number.

USAGE: This register sets the Rest1 period. Period = (register value R1P [7:0] +1) x 10 ms (typical slow clock period). **Min value for this register is 0x01**. Max value is 0xFD.

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 40 -> write 0x40H into register 0x22H prior to writing into this register
w 0f XX -> writing into this register
w 22 00 -> write 0x00H into register 0x22H after writing into this register

REST1_DOWNSHIFT Address: 0x10

Rest1 to Rest2 Downshift Time Register

Access: Read/Write Reset Value: 0x1f

Bit	7	6	5	4	3	2	1	0
Field	R1D7	R1D6	R1D5	R1D4	R1D3	R1D2	R1D1	R1D0

Data Type: Eight bit number.

USAGE: This register sets the Rest1 to Rest2 mode downshift time. Time = (register value R1D [7:0]) x (Rest1 period) x 16. Min value for this register is 0x01.

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 40 -> write 0x40H into register 0x22H prior to writing into this register
w 10 XX -> writing into this register
w 22 00 -> write 0x00H into register 0x22H after writing into this register

REST2_PERIOD Address: 0x11

Rest2 Period Register

Access: Read/Write Reset Value: 0x09

Bit	7	6	5	4	3	2	1	0
Field	R2P7	R2P6	R2P5	R2P4	R2P3	R2P2	R2P1	R2P0

Data Type: Eight bit number.

USAGE: This register sets the Rest2 period. Period = (register value R2P [7:0] +1) x 10 ms (typical slow clock period). Min value for this register is 0x01. Max value is 0xFD.

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 40 -> write 0x40H into register 0x22H prior to writing into this register
w 11 XX -> writing into this register
w 22 00 -> write 0x00H into register 0x22H after writing into this register

REST2_DOWNSHIFT Address: 0x12

Rest2 to Rest3 Downshift Time Register

Access: Read/Write Reset Value: 0x2f

Bit	7	6	5	4	3	2	1	0
Field	R2D7	R2D6	R2D5	R2D4	R2D3	R2D2	R2D1	R2D0

Data Type: Eight bit number.

USAGE: This register sets the Rest1 to Rest2 mode downshift time. Time = (register value R2D [7:0]) x (Rest2 period) x 128. Min value for this register is 0x01.

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 40 -> write 0x40H into register 0x22H prior to writing into this register
w 12 XX -> writing into this register
w 22 00 -> write 0x00H into register 0x22H after writing into this register

REST3_PERIOD Address: 0x13

Rest3 Period Register

Access: Read/Write Reset Value: 0x31

Bit	7	6	5	4	3	2	1	0
Field	R3P7	R3P6	R3P5	R3P4	R3P3	R3P2	R3P1	R3P0

Data Type: Eight bit number.

USAGE: This register sets the Rest3 period. Period = (register value R3P [7:0] +1) x 10 ms (typical slow clock period). Min value for this register is 0x01. Max value is 0xFD.

NOTE: Writing into this register when the sensor itself is operating in this rest mode may result in unexpected behavior of the sensor. To avoid this from happening, below commands should be incorporated prior and after the write command into this register.

w 22 40 -> write 0x40H into register 0x22H prior to writing into this register
w 13 XX -> writing into this register
w 22 00 -> write 0x00H into register 0x22H after writing into this register

PERFORMANCE Address: 0x22

Performance Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RSVD	FORCE3	FORCE1	FORCE0	RSVD	RSVD	RSVD	RSVD

Bit(s)	Field Name	Description
7	RSVD	Reserved
6:4	FORCE[2:0]	force modes **0x0: Normal operation.** 0x1: force mode rest 1. 0x2: force mode rest 2. 0x3: force mode rest 3. 0x4: force mode run 1. 0x5: force mode run 2. 0x6: force mode idle.
3:0	RSVD	Reserved

RESET Address: 0x3a

Reset Register

Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RST7	RST6	RST5	RST4	RST3	RST2	RST1	RST0

Data Type: Eight bit unsigned integer.

USAGE: This register is used as chip reset by writing 0x5a into this register.

NOT_REV_ID Address: 0x3f

Inverted Revision ID Register

Access: Read Reset Value: 0xff

Bit	7	6	5	4	3	2	1	0
Field	RRID7	RRID6	RRID5	RRID4	RRID3	RRID2	RRID1	RRID0

Data Type: Eight bit unsigned integer.

USAGE: This register contains the inverse of the revision ID which is located at register 0x01.

LED_CTRL Address: 0x40

LED Control Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	LCOF	RSVD	RSVD	RSVD

Data Type: Eight bit unsigned integer.

USAGE: This register is used to control the LED operating mode.

Bit(s)	Field Name	Description
7:4	RSVD	Reserved
3	LCOF	**0 : Normal operation (default)** 1 : LED Continuous Off
2:0	RSVD	Reserved

MOTION_CTRL Address: 0x41

Motion Control Register

Access: Read/Write Reset Value: 0x40

Bit	7	6	5	4	3	2	1	0
Field	MOT_A	MOT_S	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Data Type: Eight bit unsigned integer.

USAGE: This register is used to set the feature of MOTION interrupt output. If MOT_S bit is clear, the MOTION pin is level-sensitive. With active low (MOT_A bit is clear) level-sensitive configuration, the MOTION pin will be driven low when there is motion detected indicating there is motion data in DELTA_X and DELTA_Y registers. The mouse microcontroller can read MOTION_ST register, DELTA_X register, and then DELTA_Y register sequentially. After all the motion data has been read, DELTA_X and DELTA_Y registers will be zero, the MOTION pin will be driven high by the sensor.

If MOT_S is set, the MOTION pin is edge sensitive. If MOT_A is also set, it means active high or rising edge triggered. Whenever there is motion detected by the sensor, a pulse (~380ns) will be sent out through this pin. This pulse can be used to trigger or wake the controller up from its sleep mode to read motion data from the sensor. The controller can then read MOTION_ST register, DELTA_X register, and then DELTA_Y register sequentially. (Refer to Motion Function for more information).

Bit(s)	Field Name	Description
7	MOT_A	MOTION Active **0 : LOW (default)** 1 : HIGH
6	MOT_S	MOTION Sensitivity 0 : Level sensitive **1 : Edge sensitive (default)**
5:0	RSVD	Reserved

BURST_READ_FIRST Address: 0x42

Burst Read Starting Address Register

Access: Read/Write Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
Field	BM7	BM6	BM5	BM4	BM3	BM2	BM1	BM0

Data Type: Eight bit unsigned integer.

USAGE: This register provides the starting register address the sensor will read during Burst Mode. For more information, refer to Burst Mode Operation.

REST_MODE_CONFIG Address: 0x45

Rest Mode Configuration Register

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RM1	RM0	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Data Type: Eight bit unsigned integer.

USAGE: This register is used to set the operating mode of the ADNS-4005.

Bit(s)	Field Name	Description
7:6	RM[1:0]	Sensor Operating Mode **0x00: Normal (default)** 0x01: Rest 1 0x02: Rest 2 0x03: Rest 3
5:0	RSVD	Reserved

Read operation to REST_MODE_CONFIG indicates which mode the sensor is in. Write operation into this register will force the sensor into rest modes (Rest 1, 2 or 3). Write the value 0x40 into 0x45 register to force sensor into Rest 1, 0x80 to Rest 2 or 0xC0 to Rest 3. To get out of any forced rest mode, write 0x00 into this register to set back to normal mode.

MOTION_BURST Address: 0x63

Burst Read Register

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0

Data Type: Various.

USAGE: This register is used to enable burst mode. Burst is initiated by a read of this register, which will then return continuous data starting from the address stored in BURST_READ FIRST register through BURST_READ_LAST register. Burst read must read the exact number of addresses set in order to complete the burst operation. For more information refer to Burst Mode Operation section.

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