HAMED SEYEDROUDBARI

US Citizen

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OBJECTIVE

Seeking full-time opportunities to research and develop forms of in-network computing to accelerate high-bandwidth and latency-sensitive datacenter workloads.

EDUCATION

2019 - present Ph.D. - Electrical and Computer Engineering – **GPA 4.0**

- Georgia Institute of Technology (Georgia Tech), Atlanta, GA
- Research Advisor: Dr. Alexandros Daglis
- Topic: Enabling an application-aware network with SmartNICs to accelerate latency-critical online services.

2015 - 2019 B.S. - Computer Engineering – **GPA 3.93**

- California State University, Northridge (CSUN), Northridge, CA

EMPLOYMENT

2020 - present Graduate Research Assistant – Georgia Tech, Atlanta, GA

Exploring unique in-network compute offloads (mainly on smartNICs) to alleviate processing load from server CPUs.

1. Load Balancing µs-scale RPCs (published at HPCA'23)
   - Insight: µs-scale RPCs require immediate load imbalance detection and remediation mechanism operating on a per-packet granularity.
   - Adaptive load balancing to intelligently steer packets into user space queues at line rate, improving throughput under SLO and reducing tail response latency.
   - Implemented on Mellanox Innova Flex-4 FPGA SmartNIC
   - Evaluated on RDMA (UD/UC/RC) microbenchmark and Masstree-RDMA key-value store with various service time distributions.

2. Data Movement (on ArXiv)
   - Insight: Moving packets across PCIe increases contention and PCIe interface latency.
     - Shallow network functions only require packet header for processing.
   - Implemented FPGA emulation of mechanism to slice packet into header and payload on ingress, sending only the header to the host, storing payload on the NIC. Payload is spliced back to header on egress.
   - Enabling payload slicing eliminates data movement bottlenecks between the NIC and server, reducing tail response latency.

3. In progress
   - SmartNIC-enabled mechanism to load balance active RDMA connections across CPU cores.

2024 - present Research Scientist – Microsoft (Remote)

- Optimize RDMA networks to extract peak network utilization for AI workloads by investigating loss recovery mechanisms when packets arrive mis-ordered.
- Develop simulator in SystemC to simulate and analyze NIC-based loss recovery mechanisms (i.e., go-back-n, selective retransmit) for a RDMA/RoCE network.
- Analyze performance by tuning simulator knobs (e.g., receiver queue depth, memory latency, link latency, timeout) and observing metrics such as flow completion and time tail latency.
- Propose NIC architectural optimizations to enable support for recovery from multi-path packet losses.

2022 Research Intern (Systems) – Arm Research, Austin, TX

- Developed high performance RDMA, RoCE based microbenchmark to identify system bottlenecks (outperforming state-of-the-art perftest from NVIDIA's UCX library).
- Characterized performance of BlueField-2 DPU in terms of peak sustainable throughput and communication latency and gauged its potential as a candidate for accelerating latency critical workloads.
- Demonstrated the Bluefield-2 DPU can boost server's peak sustained throughput by 66% without incurring additional cost for cloud service provider.

2021 SSD Platform Architecture Pathfinding Intern – Intel Corporation, Remote, USA

- Devised statistical probability based adaptive load balancing methodology for multi-tenant workloads to configure bandwidth and Quality of Service (QoS) delivery for each tenant by leveraging device physics.
- Designed scheduler with closed-loop credit-based admission control to balance SSD die loading, and balance bandwidth and QoS of tenants, while preventing resource wastage and starvation for any tenant.
- Implemented scheduler within FIO using SPDK and evaluated on NVMe storage device to demonstrate scheduler's efficiency gains while meeting SLO.

TECHNICAL SKILLS

Programming Language	: C, C++, SystemC, Python
HDL	: Verilog, SystemVerilog
Toolchain	: Xilinx Vivado, HLS, Vitis, Synopsys VCS, Design Compiler
NIC Platforms	: Mellanox Innova Flex-4 SmartNIC, Bluefield-2 DPU
Computer Networks	: Ethernet, RDMA, RoCE, IBVerbs, BGP, TCP/IP, UDP

FELLOWSHIPS/AWARDS

2019	President's Fellowship, Georgia Tech
2019	Outstanding Graduating Senior Award, CSUN
2018	Outstanding Student Employee Aware, CSUN
2018	STEM Advantage Scholar
2018	Robert Sprague Foundation Scholarship
2017, 2018	University Scholarship, CSUN
2016	James R. Simpson Merit Scholarship, CSUN
2015	Honors at Entrance Scholarship, CSUN

PUBLICATIONS

Turbo: SmartNIC-enabled Dynamic Load Balancing of µs-scale RPCs
H. Seyedroudbari, S. Vanavasam, A. Daglis
IEEE International Symposium on High-Performance Computer Architecture (HPCA 2023)

NFSlicer: Data Movement Optimization for Shallow Network Functions
A. Sarma, **H. Seyedroudbari,** H. Gupta, U. Ramachandran, A. Daglis
ArXiv, March 2022