Hameedah Sultan

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Education

2015 – present
- **Ph.D.**, Indian Institute of Technology Delhi
  Thesis title: *A Fast Leakage-aware Thermal Simulator*
  Advisor: Dr. Smruti R. Sarangi

2013 – 2015
- **M.Tech.**, Indian Institute of Technology Delhi in VLSI Design Tools and Technology.
  Thesis title: *A Fast 3D Thermal Simulator*.
  Advisor: Dr. Smruti R. Sarangi
  GPA: **9.47/10 (Rank 1)**

2009 – 2013
- **B.Tech.**, Aligarh Muslim University in Electronics Engg.
  Thesis title: *Brain Computer Interface for Hand Movement Detection*.
  GPA: **9.89/10 (Rank 1, Gold medallist)**

Research

Ph.D. Projects

- **A Survey of Architectural Thermal Simulators**
  We conducted an exhaustive survey of architectural-level thermal simulation methods. This work was published in ACM Computing Surveys **(CSUR) 2019**.

- **Fast Leakage Aware Thermal Simulation**
  - In this work, we developed a fast leakage aware thermal simulator for 3D chips using Green's functions (impulse response of a unit power source). We formulate a set of equations and solve these using novel algebraic techniques and approximations to compute the thermal profile. Our simulator is analytical and exploits the radial symmetry in the thermal profile to reduce a 2D Fourier transform to a 1D Hankel transform. We obtain a 68X speedup as compared to competing simulators with an error limited to $1.5^{\circ}C$. This work was published in **DATE 2017**.
  - We extend the previous work to model the temperature profile in chips with microchannels using novel *residual Green's functions*. The boundary effects have been handled using a novel edge correction approach. Additionally, we incorporate piecewise linear leakage models in this work for improved accuracy. This work has been accepted in **TVLSI**.

- **Analytical Variability Aware Thermal Simulation**
  Process variation is increasingly becoming important as the device dimensions are decreasing. So, in this work, we consider the effects of process variation, temperature-dependent leakage power, and temperature-dependent conductivity together, and propose a closed-form solution for the Green's function considering all these effects. We reduce computations by identifying similar regions in the chip using k-means clustering during the process of computing the thermal map. We obtained a 700,000X speedup over state-of-the-art proposals with a mean absolute error limited to $0.7^{\circ}C$(1.5%). This work was published in **DAC 2020**.

- **Variability Aware Thermal Simulation using CNNs**
  An analytical process variation-aware thermal simulation method cannot be extended to complex geometries because of its complexity. So, we next propose a convolutional neural network for thermal estimation in the presence of variability that leverages the physics of the heat transfer. This approach

is capable of modeling modern-day 3D chips with microchannels and incorporates accurate leakage power models. The mean absolute error using our technique is 0.61$^{\circ}C$, for a maximum temperature rise of 67.5$^{\circ}C$(0.6%). This work has been submitted to **ASPDAC 2020**.

- **System-level Thermal Modeling**
  In this work, we propose an ultra-fast Green's function-based system-level thermal modeling approach for smartphones and tablets. We also propose fast polynomial models to quickly adapt the Green's function for a range of design parameters. This work has been submitted to **VLSID**.

- **Nanoscale Thermal Modeling**
  Traditional thermal simulation methods are based on solving the Fourier equation, which fails to hold at the nanometer level. At such small scales, quantum effects come into play and the Boltzmann equation has to be solved. In this work, we propose a hybrid Fourier-Boltzmann framework to compute the full-chip thermal profile. The chip-level temperature profile is obtained by solving the Fourier equation, and at the standard cell level, the gray Boltzmann equation is solved. These two are superimposed to obtain accurate full-chip thermal profile. We propose fast analytical methods to solve both of these equations. This work was published in **ICCAD 2019**, where it was nominated for the best paper award.

- **Noise aware Scheduling in Data Centers**
  In developing countries as well as small scale enterprises, employees often have to work near servers. These servers produce a lot of noise, which reduces employee productivity and can lead to long-term hearing problems. In this paper, we propose two heuristics to schedule workloads such that noise at targeted locations is reduced while keeping the temperature under certain thresholds. This paper was published in **ICS 2016**.

Past Projects

- **Architecture/ Digital Design Projects**
  - Implemented the AMD K6 out of order pipeline as an extension to the existing Tejas simulator, and analyzed its sensitivity to the number and latency of different functional units.
  - Implemented a bubble sort algorithm using VHDL on FPGA, where the inputs were taken from a block RAM on the board.
  - Implemented a timer in software using Microblaze. The timer setting inputs were taken from the DIP switches on the FPGA, and the time was output on the LEDs. The LEDs started blinking after the time ran out.
  - Designed a lift controller in VHDL, with the number of floors and lifts as generic parameters. The lift was based on Destination Floor Reservation System.

- **Analog/ Mixed Signal Projects**
  - Implemented an 8 bit divider in VHDL, and synthesized and implemented it on FPGA. Next we synthesized it for ASIC followed by floorplanning, power planning, clock tree synthesis, pre-CTS and post-CTS optimization and routing.
  - Designed a Schmitt Trigger in Cadence and created its layout, followed by post layout simulations.
  - An 8-bit Cyclic analog to digital converter was designed using recyclic folded cascode amplifier and implemented in Cadence.

- **Bachelor's Project**
  EEG signal processing was done to determine features for classification of executed wrist movements of four different kinds, to develop a Brain- Computer Interface (BCI) system.

Publications

1 **Sultan, H.**, & Sarangi, S. R. (n.d.). A fast leakage aware Green's function based thermal simulator for 3D chips. *IEEE Transactions on Very Large Scale Integration Systems (accepted)*.

2. **Sultan**, **H.**, & Sarangi, S. R. (2020). VarSim: A fast and accurate variability and leakage aware thermal simulator. *DAC*, 1–6.
3. **Sultan**, **H.**, Chauhan, A., & Sarangi, S. R. (2019). A survey of chip-level thermal simulators. *ACM Computing Surveys (CSUR)*, *52*(2), 1–35.
4. Varshney, S., **Sultan**, **H.**, Jain, P., & Sarangi, S. R. (2019). NanoTherm: An analytical Fourier-Boltzmann framework for full chip thermal simulations. *ICCAD*, 1–8 (nominated for the best paper award).
5. **Sultan**, **H.**, & Sarangi, S. R. (2017). A fast leakage aware thermal simulator for 3D chips. *2017 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 1733–1738.
6. **Sultan**, **H.**, Katiyar, A., & Sarangi, S. R. (2016). Noise aware scheduling in data centers. *Proceedings of the 2016 International Conference on Supercomputing*, 1–14.
7. Arora, A., Harne, M., **Sultan**, **H.**, Bagaria, A., & Sarangi, S. R. (2014). FP-NUCA: A fast NoC layer for implementing large NUCA caches. *IEEE Transactions on Parallel and Distributed Systems*, *26*(9), 2465–2478.
8. **Sultan**, **H.**, Ananthanarayanan, G., & Sarangi, S. R. (2014). Processor power estimation techniques: A survey. *International Journal of High Performance Systems Architecture*, *5*(2), 93–114.
9. Ghani, F., **Sultan**, **H.**, Anwar, D., Farooq, O., & Khan, Y. U. (2013). Classification of wrist movements using EEG signals. *Journal of Next Generation Information Technology (JNIT)*, *4*(8), 29–39.

Academic Services and Experience

Mentor

Master's students mentored	◆ I have mentored four master's students advised by Dr. Smruti R. Sarangi towards their thesis – Shashank Varshney, Ankit Gola, Anand Singh, and Anjali Agrawal. All four of them had their works published/submitted to leading EDA conferences.

Teaching Assistant

UG courses	◆ Introduction to Computer Science (**head TA**, 474 students), Digital Logic and System Design, Computer Architecture (basic course, **head TA**, 192 students).
PG courses	◆ Architecture of High Performance Computers (twice), Synthesis of Digital Systems, Computer Architecture (advanced course).

Reviewer

Journals	◆ JETC, TVLSI.
Conferences	◆ HiPC, VLSID, VDAT.

Funding Agency

SRC	◆ I was involved in writing a grant proposal titled "Ultra Fast Thermal Simulation of Electronic Systems" submitted to the Semiconductor Research Corporation (SRC). I have also been responsible for making or coordinating the creation of 9 out of 10 deliverables required by the funding agency so far.

Skills

Languages	◆ English, Hindi, Urdu.
Coding	◆ C, C++, Python, R, MATLAB, VHDL, Verilog.

Skills (continued)

Miscellaneous	◆ LaTeX, Mercurial, Cadence Spectre, Virtuoso, Encounter RTL Compiler, Eagle PCB Design Software, Xilinx ISE.

Awards and Achievements

- Paper nominated for the best paper award at ICCAD 2019.
- Awarded *Outstanding teaching assistant award* for COL100: Introduction to Computer Science, with 474 students. I was the head TA responsible for managing a team of 28 TAs.
- Ranked 48 out of 256135 candidates in the GATE 2013 exam.
- Held position among the top rankers of class/university throughout my academic career.
- First rank holder in the entire Faculty of Engineering in B.Tech. and the entire VLSI batch in M.Tech.
- Awarded two gold medals in B.Tech. for obtaining the first rank in the Department of Electronics Engineering as well as first rank in the entire Faculty of Engineering (all branches).
- Awarded University Merit Scholarship throughout B.Tech., and for Physics in class 11^{th} and 12^{th}.

References

Available on Request