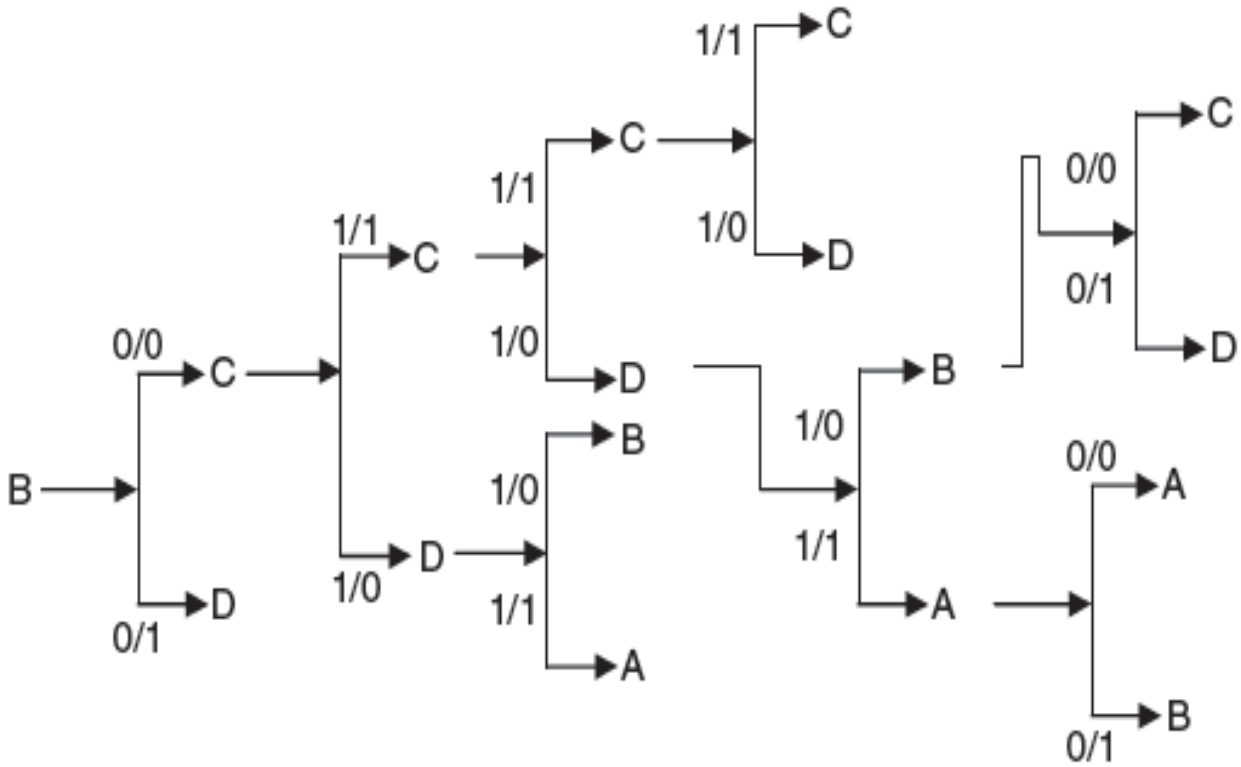
Solution: To retrieve the input sequence, first we need to check whether the machine is information lossless or not. The machine is information lossless as given in Example 4.20.

The output successor table for the given machine is

Solution: To retrieve the input sequence, first we need to check whether the machine is information lossless or not. The machine is information lossless as given in Example 4.20.

The output successor table for the given machine is

	NextState, I/P	
State	$z = 0$	$z = 1$
A	(A, 0), (B, 1)	–
B	(C, 0), (D, 1)	–
C	–	(D, 0), (C, 1)
D	–	(B, 0), (A, 1)



The final state is B, and thus the input is 01011.

24. Design a minimal inverse of the machine shown in the following table.

[WBUT 2007, 2008]

24. Design a minimal inverse of the machine shown in the following table.

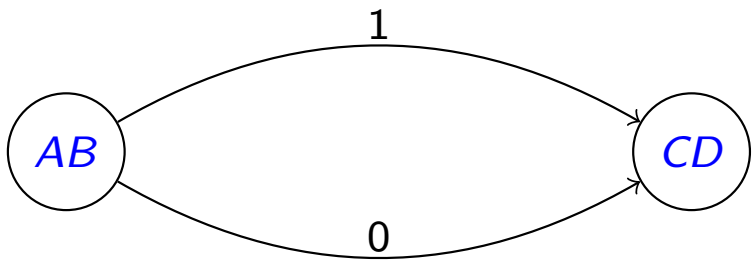
[WBUT 2007, 2008]

	NextState	
PresentState	$X = 0$	$X = 1$
A	C, 0	D, 1
B	D, 0	C, 0
C	A, 1	B, 1
D	C, 1	D, 1

Solution: To find the minimal inverse machine, fi rst we need to fi nd the order of losslessness of the machine.

PresentState	$z = 0$	$z = 1$
A	C	D
B	D	C
C	AB	–
D	–	CD
AB	CD	CD
CD	–	–

The testing graph is



It is loop-free. And the order of finiteness is 3.

Therefore, if we know the initial state and the values of three successive outputs produced by transitions from the initial state, we can determine the first input given to the machine. We need to determine a set of triples, denoted by $\{S(t), z(t+1),$ and $z(t+2)\}$. There are four states of the machine. The triples are

(A, 0, 0)	(B, 0, 1)	(C, 0, 0)	(D, 1, 0)
(A, 1, 1)	(B, 1, 0)	(C, 0, 1)	(D, 1, 1)

	$NextState, X$	
$PresentState$	$z = 0$	$z = 1$
(A, 0, 0)	(C, 0, 0), 0	(C, 0, 1), 0
(A, 1, 1)	(D, 1, 0), 1	(D, 1, 1), 1
(B, 0, 1)	(D, 1, 0), 0	(D, 1, 1), 0
(B, 1, 0)	(C, 0, 0), 1	(C, 0, 1), 1
(C, 0, 0)	(A, 0, 0), 0	(B, 0, 1), 1
(C, 0, 1)	(B, 1, 0), 1	(A, 1, 1), 0
(D, 1, 0)	(C, 0, 0), 0	(C, 0, 1), 0
(D, 1, 1)	(D, 1, 0), 1	(D, 1, 1), 1

Here, states (A, 0, 0), (D, 1, 0) and (A, 1, 1) and (D, 1, 1) are equivalent states as they produce the same next state and same output. Let us assign $(A, 0, 0)$ as $S_1, (A, 1, 1)$ as $S_2, (B, 0, 1)$ as $S_3, (B, 1, 0)$ as $S4, (C, 0, 0)$ as S_5, and $(C, 0, 1)$ as S_6.

The minimal inverse machine is

	$NextState, X$	
$PresentState$	$z = 0$	$z = 1$
S_1	$S_5, 0$	$S6, 0$
S_2	$S_1, 1$	$S2, 1$
S_3	$S_1, 0$	$S2, 0$
S_4	$S_5, 1$	$S6, 1$
S_5	$S_1, 0$	$S3, 1$
S_6	$S_4, 1$	$S2, 0$

Multiple Choice Questions

1. A palindrome cannot be recognized by any FSM because

a) An FSM cannot remember arbitrary, large amount of information

b) An FSM cannot deterministically fix the mid-point

c) Even if the mid-point is known, an FSM cannot find whether the second half of the string matches the first half

d) All of these

2. The basic limitation of an FSM is that

a) It cannot remember arbitrary, large amount of information

b) It cannot recognize grammars that are regular

that are not regular

d) All of these

3. The operation of synchronous circuits are controlled by

a) Input

b) State

c) Output

d) Clock pulses

4. The output of combinational circuit depends on

a) Present state

b) Past input

c) Present input

d) Present stored information and

5. The output of sequential circuit depends on

a) Present state

b) Past input

c) Present input

d) Present stored information and present input

6. For which of the following, FSM cannot be designed

a) Addition of two binary numbers

b) Subtraction of two binary numbers

c) Multiplication of two binary numbers

d) All of these

7. Which is true of the following?

a) A merger graph is a directed graph

b) A compatible graph is a directed graph

c) Both are not directed

d) None of these

8. A merger table is a substitute of

a) Merger graph

b) Compatible graph

c) Minimized machine

d) FSM

9. Two states are called 1-equivalent if

a) Both of the states produce 1

b) If both of the states produce the same output for string length 1

c) If both of the states produce the same output for same input.

d) If both of the states produce the same output for input 1.

10. Which is true for an incompletely specified machine?

a) All Next states are not mentioned

b) All outputs are not mentioned

c) All inputs are not mentioned

d) Both a and b

11. Compatible pairs are obtained from

a) Merger graph

b) Compatible graph

c) Testing table

graph is

a) The number of states of the machine

b) The number of compatible pairs

c) The number of states combinations

d) None of these

13. The number of vertices of a compatible graph is

a) The number of states of the machine

b) The number of compatible pairs

c) The number of states combinations

d) None of these

14. An FSM M is called a finite memory machine of order μ if the present state of the machine M can be obtained from

a) The last μ number of inputs and the corresponding μ number of next states

b) The last μ number of inputs and the corresponding μ number of outputs

c) The last μ number of next states and the corresponding μ number of outputs

d) The last μ number of inputs

15. A sequential machine M is called definite if there exists a least integer μ, so that the present state of the machine M can be uniquely obtained from the

a) Past μ number of inputs

b) Past μ number of outputs

c) Past μ number of next states

d) Past μ number of inputs, outputs, and next states

16. Which is sufficient to find the initial state of an information lossless machine from the input string?

a) Next state and output string

b) Final state and next state

c) Final state and output string

d) Final state, next state, and output string

17. The input sequence of an information lossless machine can be determined from the knowledge of

a) Only the output sequence

b) The output sequence and initial state

c) The output sequence, initial state, and final state

d) The initial state

18. Which is true of the following?

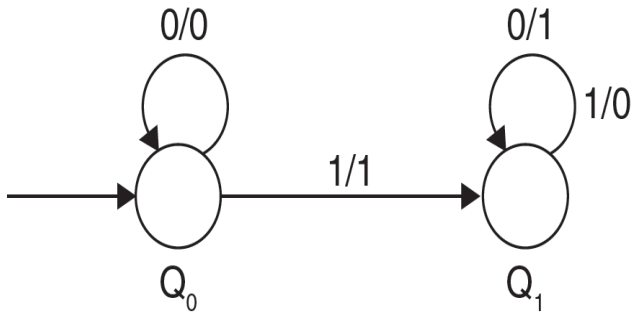
a) All information lossless machines are of finite order

b) Some information lossless machines are of finite order

c) Those machines which are not lossless of finite order are lossy

d) None of the above

19. The following diagram represents an FSM which takes as input a binary number from the least significant bit.



Which one of the following is true?

(a) It computes 1's complement of the input number

(b) It computes 2's complement of the input number

(c) It increments the input number

(d) It decrements the input number