



DVA494

Programming of Reliable Embedded Systems

Obed Mogaka | Hamid Mousavi | Masoud Daneshthalab

IDT, Malardalens University

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Vivado is a Design suite for AMD adaptive SoCs and FPGAs.

(This guide is based on Vivado version 2024.2 on a Windows system. The process is generally the same for other versions.)

Resources:

- Vivado Design Suite User Guide: Release Notes, Installation, and Licensing (UG973)
- AMD Download Webpage ¹

¹You need to create an account to download AMD design tools.

Step 1: Download the Unified Installer for Windows or Linux

Vivado
2022
2023
2023.2
Vivado Archive
ISE Archive
CAE Vendor Libraries Archive

Vivado™ Edition - 2024.2 Full Product Installation

Important Information

Vivado™ 2024.2 is now available for download!

Advanced Flow for Place-and-Route of All Versal™ Devices

- Automatic partition-based placement and parallel PAR
- Reduces computation and improves readability for fast design closure
- Default flow for all versa devices

Enabling Top-Level RTL Flows for Versal Devices

- Configures key components like HSC and transceivers from top-level RTL
- Enables programmable logic developers to stay in a RTL-centric design environment

Segmented Configuration for Fast Boot of Versal Processing Subsystems (FPS)

- PSoC boots first, deferring configuration of programmable logic (PL)
- Enables fast bringup of CDS with COD
- Maintains diverse boot sequence requirements

Break-of-Use Features

- New real-time preset for Microblaze™ V
- In-line HDL utility IP allows faster IP load and configuration
- Enhanced DFX Resource visualization & DFX summary report
- New utility for PCI-bridge diagnosis and analyze board configuration errors
- Cloud enhancements for Vivado Design Automation

We strongly recommend to use the web installers as it reduces download time and saves significant disk space.

Please see [Important Information](#) for details.

Note:

- Download verification is only supported with Google Chrome and Microsoft Edge web browsers.
- Vivado ML 2021.1 and later versions require upgrading your license server tools to the Flex 11.17.2.5 version.

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.2 Windows Self-Extracting Web Installer (EXE - 333 MB)
MD5 SUM Value: A4ee3f1d6bfef0f36a75e7a780

Download Verification

[Digests](#) [Signature](#) [Public Key](#)

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.2 Linux Self-Extracting Web Installer (BIN - 303 MB)
MD5 SUM Value: 2659897005abef70773bf105a727ff

Download Verification

[Digests](#) [Signature](#) [Public Key](#)

AMD Unified Installer for FPGAs & Adaptive SoCs 2024.2 ZIP (7ZAR) (ZIP - 104.81 GB)
MD5 SUM Value: 8a211475b5980805021502a004446

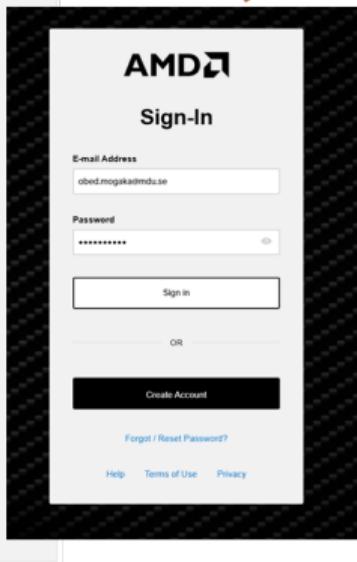
Download Verification

[Digests](#) [Signature](#) [Public Key](#)

AMD Vivado™ Design Suite

2024.2 release now available including major enhancements for designing with AMD Versal™ adaptive SoCs.

[Download Now](#) [Versal Features](#)



You will be required to sign in to your AMD Account. If you don't have, create one.

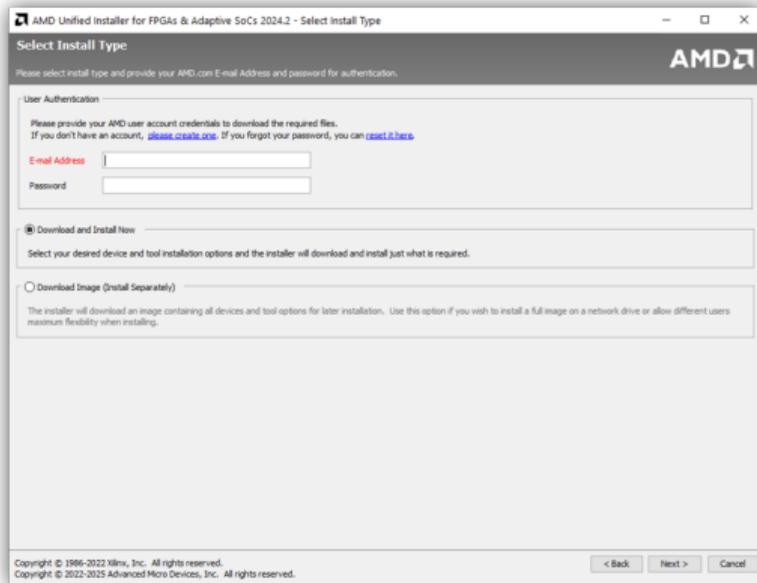
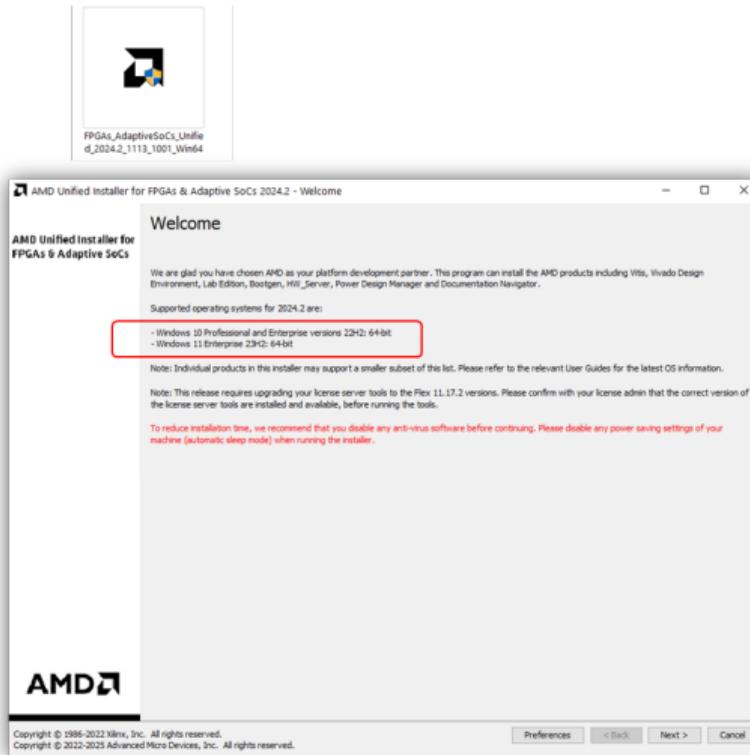
Filename:
FPGAs_AdaptiveSoCs_Unified_2024.2_1113_1001_Win64.exe

If you are downloading the Vivado / Vitis unified installer, you will receive a follow-up confirmation email with a notice regarding our Developer Program.

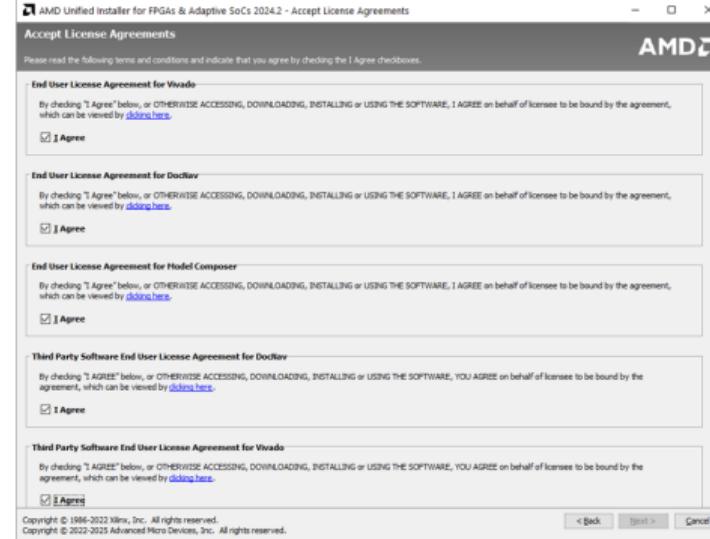
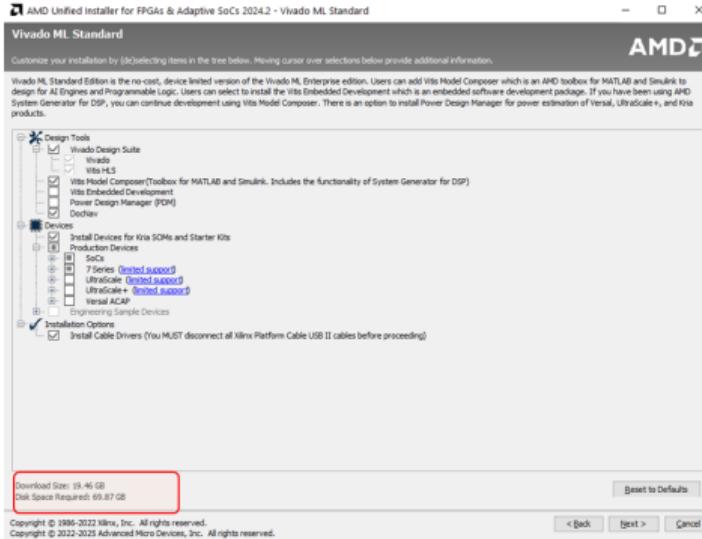
You can read about how we handle your personal data, your personal data rights, and how you can contact us in our [privacy notice](#).

[Download](#)

Step 2: Run the .exe file on windows

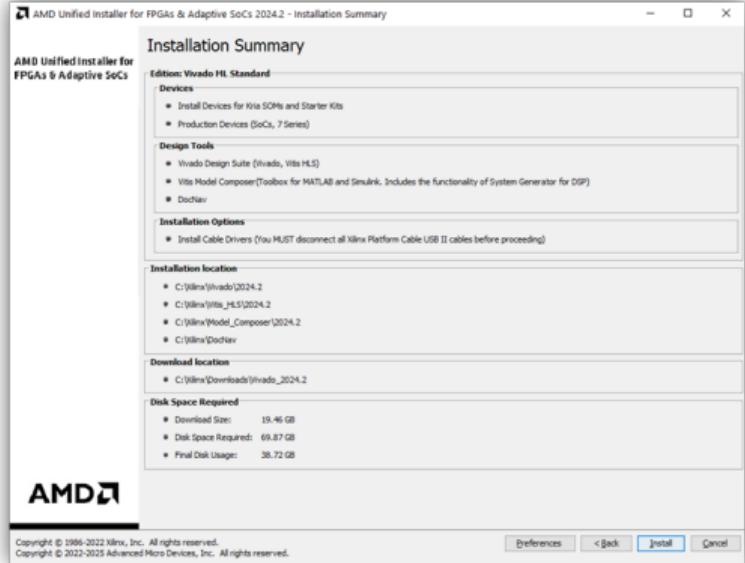
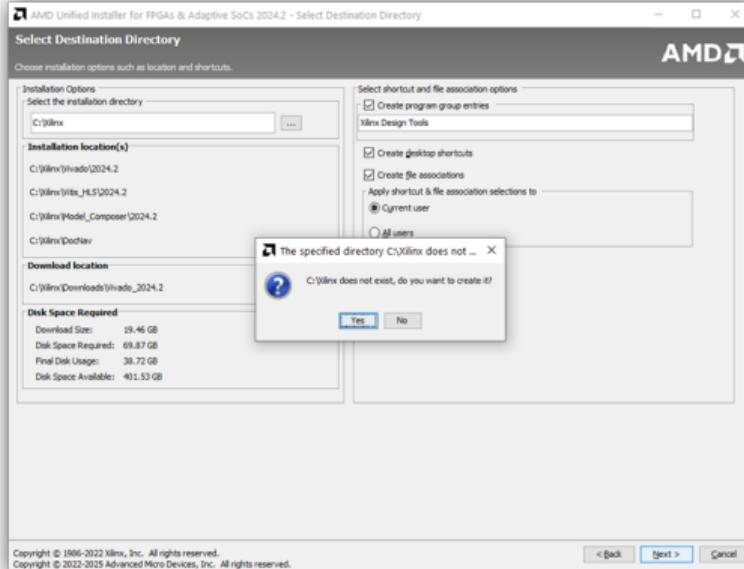


Step 3-4: Select Devices and Accept License Agreements

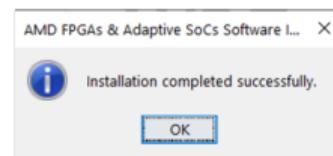
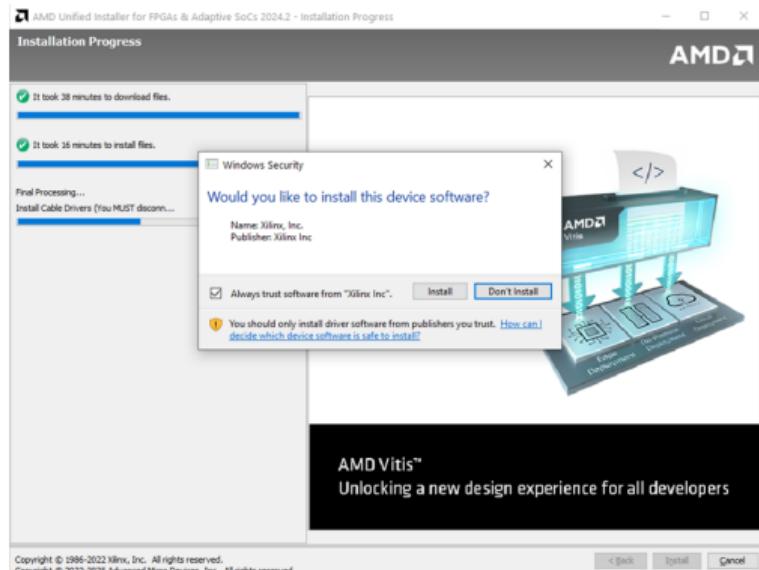
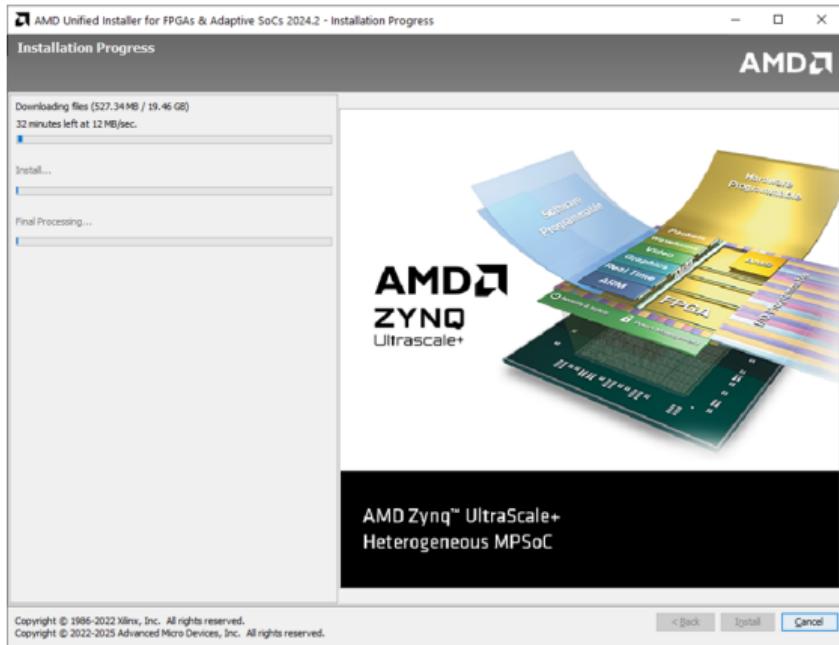


Note: Selecting only the target devices saves on storage significantly!!

Step 5: Set Installation Directory



Installation Progress

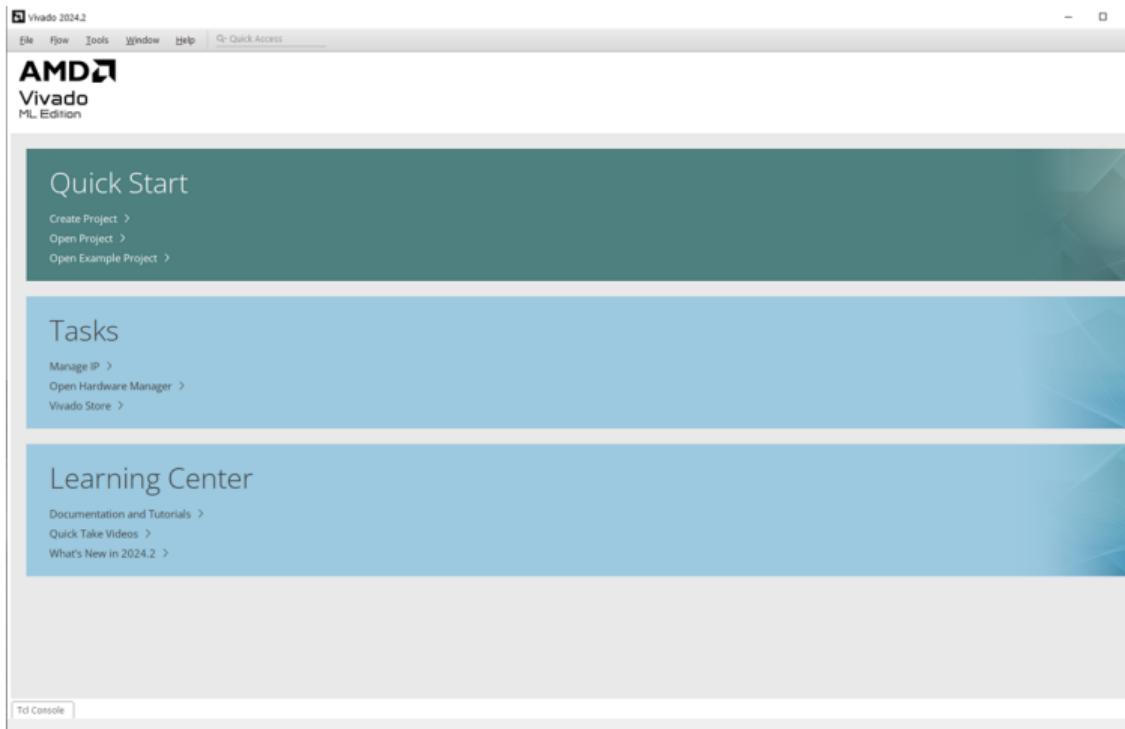


Using Vivado: Quick Introduction

Navigation, Simulation, and Basic Flow

Using Vivado (Start Page)

The Vivado start page, where you can quickly create/open projects and access recent tasks and learning resources.



Documentation and Tutorials

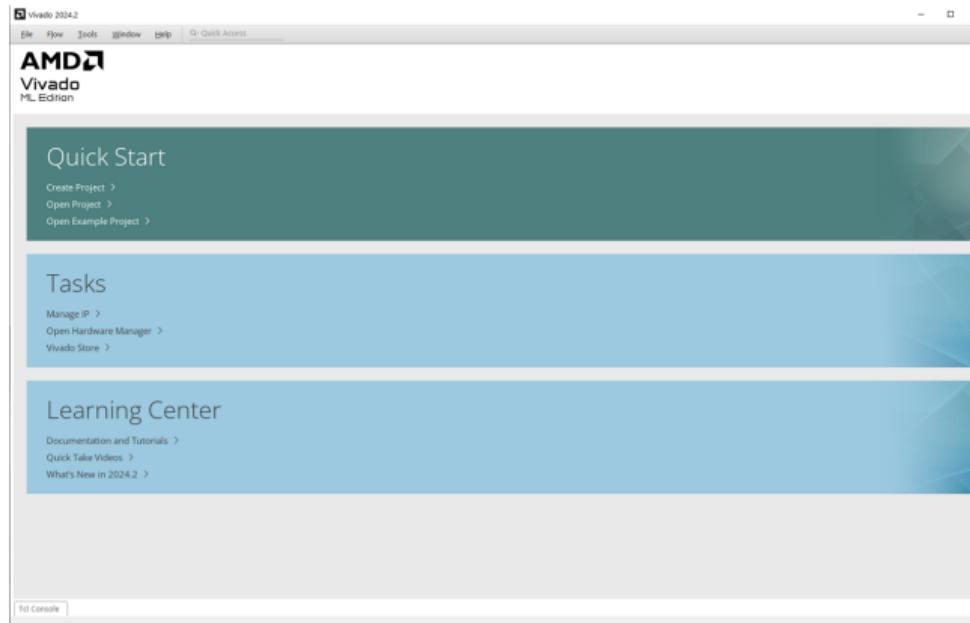
The built-in documentation/tutorial browser is used to find official guides, reference manuals, and example workflows.

The screenshot shows the AMD Adaptive Computing Documentation Navigator interface. The title bar reads "AMD Adaptive Computing Documentation Navigator 2024.2 - Catalog View". The main area is titled "Catalog 2024.12.19 Up to Date" and displays "Xilinx Design Tools 2024.2/14.7" and "Vivado Docs". A toolbar at the top includes icons for search, refresh, and various document types. On the left, a "Document Filters" sidebar lists categories like Product Types (Silicon Devices, Accelerator Cards, System-on-Chips, Design Tools, ISE Design Suite, IP, Design Processes), Silicon Devices (Versal, Zynq UltraScale+, UltraScale & UltraScale+, Zynq 7000, 7 Series, Virtex 6, Virtex 5, Spartan 6, CoreRunner), Accelerator Cards (Alveo Cards, Varium Cards, Telco Cards), System-on-Chips (Kria), Design Tools (Vitis, Vitis AI 3.5, Model Composer, Petalinux, Vivado), ISE Design Suite (ChipScope, EDK and SDK, ISE, PlanAhead, System Generator, IP), and Design Processes (AI Engine Development, Board System Design, Embedded Software Development, Hardware - IP - Platform Dev...). The main pane displays a list of 212 documents under "Vivado: Design Hubs" and "Vivado: Methodology Guides". Each entry includes a thumbnail, title, ID, size (MB), published date, and status. The "Vivado: Design Hubs" section contains documents such as System-Level Design Flow (DH267), Design Flows Overview (DH220), Implementation (DH229), Logic Synthesis (DH228), Dynamic Function eXchange (DH230), Installation and Licensing (DH233), Programming and Debug (DH232), Logic Simulation (DH227), Using IP Integrator (DH224), Power Estimation and Optimization (DH226), I/O and Clock Planning (DH221), Timing Closure and Design Analysis (DH231), Applying Design Constraints (DH225), and Designing with IP (DH223). The "Vivado: Methodology Guides" section contains documents like Ultrafast Design Methodology: Timing Closure Guide (UG1292), ISE to Vivado Design Suite Migration Guide (UG911), Ultrafast Design Methodology Guide for FPGAs and SoCs (UG949), Vivado: Release Notes (UG973), Vivado Design Suite User Guide: Release Notes, In... (UG973), Vivado: Reference Guides (UG984, UG985, UG991, UG992, UG995), and Vivado: Tutorial with Labs (UG945, UG996, UG997, UG998, UG999, UG996).

Document	ID	Size (MB)	Status
System-Level Design Flow (DH267)	DH267	~	Current
Design Flows Overview (DH220)	DH220	~	Current
Implementation (DH229)	DH229	~	Current
Logic Synthesis (DH228)	DH228	~	Current
Dynamic Function eXchange (DH230)	DH230	~	Current
Installation and Licensing (DH233)	DH233	~	Current
Programming and Debug (DH232)	DH232	~	Current
Logic Simulation (DH227)	DH227	~	Current
Using IP Integrator (DH224)	DH224	~	Current
Power Estimation and Optimization (DH226)	DH226	~	Current
I/O and Clock Planning (DH221)	DH221	~	Current
Timing Closure and Design Analysis (DH231)	DH231	~	Current
Applying Design Constraints (DH225)	DH225	~	Current
Designing with IP (DH223)	DH223	~	Current
Vivado: Methodology Guides			
Ultrafast Design Methodology: Timing Closure Guide (UG1292)	UG1292	~	Current
ISE to Vivado Design Suite Migration Guide (UG911)	UG911	~	Current
Ultrafast Design Methodology Guide for FPGAs and SoCs (UG949)	UG949	~	Current
Vivado: Release Notes			
Vivado Design Suite User Guide: Release Notes, In... (UG973)	UG973	~	Current
Vivado: Reference Guides			
MicroBlaze Processor Reference Guide (UG994)	UG994	~	Current
Vivado Design Suite Tcl Command Reference Guide (UG985)	UG985	~	Current
Vivado Design Suite Properties Reference Guide (UG991)	UG991	~	Current
Vivado Design Suite Quick Reference Guide (UG975)	UG975	~	Current
Vivado: Tutorial with Labs			
Vivado Design Suite Tutorial: Using Constraints (UG945)	UG945	~	Current
Vivado Design Suite Tutorial: Implementation (UG996)	UG996	~	Current
Vivado Design Suite Tutorial: Power Analysis and ... (UG997)	UG997	~	Current
Vivado Design Suite Tutorial: Programming and O... (UG998)	UG998	~	Current
Vivado Design Suite Tutorial: Using Constraints (UG999)	UG999	~	Current
Vivado Design Suite Tutorial: Using Constraints (UG996)	UG996	~	Current

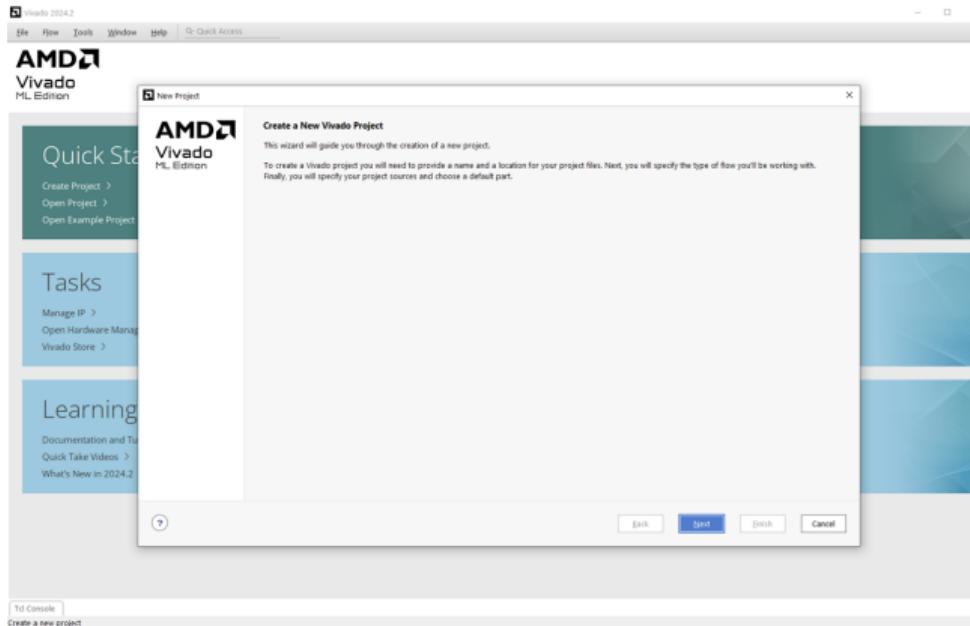
Creating Project (Menu Entry)

Starting a new project from the top menu (**Project** → **New**), launches the New Project wizard.



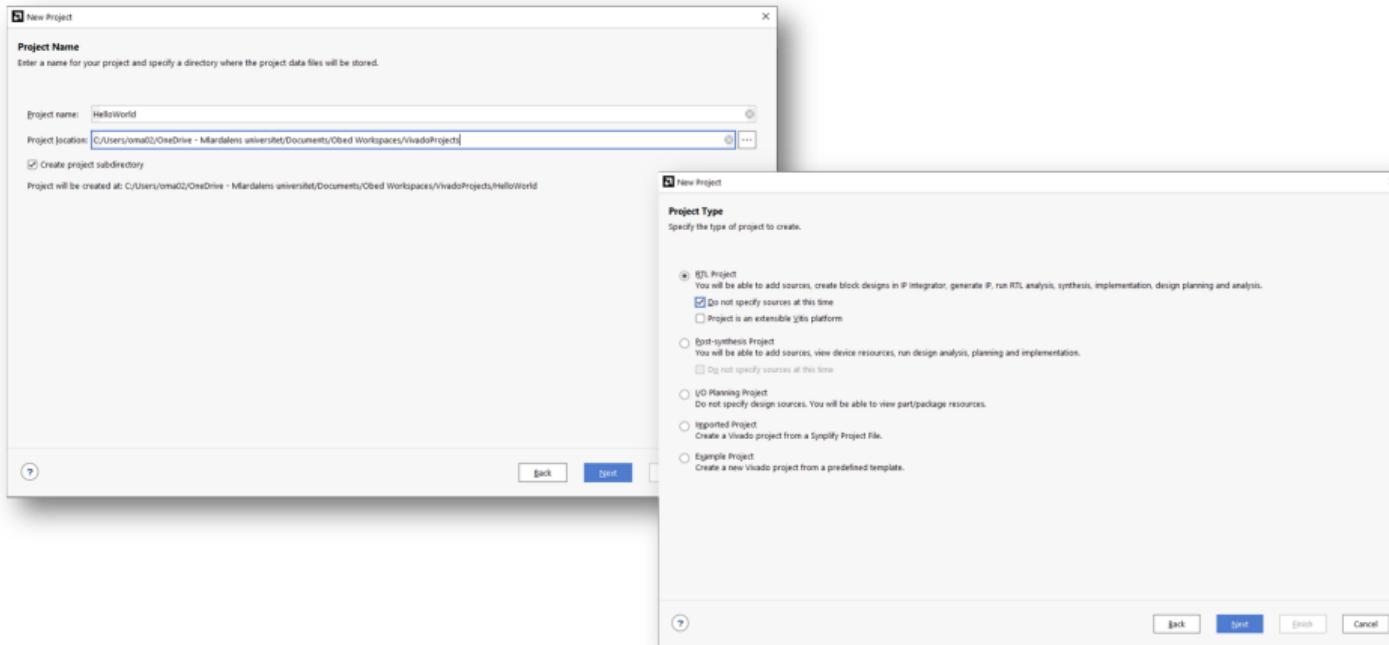
Creating Project (Wizard Start)

The New Project wizard welcome screen; proceed through the wizard to define the project configuration.



Creating Project (Name/Directory & Type)

Set the project name and location, then choose the project type (e.g., RTL project) and whether to include sources/-constraints at creation.



Select Device

Select the target FPGA device/board by filtering the part list, then confirm the selection in the project summary before finishing.

New Project

Default Part

Choose a default AMD part or board for your project.

Parts | Boards

Reset All Filters

Category: General Purpose

Family: Arteris?

Package: All Remaining

Speed: All Remaining

Temperature: All Remaining

Static power: All Remaining

Search: xc7a20t (25 matches)

Part	I/O Pin Count	Available IOBs	LUT Elements	Flipsops	Block RAMs	Ultra RAMs	DSPs	BUFOs	Gb Transceivers	GTPED Trans
xc7a20tpg136-3	236	106	20800	41600	50	0	90	32	2	2
xc7a20tpg136-2	236	106	20800	41600	50	0	90	32	2	2
xc7a20tpg136-3L	236	106	20800	41600	50	0	90	32	2	2
xc7a20tpg136-1	236	106	20800	41600	50	0	90	32	2	2
xc7a20tpg134-3	324	210	20800	41600	50	0	90	32	0	0
xc7a20tpg134-2	324	210	20800	41600	50	0	90	32	0	0
xc7a20tpg134-3L	324	210	20800	41600	50	0	90	32	0	0
xc7a20tpg134-1	324	210	20800	41600	50	0	90	32	0	0
xc7a20tpg135-3	325	150	20800	41600	50	0	90	32	4	4
xc7a20tpg135-2	325	150	20800	41600	50	0	90	32	4	4
xc7a20tpg135-3L	325	150	20800	41600	50	0	90	32	4	4

Back Next Finish Cancel

New Project

AMD Vivado ML Edition

New Project Summary

A new RTL project named HelloWorld will be created.

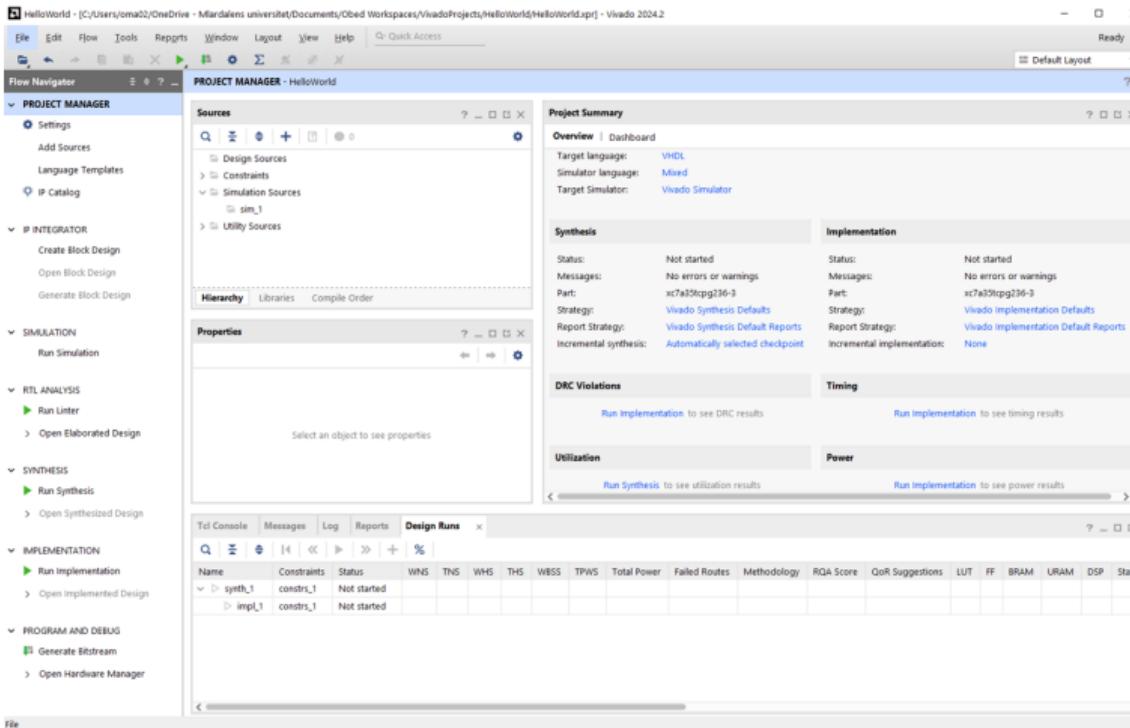
The default part and product family for the new project:
Default Part: xc7a20tpg136-3
Family: Arteris?
Package: cpg136
Speed Grade: -9

To create the project, click Finish.

Back Next Finish Cancel

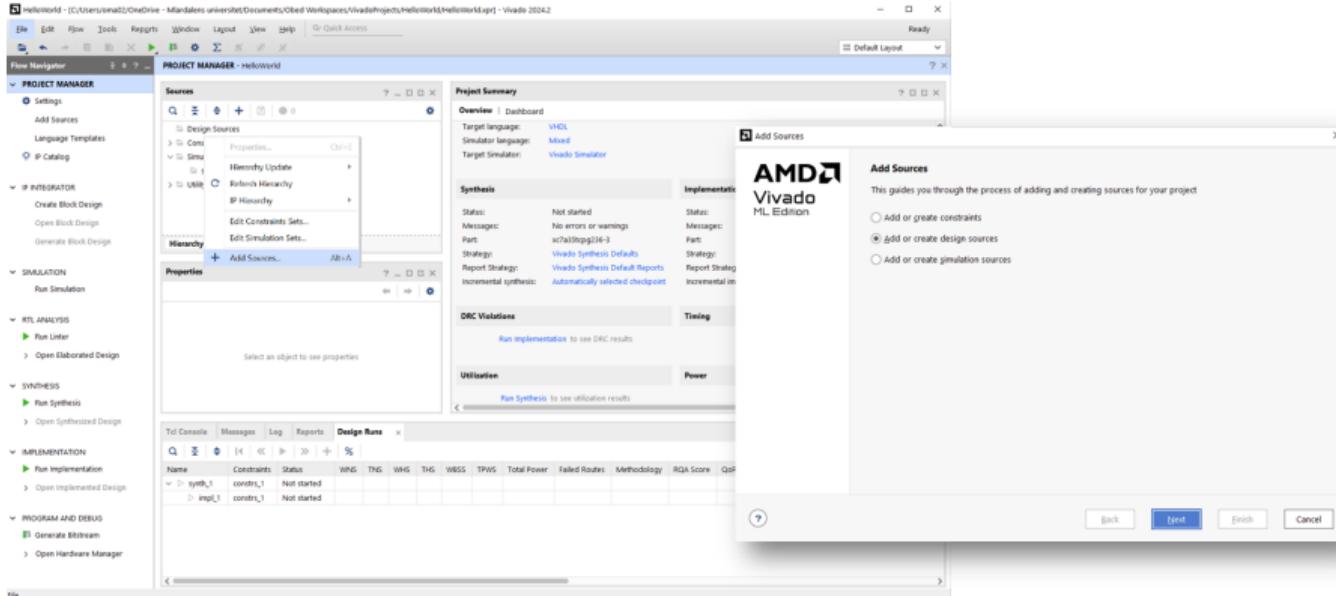
Project Window

The main **Vivado workspace**: Flow Navigator on the left, sources/properties panels, and central views for design, reports, and messages.



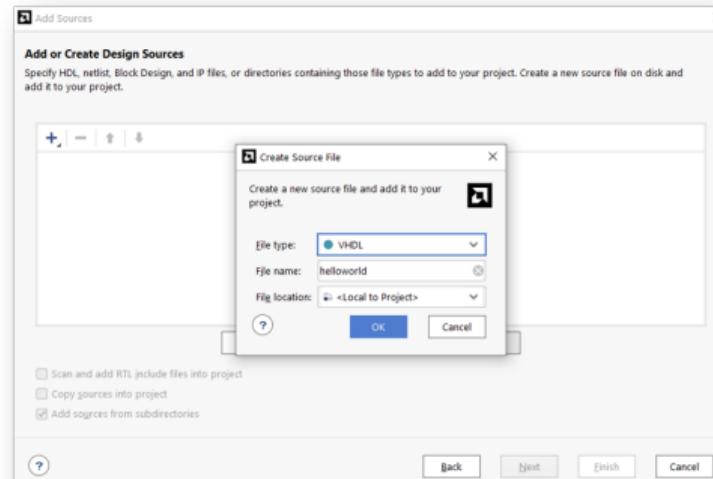
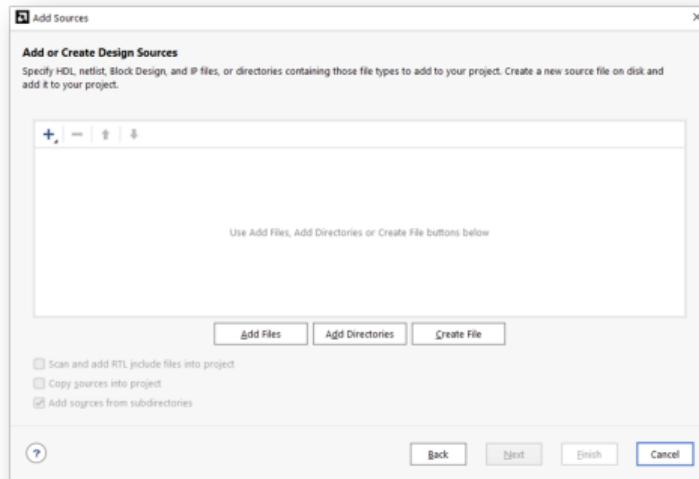
Add Sources (Context Menu)

Right-click **Design Sources** and choose **Add Sources** to bring VHDL/Verilog files, IP, or existing designs into the project.



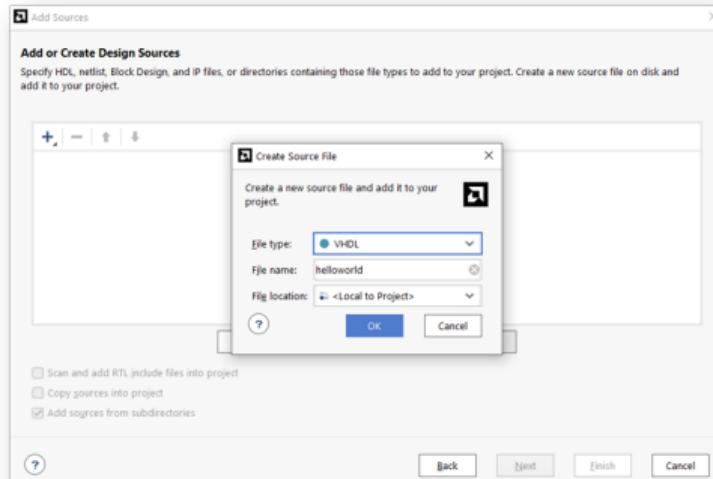
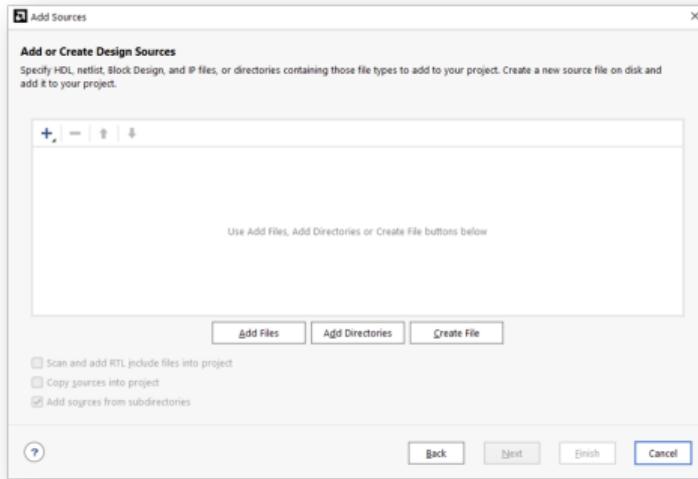
Add Sources (Add/Create Options)

Use the **Add Sources** dialog to either add existing files or create new source files, selecting the appropriate source type and file settings.



Add Sources (Create Module Details)

When creating a new module, specify the module name and define ports (names, directions, and widths), then confirm file creation.



Source Code

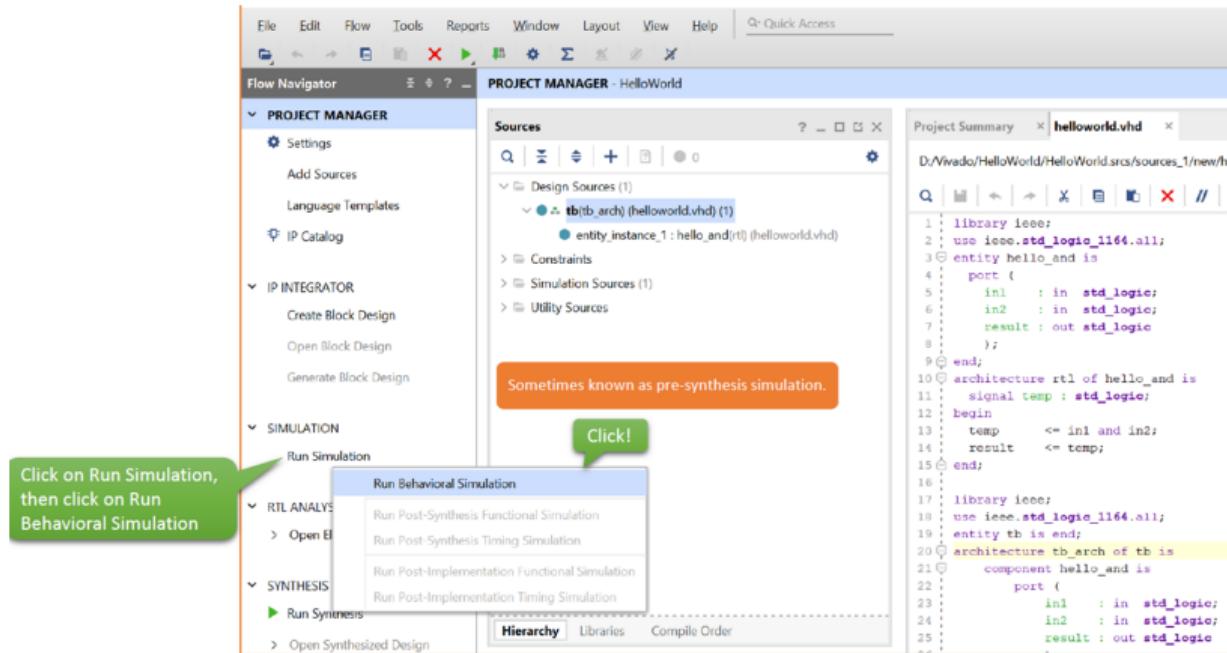
The code editor and source tree; use this view to edit HDL, navigate files, and review source-file properties.

The screenshot shows the Vivado IDE interface with the "Sources" tab selected in the top-left corner. The "Sources" pane displays a tree structure with "Design Sources (1)" containing "helloworld(Behavioral) (helloworld.vhd)". Other sections like "Constraints", "Simulation Sources (1)", and "Utility Sources" are also listed. Below the tree are tabs for "Hierarchy", "Libraries", and "Compile Order". The "Source File Properties" pane shows details for "helloworld.vhd", including its location at "C:/Users/oma02/OneDrive - Mälardalens universitet/Documents/Obed Workspaces/VivadoProjects/HelloWorld>HelloWorld.sr...". The "Type" is set to "VHDL" and the "Library" is "xil_defaultlib". The main workspace is a code editor titled "helloworld.vhd" showing VHDL code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;
entity helloworld is
    -- Port ( );
end helloworld;
architecture Behavioral of helloworld is
begin
end Behavioral;
```

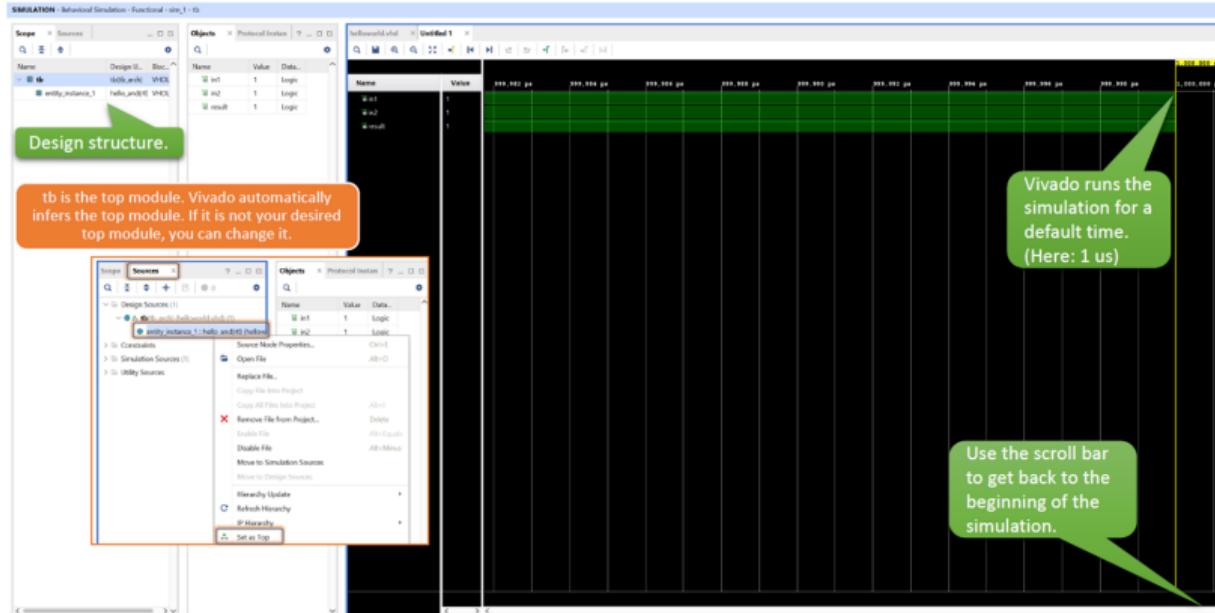
Simulation

Run behavioral simulation from the **Flow Navigator**; if errors appear, fix the HDL and re-run until the simulation launches cleanly.



Set to Top Module

Set the intended design unit as the top module; Vivado simulates the selected top by default, and you can return to the start of simulation via the cursor bar.



Run Simulation

Use simulation controls to restart and run for a specified time; add key outputs/signals to observe behavior during the run.

The screenshot shows the Quartus II software interface with two main windows open:

- SIMULATION - Behavioral Simulation - Functional - sim_1 - tb**: This window contains:
 - A toolbar with icons for Window, Layout, View, Run, Help, and Quick Access.
 - A status bar showing "1 us".
 - Two tabs: Scope and Sources. The Sources tab is selected, showing a table of signals:

Name	Value	Data...
in1	1	Logic
in2	1	Logic
result	1	Logic
 - A tree view of design sources, constraints, simulation sources, and utility sources.
- SIMULATION - Behavioral Simulation - Functional - sim_1 - tb**: This window displays:
 - A Sources tab showing a table of signals:

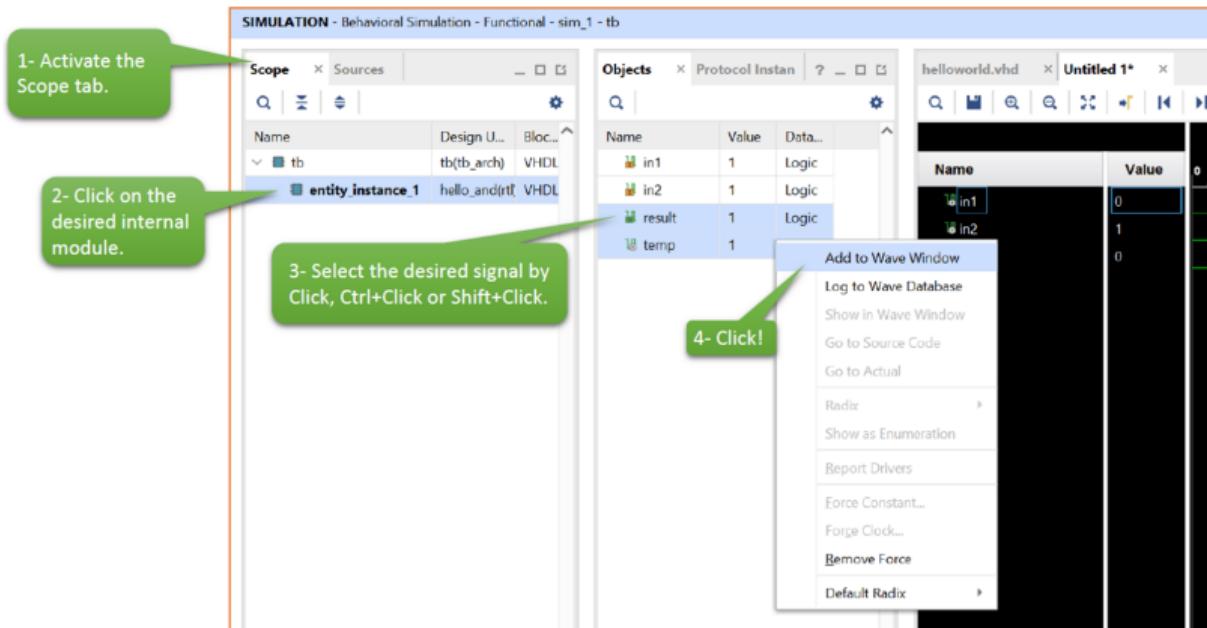
Name	Value	Data...
in1	0	
in2	1	
result	0	/tb/result
 - An Objects tab showing a list of design sources, constraints, simulation sources, and utility sources.
 - A waveform viewer on the right showing the signal "result" over time.

Annotations with green callouts point to specific features:

- A callout points to the "Run" button in the toolbar with the text "Run simulation for a specified time."
- A callout points to the "Restart" button in the toolbar with the text "Restart simulation run."
- A callout points to the "result" signal in the waveform viewer with the text "Note: The default signal list contains signals of the top module."

Adding Internal Signals to Waveform View

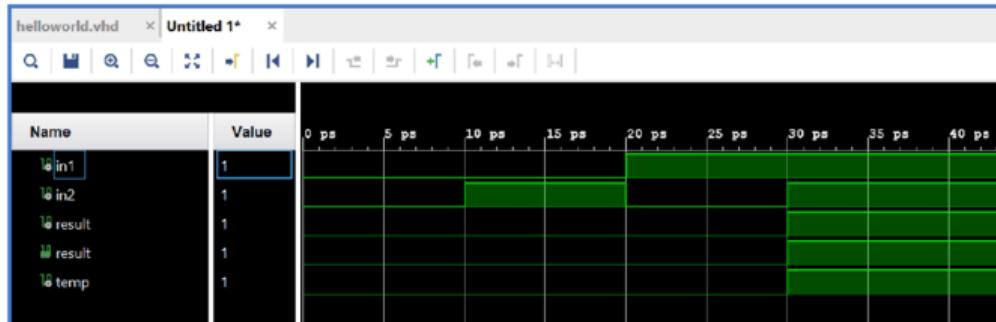
Use the Scope tab to find internal instances/signals, then add selected signals to the waveform window via right-click.



Inspect Waveforms

Correlate stimulus/process code and DUT logic with waveform transitions to validate timing and functional correctness.

```
process is
begin
    in1 <= '0';
    in2 <= '0';
    wait for 10 ps;
    in1 <= '0';
    in2 <= '1';
    wait for 10 ps;
    in1 <= '1';
    in2 <= '0';
    wait for 10 ps;
    in1 <= '1';
    in2 <= '1';
    wait;
end process;
```

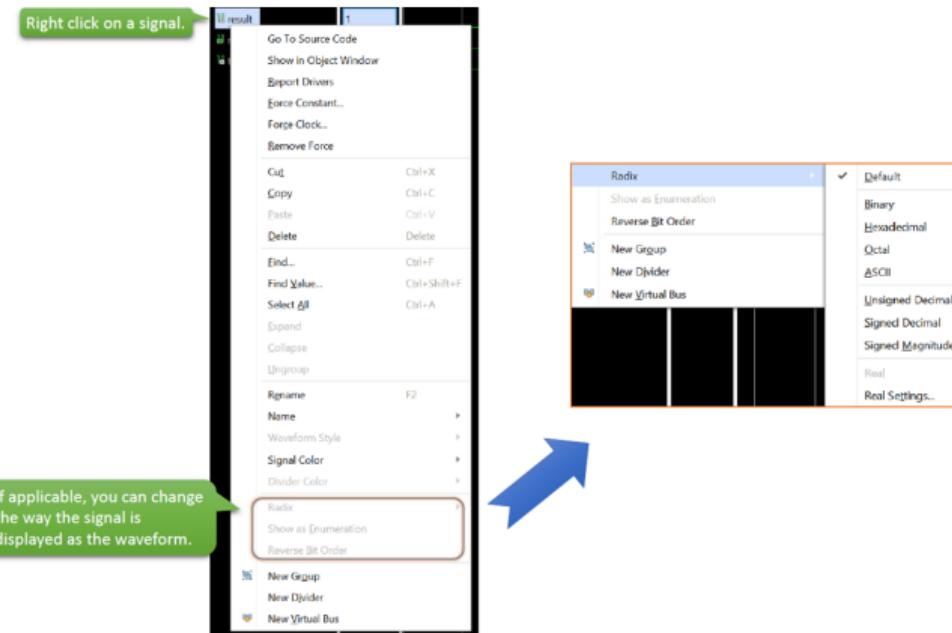


```
entity_instance_1: hello_and
    port map(in1, in2, result);
```

```
architecture rtl of hello_and is
    signal temp : std_logic;
begin
    temp      <= in1 and in2;
    result    <= temp;
end;
```

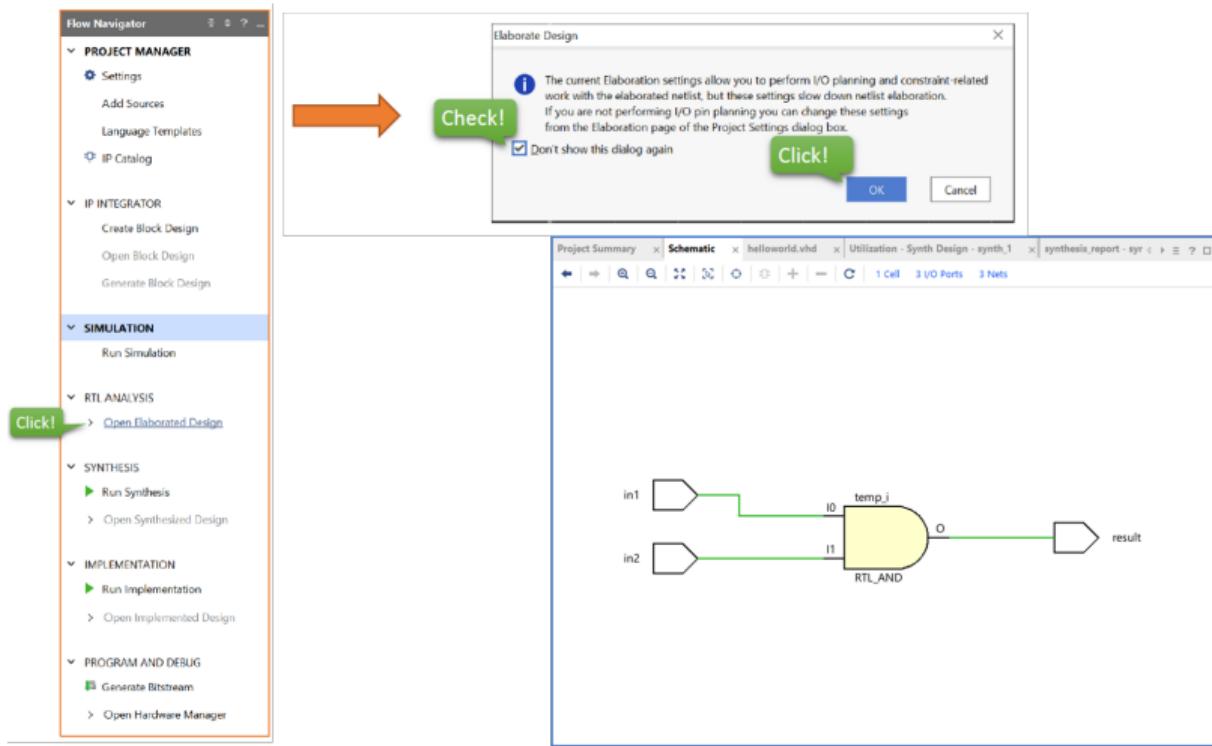
Other Useful Features

Right-click waveform signals to access utilities such as radix changes, grouping, naming, and display options to improve readability.



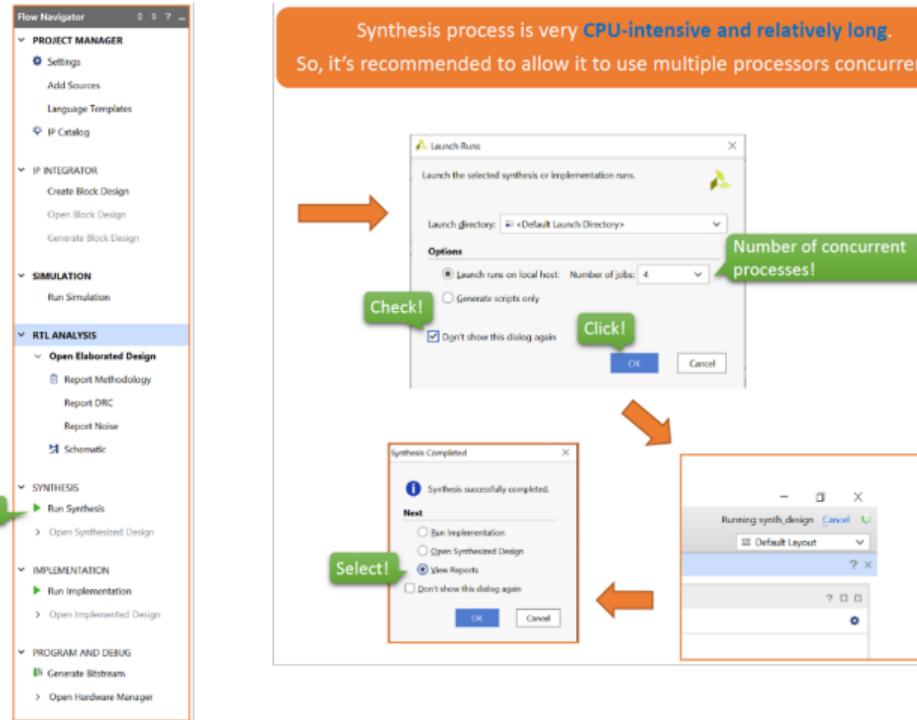
RTL Analysis (Elaboration)

Run RTL elaboration to visualize the design structure and catch connectivity/structural issues before synthesis.



Synthesis (Launching & Settings)

Launch synthesis from the Flow Navigator; optionally increase the number of concurrent processes to speed up CPU-intensive runs.



Synthesis (Report Interpretation)

Review synthesis reports for resource utilization (LUTs, FFs, BRAM, etc.) and verify that the expected design blocks are accounted for.

The screenshot shows the Vivado IDE interface. On the left, the Flow Navigator pane is open, showing various project management and synthesis-related options. A green callout bubble labeled "Click!" points to the "Report Utilization" option under the "SYNTHESIS" section. On the right, a "Utilization - Synth Design - synth_1" report window is displayed. The report content includes sections like "Design", "Utilization Design Information", and "Table of Contents". A specific table for "Site Type" usage is highlighted with red boxes around its header and body. Below this table, a green callout bubble states: "As expected, three IOs are used." An orange arrow points from the text to the table's body. The table data is as follows:

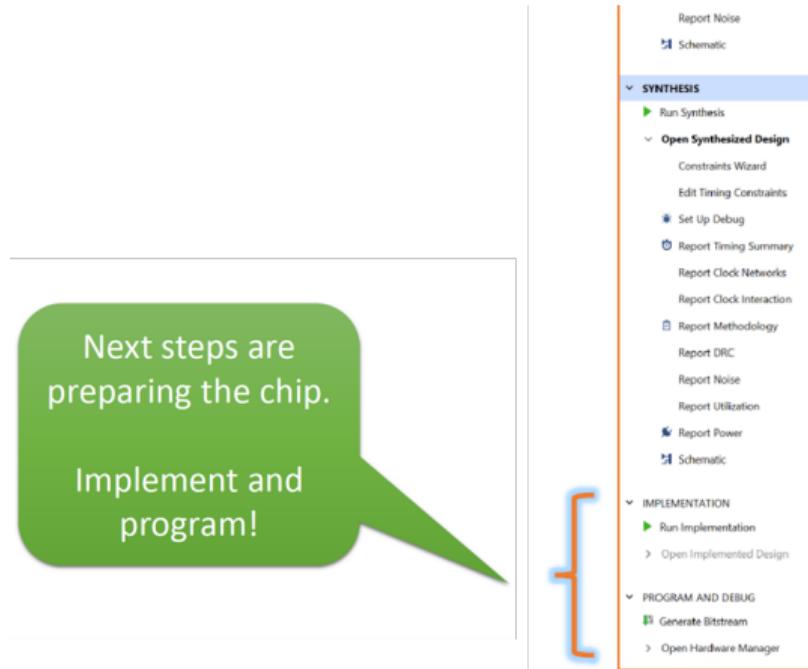
Site Type	Used	Fixed	Prohibited	Available	Units
I Slice LUT*	0	0	0	20800	<0.01
I LUT as Logic	0	0	0	20800	<0.01
I LUT as Memory	0	0	0	9400	0.00
I Slice Registers	0	0	0	41400	0.00
I Register as Flip Flop	0	0	0	41400	0.00
I Register as Latch	0	0	0	41400	0.00
I FT Muxes	0	0	0	14300	0.00

Below the table, another section titled "4. IO and GT Specific" is shown, which contains a table with one row:

Site Type	Used
Bonded IOB	3

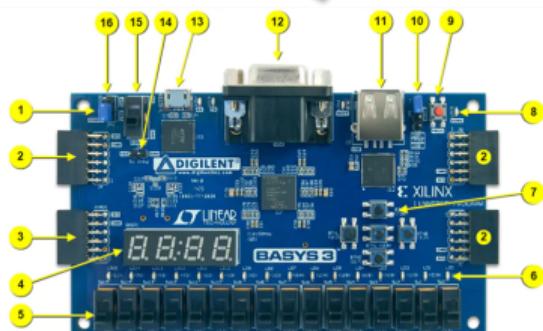
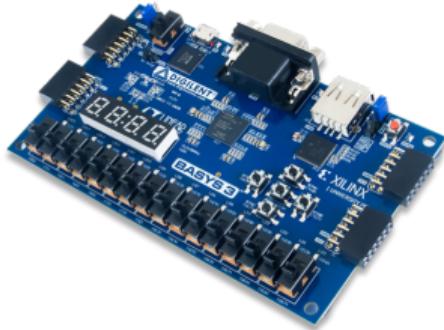
Implementation

The implementation stage (place-and-route), where the synthesized netlist is mapped and routed to meet timing and device constraints.



The Basys 3 FPGA Board

In this course, we use the Basys 3 development board.



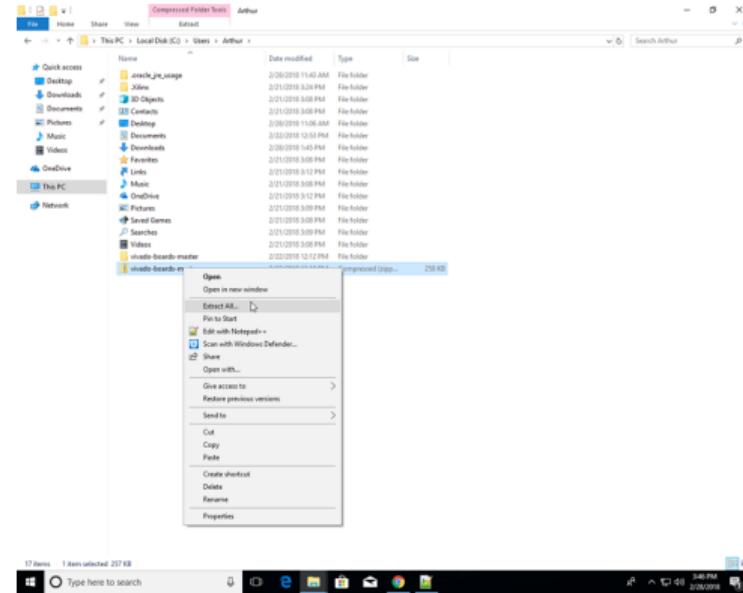
- The Basys 3 board is a complete, ready-to-use digital circuit development platform based on the Artix®-7 Field Programmable Gate Array (FPGA) from Xilinx®
- Features the Xilinx Artix®-7 FPGA (XC7A35T-ICPG236C)
- Artix-7 35T features include:
 - 33,280 logic cells in 5200 slices
 - 1800 Kbits of fast block RAM
 - Internal clock speeds exceeding 450MHz
- Other collection of ports and peripherals

Callout	Component Description	Callout	Component Description
1	Power good LED	9	FPGA configuration reset button
2	Pmod port(s)	10	Programming mode jumper
3	Analog signal Pmod port (XADC)	11	USB host connector
4	Four digit 7-segment display	12	VGA connector
5	Slide switches (16)	13	Shared UART/ JTAG USB port
6	LEDs (16)	14	External power connector
7	Pushbuttons (5)	15	Power Switch
8	FPGA programming done LED	16	Power Select Jumper

Install Digilent's Board Files

- **Digilent** provides board files for each FPGA development board. These files make it easy to select the correct part when creating a new project and allow for automated configuration of several complicated components (including the Zynq Processing System and Memory Interface Generator) used in many designs.
- The board files will be copied into your version of Vivado's installation directory.
- Download the most recent Master Branch ZIP Archive^a of Digilent's vivado-boards Github repository and extract it

^a<https://github.com/Digilent/vivado-boards/archive/master.zip>



Install Digilent's Board Files

- Open the folder extracted from the archive and navigate to its `new/board_files` folder. You will be copying all of this folder's subfolders.
- Open the folder that Vivado was installed into -
`C:/Xilinx/Vivado` or
`/opt/Xilinx/Vivado` by default. Under this folder, navigate to its
`<version>/data/boards/board_files` directory. If this folder doesn't exist, create it.
- Copy all of the folders found in vivado-boards' `new/board_files` folder, then paste them into this folder

(C:) > Xilinx > Vivado > 2024.2 > data > boards > board_files			
Name	Date modified	Type	Size
arty	1/14/2025 2:50 PM	File folder	
arty-a7-35	1/14/2025 2:50 PM	File folder	
arty-a7-100	1/14/2025 2:50 PM	File folder	
arty-s7-25	1/14/2025 2:50 PM	File folder	
arty-s7-50	1/14/2025 2:50 PM	File folder	
arty-z7-10	1/14/2025 2:50 PM	File folder	
arty-z7-20	1/14/2025 2:50 PM	File folder	
basys3	1/14/2025 2:50 PM	File folder	
cmod_a7-15t	1/14/2025 2:50 PM	File folder	
cmod_a7-35t	1/14/2025 2:50 PM	File folder	
cmod_s7-25	1/14/2025 2:50 PM	File folder	
cora-z7-07s	1/14/2025 2:50 PM	File folder	
cora-z7-10	1/14/2025 2:50 PM	File folder	
eclipse-z7	1/14/2025 2:50 PM	File folder	
genesys2	1/14/2025 2:50 PM	File folder	
genesys-zu-3eg	1/14/2025 2:50 PM	File folder	
genesys-zu-5ev	1/14/2025 2:50 PM	File folder	
nexys_video	1/14/2025 2:50 PM	File folder	
nexys4	1/14/2025 2:50 PM	File folder	
nexys4_ddr	1/14/2025 2:50 PM	File folder	
nexys-a7-50t	1/14/2025 2:50 PM	File folder	
nexys-a7-100t	1/14/2025 2:50 PM	File folder	
sword	1/14/2025 2:50 PM	File folder	
usb104-a7	1/14/2025 2:50 PM	File folder	
zerohzard	1/14/2025 2:50 PM	File folder	

Happy Design!!