Booth Multiplier

Report of CA1

School of Electrical and Computer Engineering

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Contents

Booth Algorithm

Booth Algorithm Diagram shown in Figure 1.

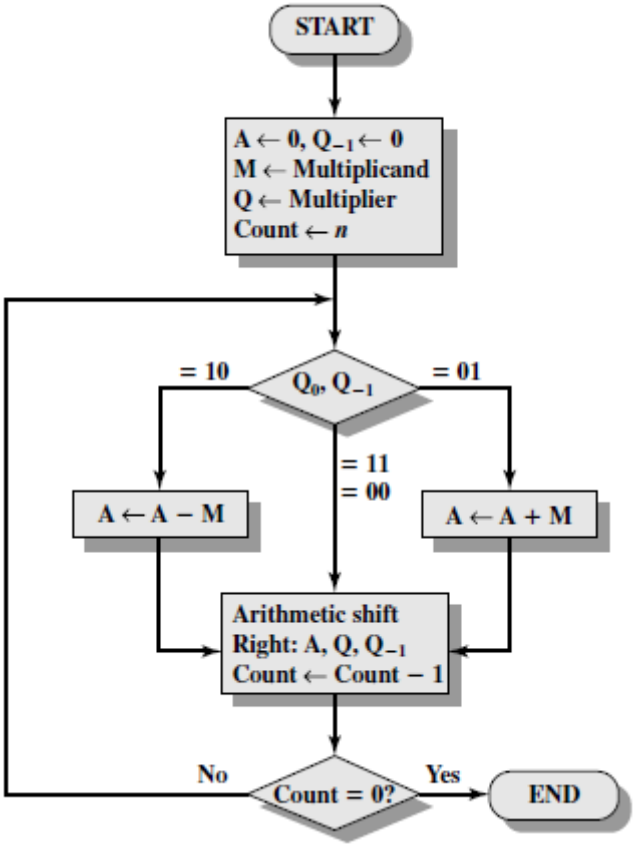

Figure 1 Booth Algorithm

Controller Design

State Machine

The state Machine of our controller can be seen in Figure 2 (based on Booth Algorithm shown in Figure 1)

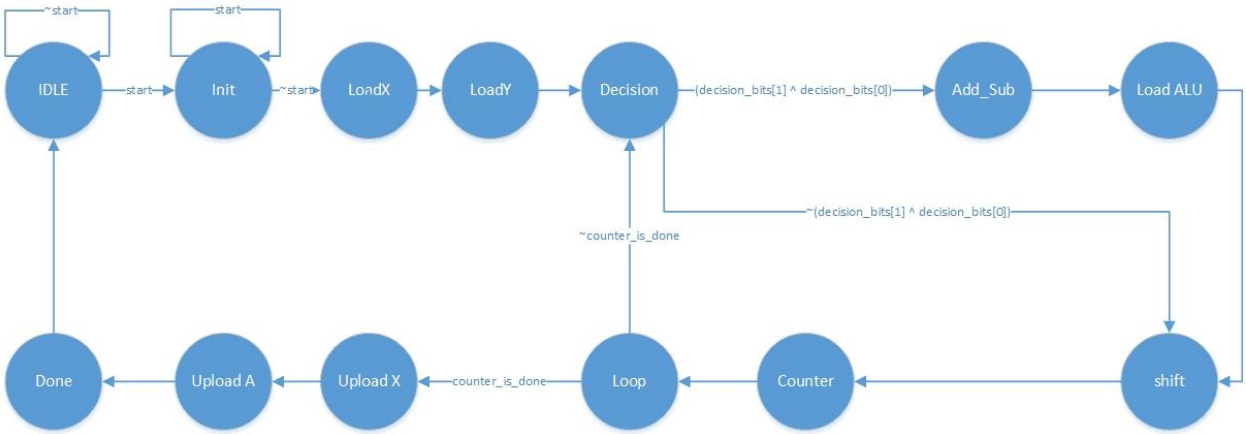

Figure 2: State Machine of Controller

And All of Controller Signals Shown in Figure 3 and also we show that what happens to these signals in each state

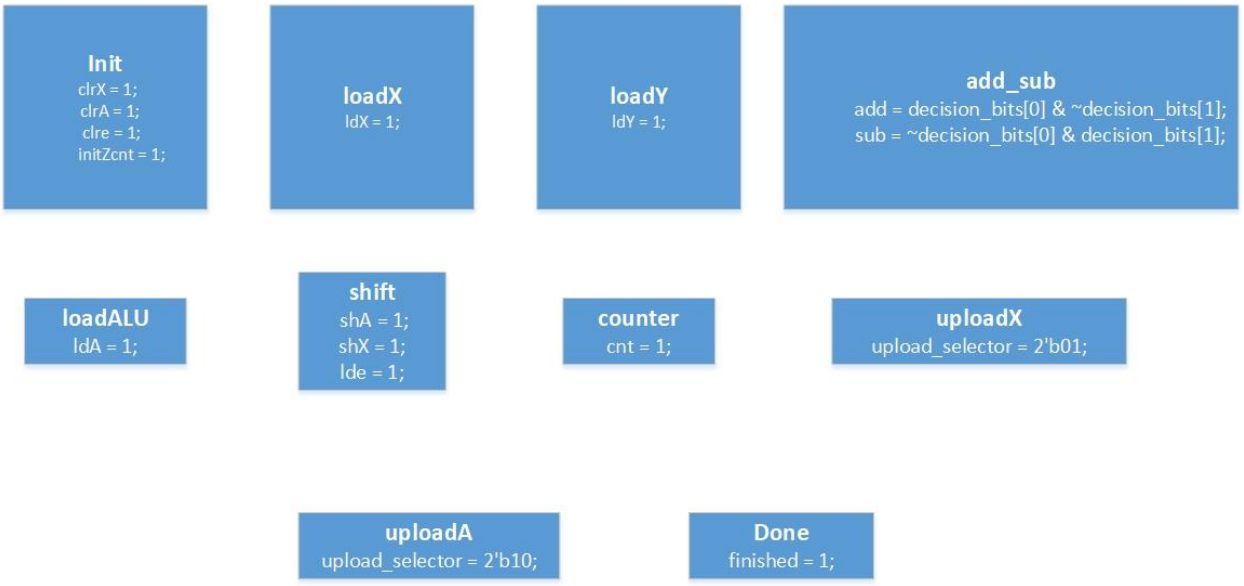

Figure 3: Controller Signals

Counter

A Counter has been added to this controller to control the loop state and finish the procedure in right time. Because the Multiplier has 6 bits (n in Figure 1) so based on Booth Algorithm the iteration should be completed 6 time and this counter controls it properly.

Data Path

Circuit

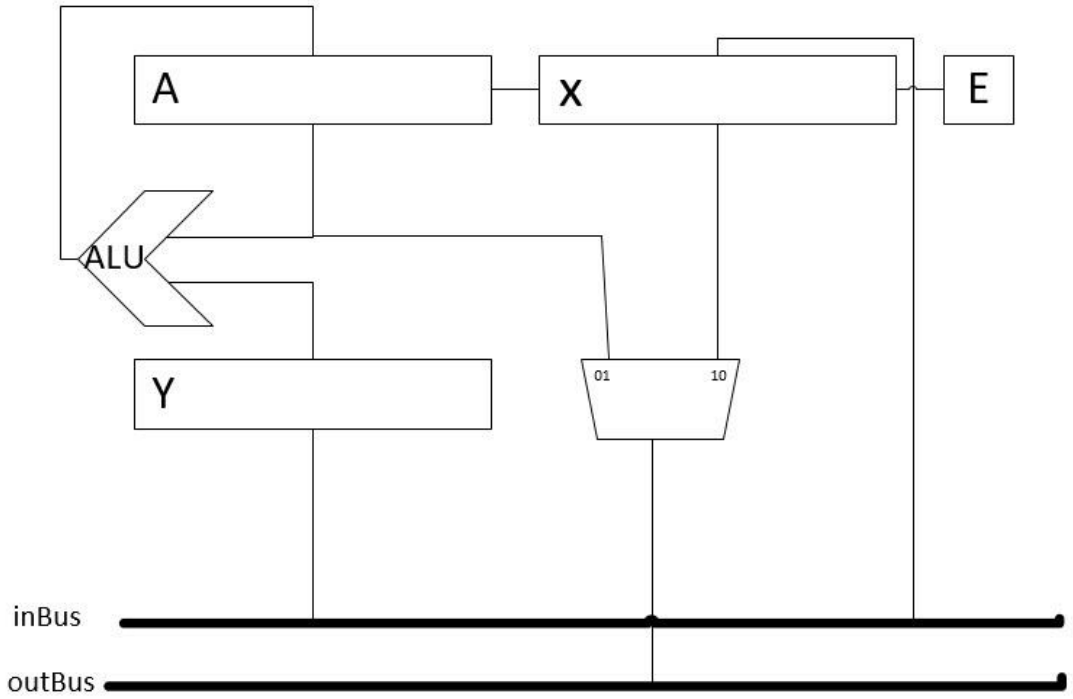

Figure 4 Data path

This data path consist of 5 parts;

ALU

This ALU only add or subtract its operands based on controller signal.

Registers

- 1 bit Register
- 6 bit Register
- 6 bit Register with shifting
- 6 bit Register with shifting and carry-in

Test Bench

Test 1

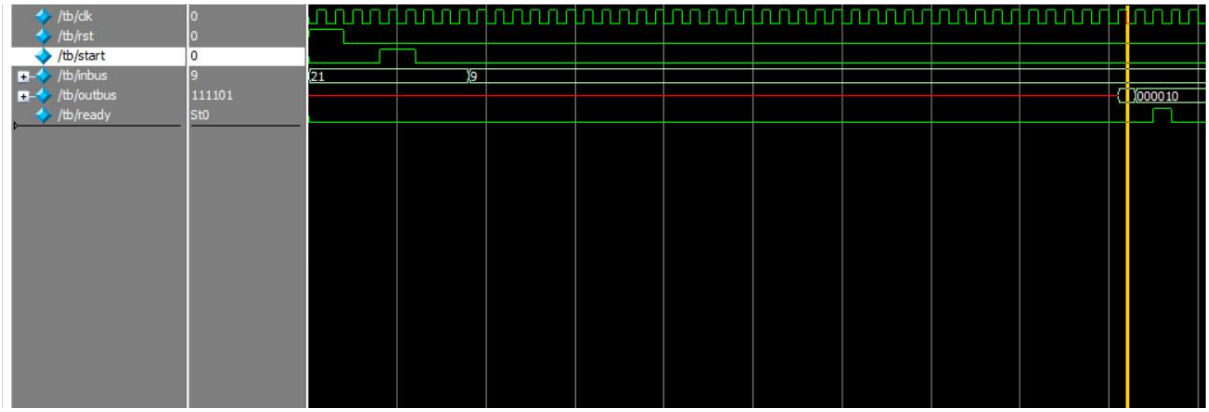

Figure 5 Test 1

21 * 9 = 000010111101

Test 2

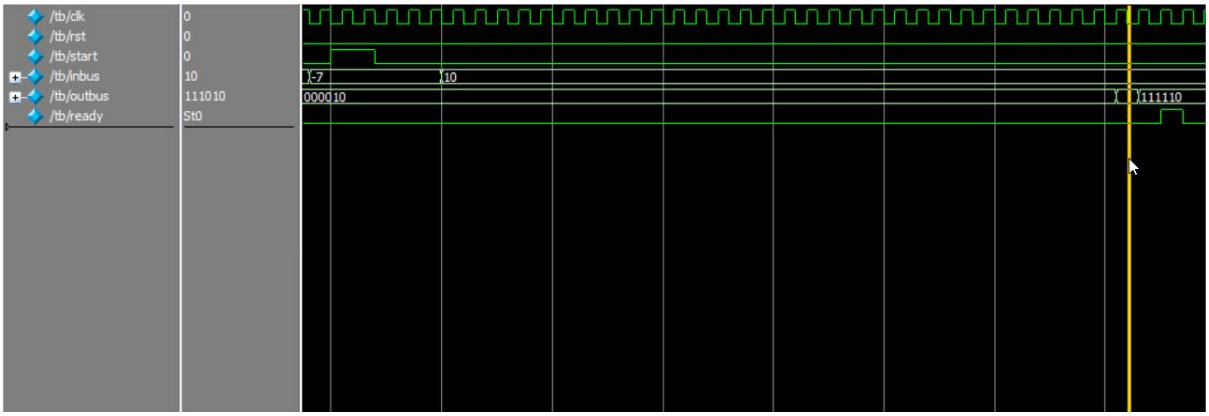

Figure 6 Test 2

-7 * 10 = 111110111010 = -70

Test 3

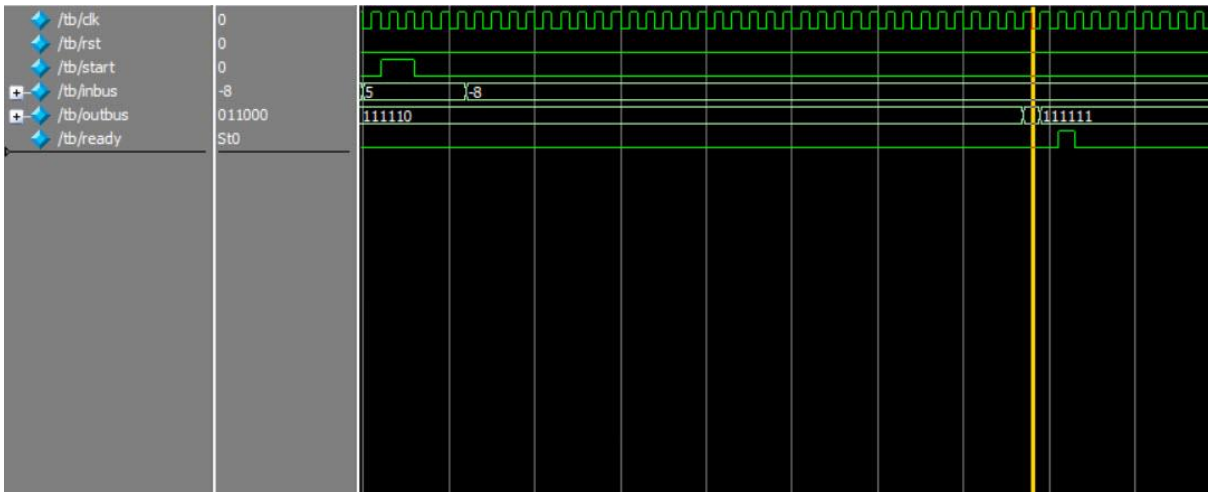

Figure 7 Test 3

5 * -8 = 111111011000 =-40

Test 4

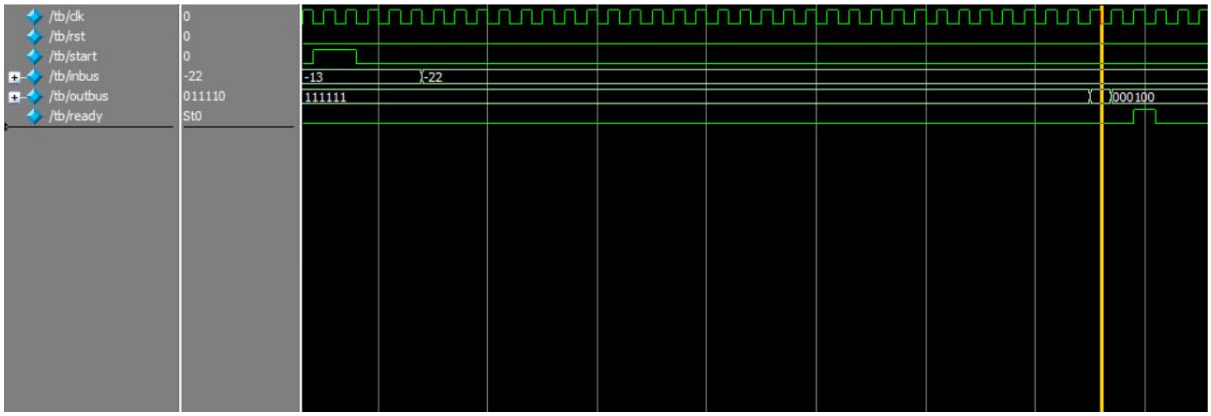

Figure 8 Test 4

-13 * -22 = 000100011110 = 286