Assignment (Implement bgezal)

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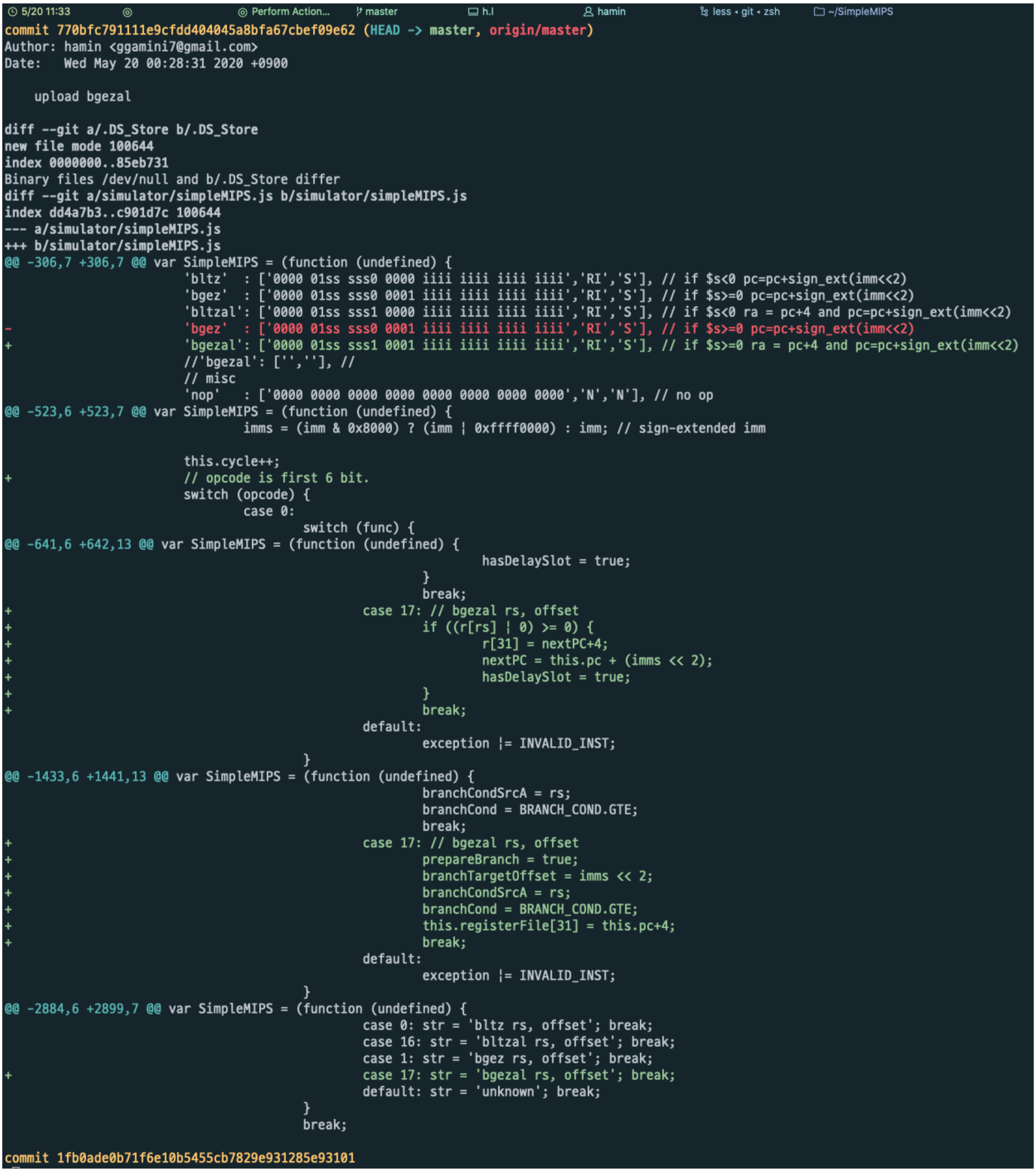
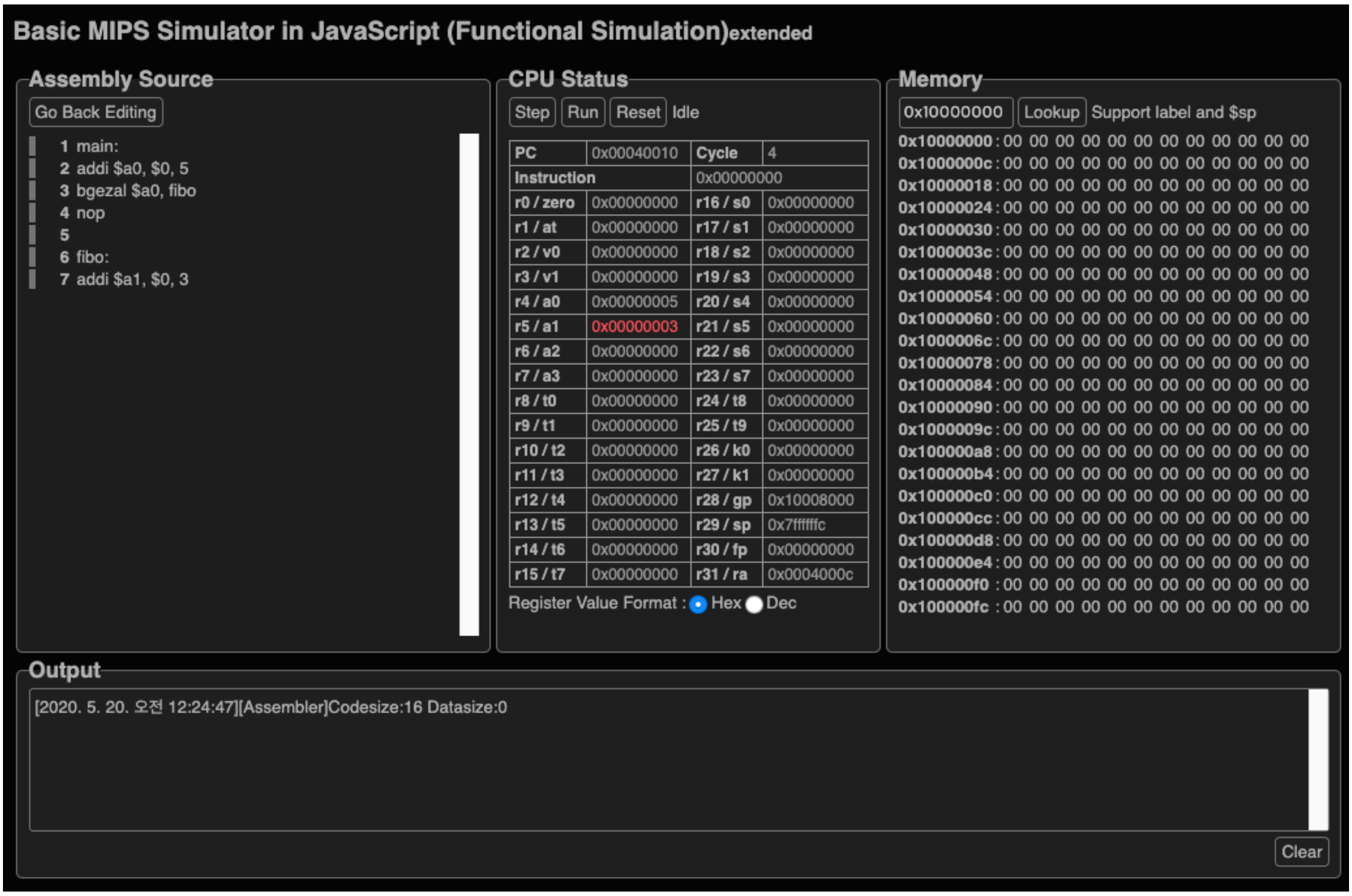
changed parts



```
commit 770bfc791111e9cfdd404045a8bfa67cbef09e62 (HEAD -> master, origin/master)
Author: hamin <ggamini7@gmail.com>
Date:   Wed May 20 00:28:31 2020 +0900

    upload bgezal

diff --git a/.DS_Store b/.DS_Store
new file mode 100644
index 0000000..85eb731
Binary files /dev/null and b/.DS_Store differ
diff --git a/simulator/simpleMIPS.js b/simulator/simpleMIPS.js
index dd4a7b3..c901d7c 100644
--- a/simulator/simpleMIPS.js
+++ b/simulator/simpleMIPS.js
@@ -306,7 +306,7 @@ var SimpleMIPS = (function (undefined) {
                        'bltz'  : ['0000 01ss sss0 0000 iiii iiii iiii iiii','RI','S'], // if $s<0 pc=pc+sign_ext(imm<<2)
                        'bgez'  : ['0000 01ss sss0 0001 iiii iiii iiii iiii','RI','S'], // if $s>=0 pc=pc+sign_ext(imm<<2)
                        'bltzal': ['0000 01ss sss1 0000 iiii iiii iiii iiii','RI','S'], // if $s<0 ra = pc+4 and pc=pc+sign_ext(imm<<2)
-                       'bgez'  : ['0000 01ss sss0 0001 iiii iiii iiii iiii','RI','S'], // if $s>=0 pc=pc+sign_ext(imm<<2)
+                       'bgezal': ['0000 01ss sss1 0001 iiii iiii iiii iiii','RI','S'], // if $s>=0 ra = pc+4 and pc=pc+sign_ext(imm<<2)
                        //'bgezal': ['',''], //
                        // misc
                        'nop'   : ['0000 0000 0000 0000 0000 0000 0000 0000','N','N'], // no op
@@ -523,6 +523,7 @@ var SimpleMIPS = (function (undefined) {
                                imms = (imm & 0x8000) ? (imm | 0xffff0000) : imm; // sign-extended imm

                        this.cycle++;
+                       // opcode is first 6 bit.
                        switch (opcode) {
                                case 0:
                                        switch (func) {
@@ -641,6 +642,13 @@ var SimpleMIPS = (function (undefined) {
                                                                hasDelaySlot = true;
                                                        }
                                                        break;
+                                               case 17: // bgezal rs, offset
+                                                       if ((r[rs] | 0) >= 0) {
+                                                               r[31] = nextPC+4;
+                                                               nextPC = this.pc + (imms << 2);
+                                                               hasDelaySlot = true;
+                                                       }
+                                                       break;
                                                default:
                                                        exception |= INVALID_INST;
                                        }
@@ -1433,6 +1441,13 @@ var SimpleMIPS = (function (undefined) {
                                                        branchCondSrcA = rs;
                                                        branchCond = BRANCH_COND.GTE;
                                                        break;
+                                               case 17: // bgezal rs, offset
+                                                       prepareBranch = true;
+                                                       branchTargetOffset = imms << 2;
+                                                       branchCondSrcA = rs;
+                                                       branchCond = BRANCH_COND.GTE;
+                                                       this.registerFile[31] = this.pc+4;
+                                                       break;
                                                default:
                                                        exception |= INVALID_INST;
                                        }
@@ -2884,6 +2899,7 @@ var SimpleMIPS = (function (undefined) {
                                                case 0: str = 'bltz rs, offset'; break;
                                                case 16: str = 'bltzal rs, offset'; break;
                                                case 1: str = 'bgez rs, offset'; break;
+                                               case 17: str = 'bgezal rs, offset'; break;
                                                default: str = 'unknown'; break;
                                        }
                                        break;

commit 1fb0ade0b71f6e10b5455cb7829e931285e93101
```

example bgezal is used.



```
main:
addi $a0, $0, 5
bgezal $a0, fibo
nop

fibo:
addi $a1, $0, 3
```

PC	0x00040010	Cycle	4
Instruction	0x00000000		
r0 / zero	0x00000000	r16 / s0	0x00000000
r1 / at	0x00000000	r17 / s1	0x00000000
r2 / v0	0x00000000	r18 / s2	0x00000000
r3 / v1	0x00000000	r19 / s3	0x00000000
r4 / a0	0x00000005	r20 / s4	0x00000000
r5 / a1	0x00000003	r21 / s5	0x00000000
r6 / a2	0x00000000	r22 / s6	0x00000000
r7 / a3	0x00000000	r23 / s7	0x00000000
r8 / t0	0x00000000	r24 / t8	0x00000000
r9 / t1	0x00000000	r25 / t9	0x00000000
r10 / t2	0x00000000	r26 / k0	0x00000000
r11 / t3	0x00000000	r27 / k1	0x00000000
r12 / t4	0x00000000	r28 / gp	0x10008000
r13 / t5	0x00000000	r29 / sp	0x7ffffffc
r14 / t6	0x00000000	r30 / fp	0x00000000
r15 / t7	0x00000000	r31 / ra	0x0004000c

Register Value Format : ● Hex ○ Dec

0x10000000

```
0x10000000 : 00 00 00 00 00 00 00 00 00 00 00 00
0x1000000c : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000018 : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000024 : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000030 : 00 00 00 00 00 00 00 00 00 00 00 00
0x1000003c : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000048 : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000054 : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000060 : 00 00 00 00 00 00 00 00 00 00 00 00
0x1000006c : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000078 : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000084 : 00 00 00 00 00 00 00 00 00 00 00 00
0x10000090 : 00 00 00 00 00 00 00 00 00 00 00 00
0x1000009c : 00 00 00 00 00 00 00 00 00 00 00 00
0x100000a8 : 00 00 00 00 00 00 00 00 00 00 00 00
0x100000b4 : 00 00 00 00 00 00 00 00 00 00 00 00
0x100000c0 : 00 00 00 00 00 00 00 00 00 00 00 00
0x100000cc : 00 00 00 00 00 00 00 00 00 00 00 00
0x100000d8 : 00 00 00 00 00 00 00 00 00 00 00 00
0x100000e4 : 00 00 00 00 00 00 00 00 00 00 00 00
0x100000f0 : 00 00 00 00 00 00 00 00 00 00 00 00
0x100000fc : 00 00 00 00 00 00 00 00 00 00 00 00
```

```
[2020. 5. 20. 오전 12:24:47][Assembler]Codesize:16 Datasize:0
```