Muhammad Hamis Haider

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Professional Summary

I am a Postdoctoral Fellow with strong research experience in digital design, RISC-V–based SoCs, and FPGA acceleration. I have hands-on expertise in Verilog/SystemVerilog, RTL microarchitecture, synthesis-aware design, and UVM-based verification. My experience includes tapeout-style flows, reusable RTL IP, and hardware–software co-design. Please refer to my website for my latest publications and projects.

Experience

Postdoctoral Fellow – RTL & SoC Design *Saskatoon, SK, Canada*
KoLab, University of Saskatchewan *Jan 2026 – present*

- I am currently researching novel RISC-V vector co-processors for cycle accurate private AI inference and training at Edge for healthcare applications. We are targeting a ~20% decrease in energy consumption compared to the exiting state-of-the-art co-processors.
- I am working closely with industry partners to enable next-gen AI accelerator ASIC SoCs with built-in differential privacy to enable private AI in wearables and mobile devices. Reducing the differential privacy overhead by ~30-40%.
- I designed custom RTL accelerators for AI accelerationa at Edge improving throughput by ~20% under fixed power budgets.
- I develop reusable, parameterized RTL IP blocks integrated into RISC-V–based SoC platforms for tightly coupled co-processors for secure AI inference at Edge.
- I optimized datapaths and memory interfaces, reducing latency and on-chip memory traffic by ~20% in multiple approximate computation units for AI inference and training on FPGA and ASIC SoCs.

Doctoral Researcher, Electrical and Computer Engineering *Saskatoon, SK, Canada*
KoLab, University of Saskatchewan *Sept 2021 – Dec 2025*

PhD research under Dr. Seok-Bum Ko focused on efficient, reliable, and secure computing architectures for edge AI systems.

- Nominated for the Best Thesis Defence Award (2026). Awaiting decision.
- I designed novel RTL approximate compute units achieving 30–60% reductions in area and power versus baseline designs for AI inference at Edge.
- I implemented multi-precision and reconfigurable datapaths enabling up to ~50% compute cost reduction for AI trianing workloads.
- I developed RTL blocks validated through simulation and FPGA prototyping using synthesis-driven flows for AI accelerator design with native differential privacy.

Sessional Lecturer & Graduate Teaching Fellow (ECE) *Saskatoon, SK, Canada*
University of Saskatchewan *Jan 2023 – Dec 2025*

Teaching and curriculum delivery for undergraduate computer architecture and networking courses.

- Lecturer for CME 334: Network Architecture Design (3 credit hours), teaching cohorts of 10–40 students.
- Delivered lectures, designed assessments, and supervised labs covering modern network architectures.
- Graduate Teaching Fellow and Teaching Assistant for CME 433: Computer Architecture Design (40 students).
- Mentored students across three academic years (2022–2024), supporting labs, grading, and project guidance.

Research Assistant *Islamabad, Pakistan*
National University of Sciences and Technology (NUST) *Jan 2019 – Dec 2019*
Early-stage research in computer architecture under the supervision of Dr. Rehan Ahmed.

- Pioneered RISC-V architecture research at NUST.
- Contributed to the design of Pakistan's first in-house RISC-V microcontroller.
- Supported RTL development and architectural validation for custom processor designs.

Education

University of Saskatchewan *Saskatoon, SK, Canada*
PhD in Electrical and Computer Engineering *Sept 2021 – Dec 2025*
Field of Research: Computer Architecture Design

- CGPA: 93.167% (3.98/4.00)
- Thesis: Design of Next-Generation Hardware-Accelerated Edge AI Engines for Privacy Preservation
- Supervisor: Dr. Seok-Bum Ko

National University of Sciences and Technology (NUST) *Islamabad, Pakistan*
Bachelor of Science in Electrical Engineering (Computer Engineering) *Sept 2017 – June 2021*

- CGPA: 3.68/4.00
- Final Year Project: Object-Avoiding Autonomous Drone for Humanitarian Operations
- Advisor: Dr. Rehan Ahmed

Publication

Power-Efficient and Reconfigurable Compute Unit for Multi-Precision AI Inference at the Edge Jan 2026
Muhammad Hamis Haider, Hao Zhang, Seok-Bum Ko
(IEEE International Symposium on Circuits and Systems (ISCAS))

Memory-Efficient Differential Privacy Accelerator Jan 2025
Muhammad Hamis Haider, Nam J. Kim, Hao Zhang, Jorge Arias-Garcia, Hyun J. Lee, Seok-Bum Ko
(IEEE Asia Pacific Conference on Circuits and Systems (APCCAS))

Exploring Hardware-Driven Privacy Techniques for Trustworthy Machine Learning Jan 2025
Muhammad Hamis Haider, Hao Zhang, S. Deivalaskhmi, G. Lakshmi Narayanan, Seok-Bum Ko
(Springer (Book Chapter))

Optimized Transformer Models: ℓ' BERT with CNN-like Pruning and Quantization Jan 2024
Muhammad Hamis Haider, Sebastian Valarezo-Plaza, S. Muhsin, Hao Zhang, Seok-Bum Ko
(IEEE International Symposium on Circuits and Systems (ISCAS))

Is Neuromorphic Computing the Key to Power-Efficient Neural Networks: A Survey Jan 2024
Muhammad Hamis Haider, Hao Zhang, S. Deivalaskhmi, G. Narayanan, Seok-Bum Ko
(Springer (Book Chapter))

Decoder Reduction Approximation Scheme for Booth Multipliers Jan 2023
Muhammad Hamis Haider, Hao Zhang, Seok-Bum Ko
(IEEE Transactions on Computers)

Booth-Encoding-Based Energy-Efficient Multipliers for Deep Learning Systems Jan 2022
Muhammad Hamis Haider, Hao Zhang, Seok-Bum Ko
(IEEE Transactions on Circuits and Systems II: Express Briefs)

Awards

Best PhD Defense (Nomination) Dec 2025
Nominated by the PhD Defense Committee in recognition of the quality, originality, and technical depth of the doctoral thesis.
University of Saskatchewan

Teacher-Scholar Doctoral Fellowship June 2024
Competitive fellowship awarded for excellence in teaching and scholarship, supporting instruction of a 3rd-year undergraduate engineering course.
University of Saskatchewan

Graduate Teaching Fellowship Apr 2023
Selected to serve as a Graduate Teaching Fellow under the supervision of Dr. Seok-Bum Ko, contributing to course delivery and student mentorship.
University of Saskatchewan

Skills

Architecture & Hardware Design: Computer architecture, accelerator design, system-on-chip (SoC), RISC-V, approximate computing units, edge AI inference and training

AI & Model Optimization: Differentially private AI models, edge-optimized architectures, training and inference optimization for large language models (GPT, BERT)

Programming Languages: SystemVerilog, Verilog, C++, Python (AI frameworks, Django, web development), JavaScript, ReactJS, NodeJS, OCaml

EDA Tools & Platforms: Intel Quartus, Xilinx Vivado, Synopsys Design Compiler, Power Compiler, VCS

Languages: English (fluent, CELPIP-G[L/R/W/S]: 12/11/12/11), Urdu (native)