



University of Haripur

Khyber Pakhtoonkhwa

Lab Reports

Submitted by : Hammad Younis Abbasi

Section : D

Course Title : Digital and Logic Design (DLD)

Department : Information Technology

Submitted to

Name : Noshaba Naeem

Lecturer in University of Haripur (KPK)



University of Haripur

Khyber Pakhtoonkhwa

DLD LAB :

Assignment title:

Lab report 1

Topic name :

Implementation of And, Or, Nand, Nor and Not gate

Objective :

To prove truth table of these gates

Equipment used :

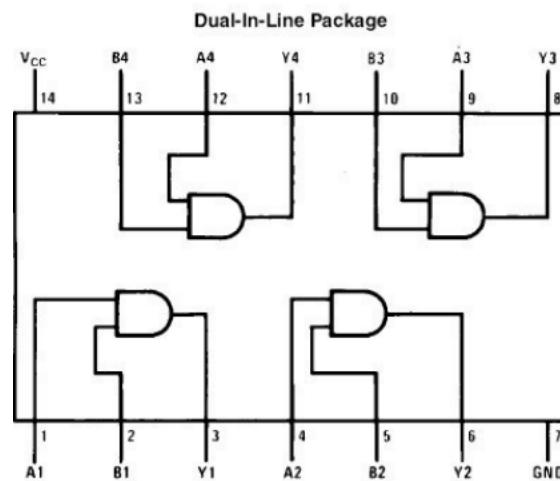
1. IC Chip 74ls04
2. IC Chip 74ls08
3. IC Chip 74ls02
4. IC Chip 74ls00
5. IC Chip 74ls32
6. Connecting wires

Logical Gates :

Logic gates are basic building blocks of a digital circuits. They takes one or more binary inputs (0s and 1s) and produce a single binary output. Each gate perform a specific logical operation based on Boolean algebra.

1. **AND gate:** - Function of AND gate is to give the output true when both the inputs are true. In all the other remaining cases output becomes false. Following table justifies the statement:-

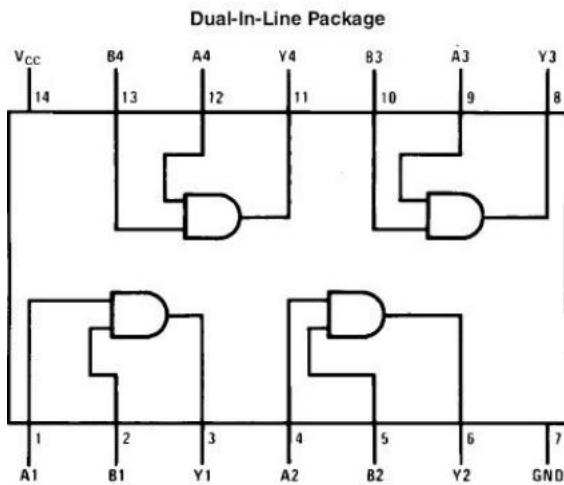
Input A	Input B	Output
1	1	1
1	0	0
0	1	0
0	0	0



IC 7408

2. OR gate: - Function of OR gate is to give output true when one of the either inputs are true .In the remaining case output becomes false. Following table justify the statement:-

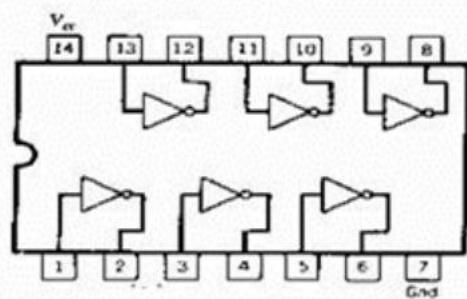
Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1



IC 7432

3. **NOT gate:-** Function of NOR gate is to reverse the nature of the input .It converts true input to false and vice versa. Following table justifies the statement :-

Input	Output
1	0
0	1

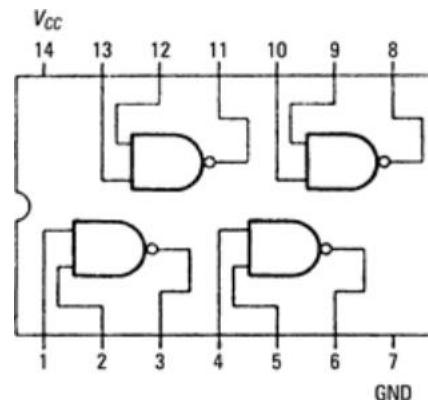


IC 7404

Universal Gates

1. **NAND gate:** - Function of NAND gate is to give true output when one of the two provided input are false. In the remaining output is true case. Following table justifies the statement :-

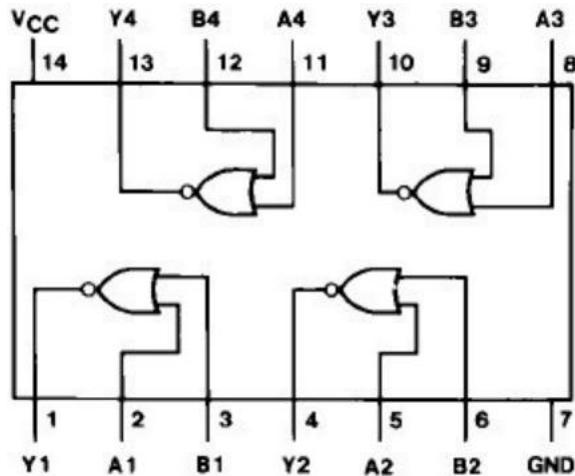
Input A	Input B	Output
1	1	0
1	0	1
0	1	1
0	0	1



IC 7400

2. **NOR gate:** - NOR gate gives the output true when both the two provided input are false. In all the other cases output remains false. Following table justifies the statement:-

Input A	Input B	Output
1	1	0
1	0	0
0	1	0
0	0	1

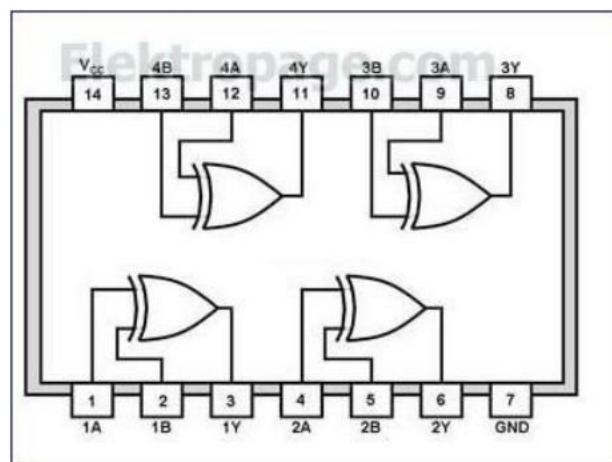


IC 7402

Advanced gate

1. **XOR gate:** - The function of XOR gate is to give output true only when both the inputs are different. Following table explains this:-

Input A	Input B	Output
1	1	0
1	0	1
0	1	1
0	0	0



IC 74136

2nd Lab Report:

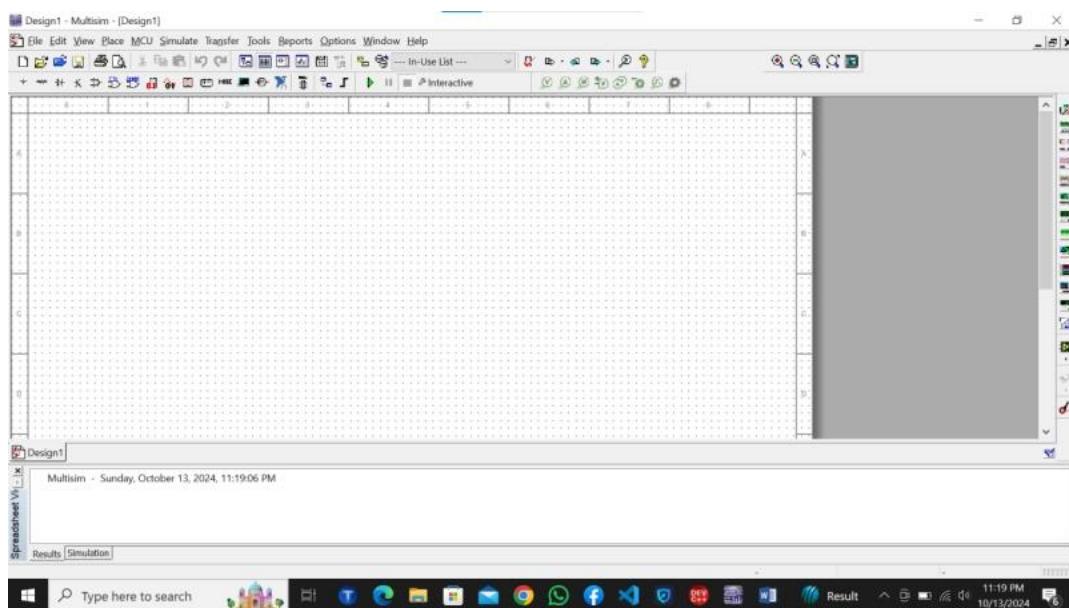
INSTALLATION OF NI MULTISIM 14.3 VERSION:

First of all I visit pesktop website.

The link of site is given below:

<https://pesktop.com/en/windows/multisim>

Then click on direct download. After download multisim setup, install it but it is paid software so I crack it for free use.



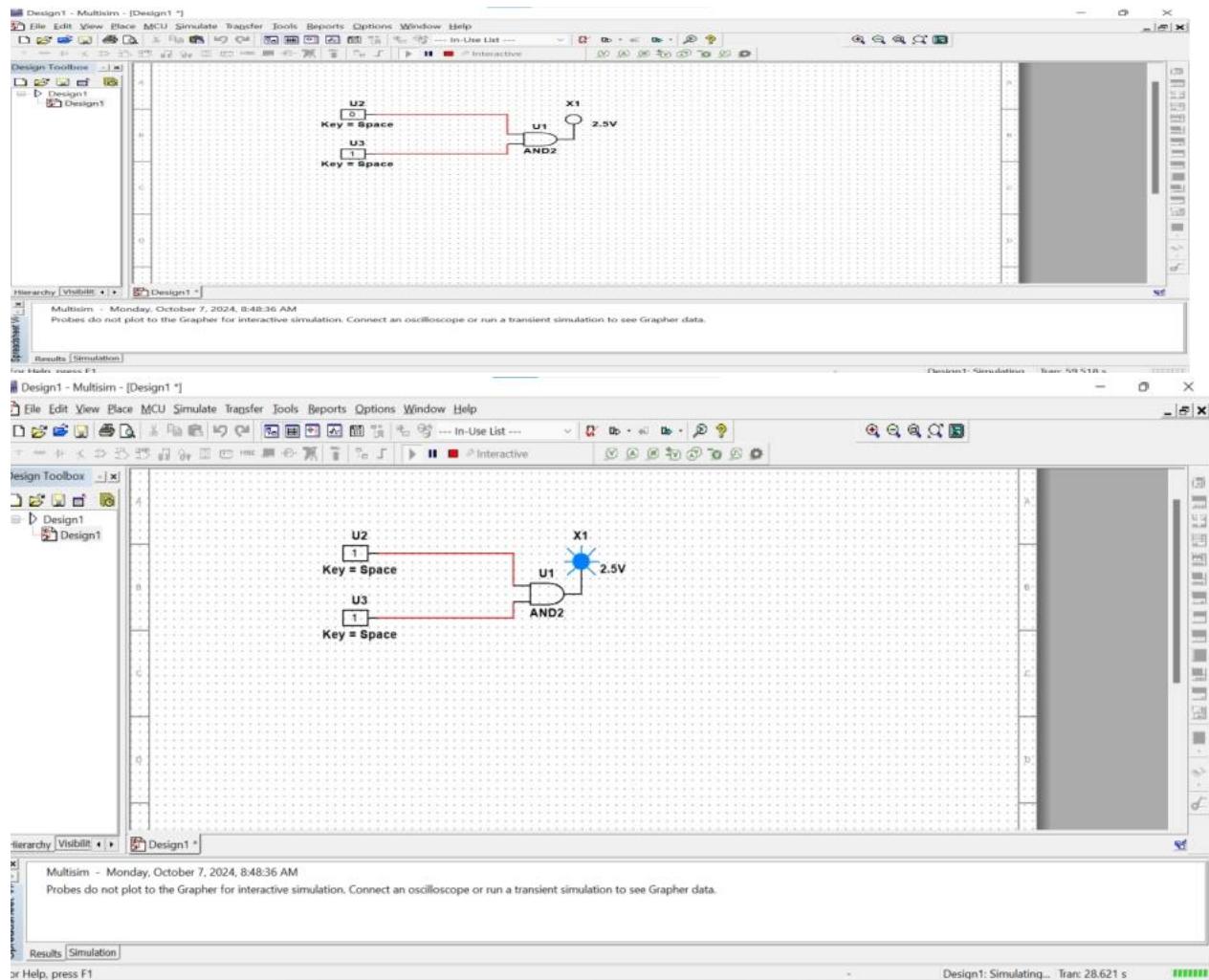
3rd Lab Report

Logical Gates

1. AND GATE:

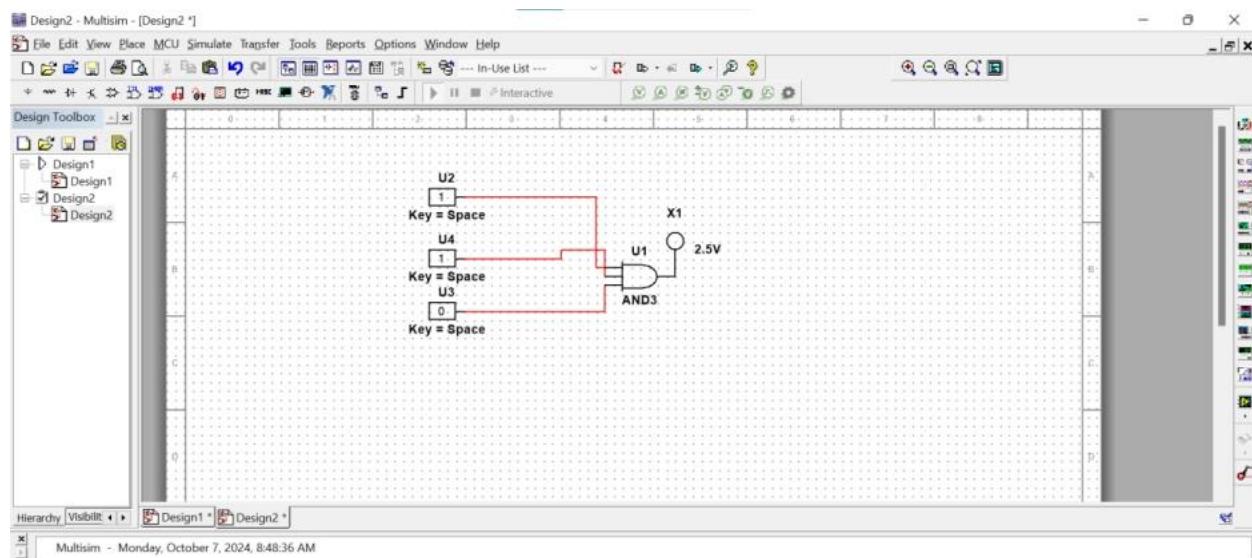
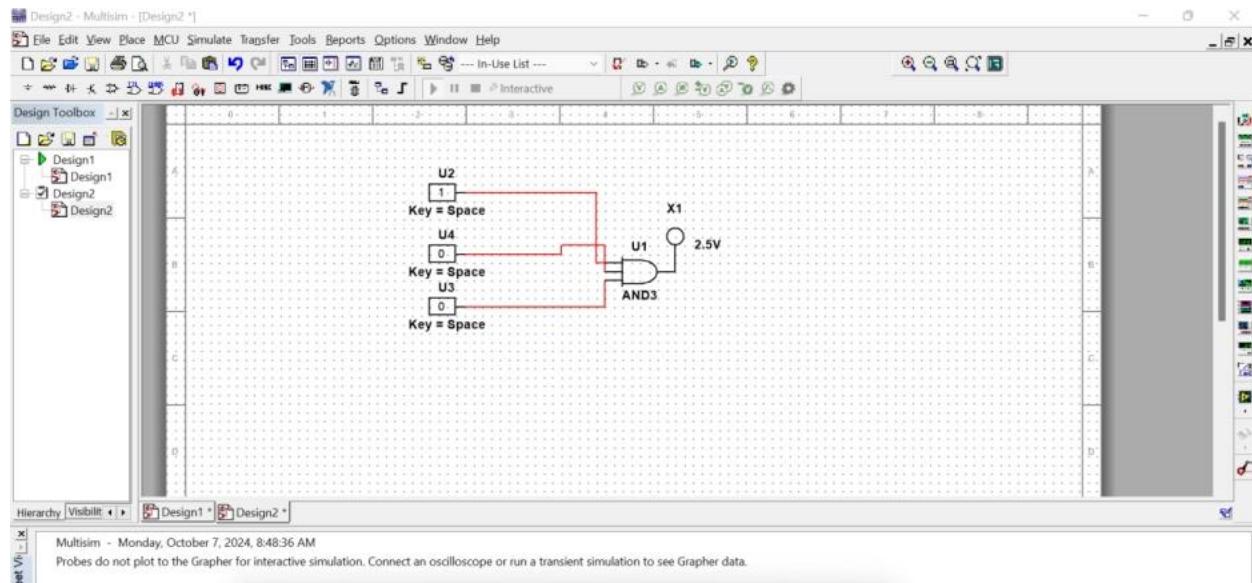
AND2:

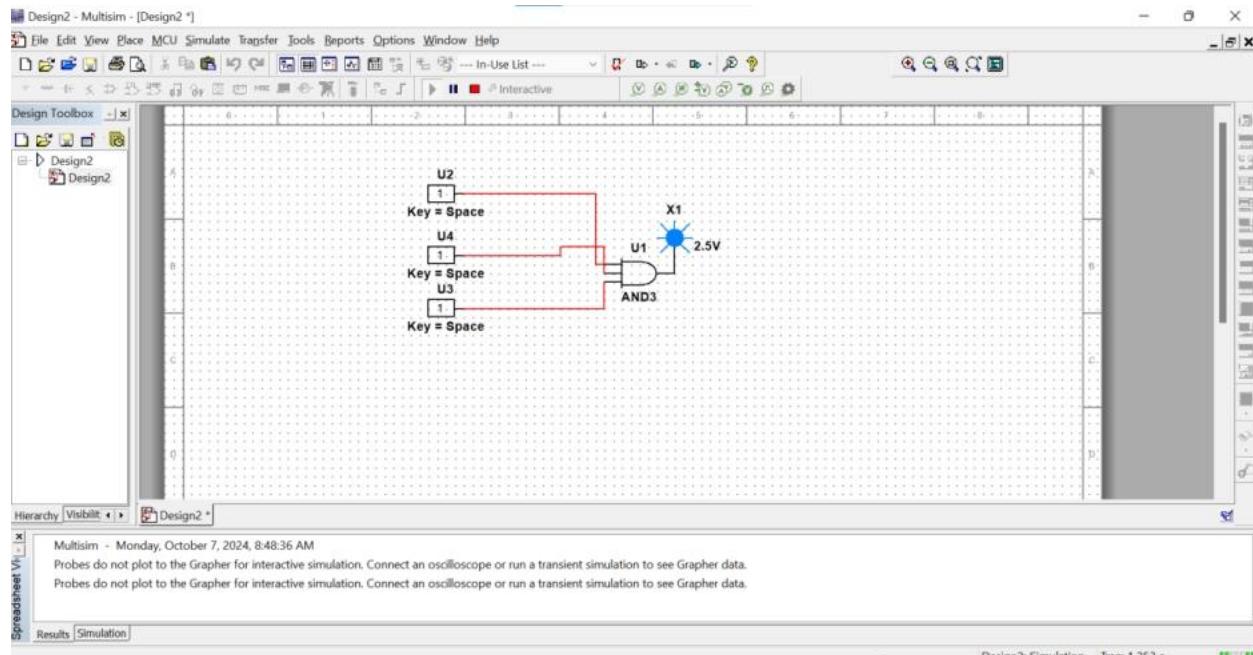
X	Y	X.Y
0	0	0
0	1	0
1	0	0
1	1	1



AND 3:

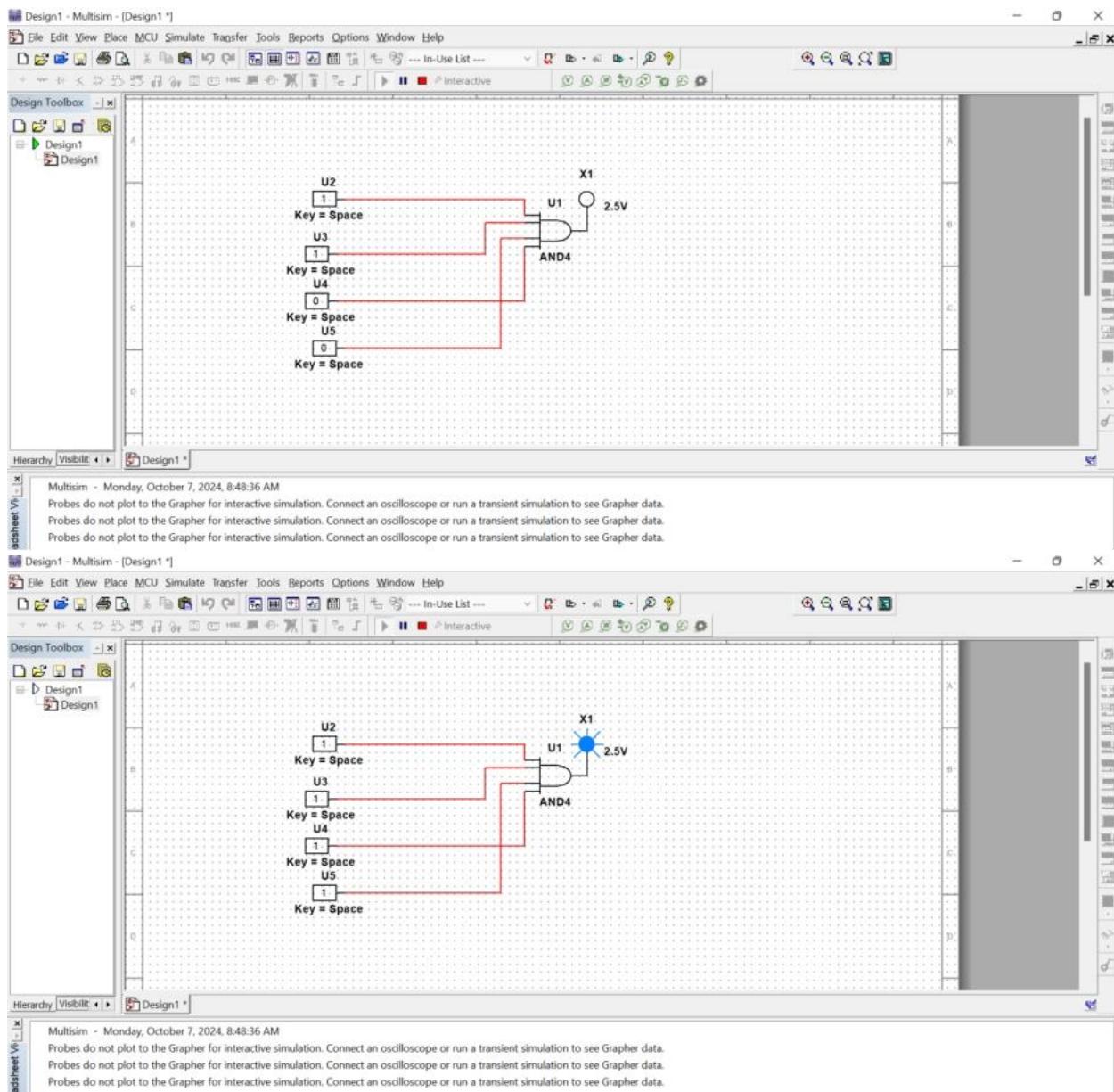
X	Y	Z	X.Y.Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1





AND 4:

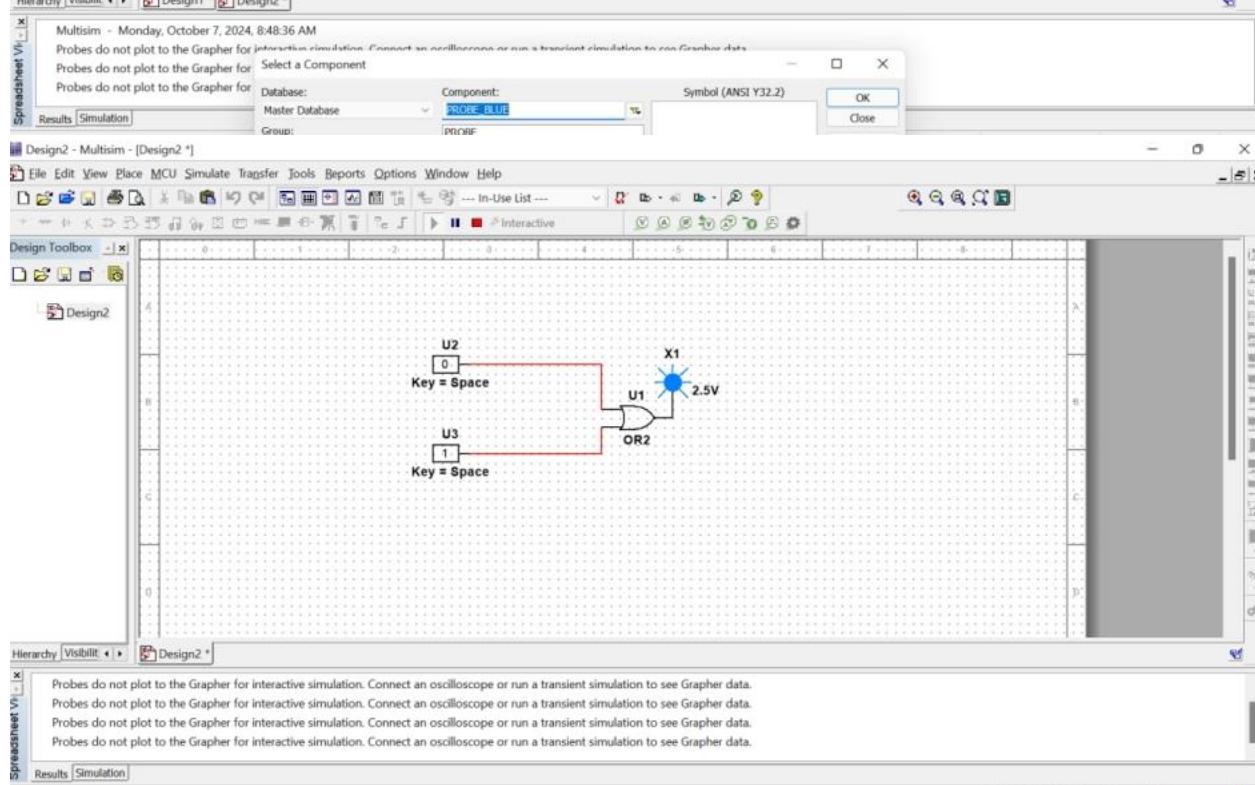
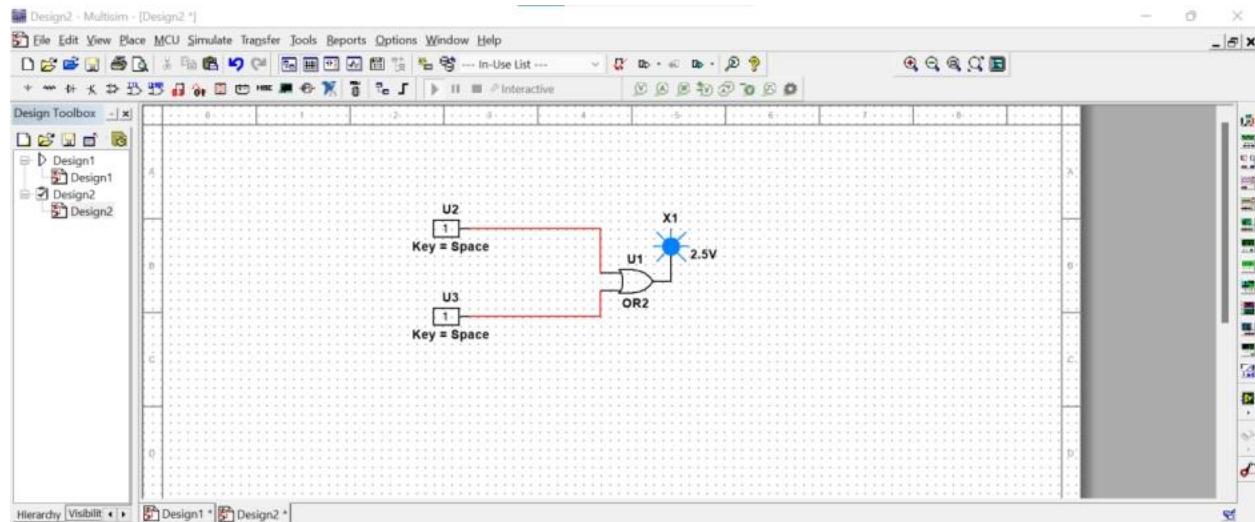
W	X	Y	Z	W.X.Y.Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

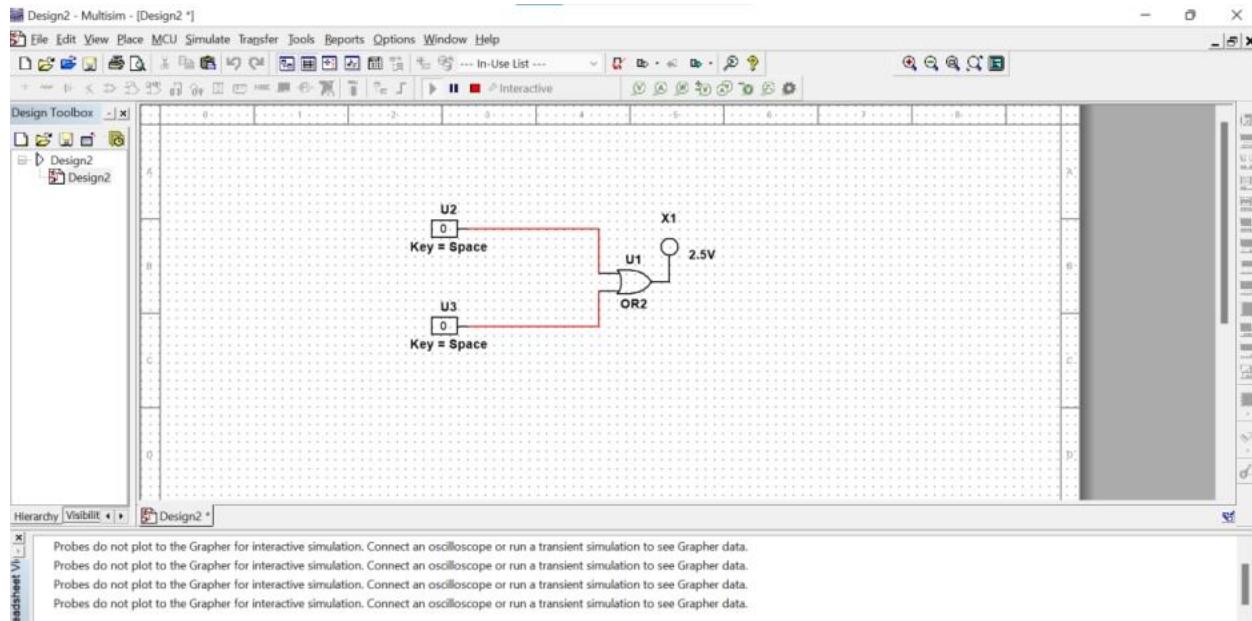


2. OR:

OR 2

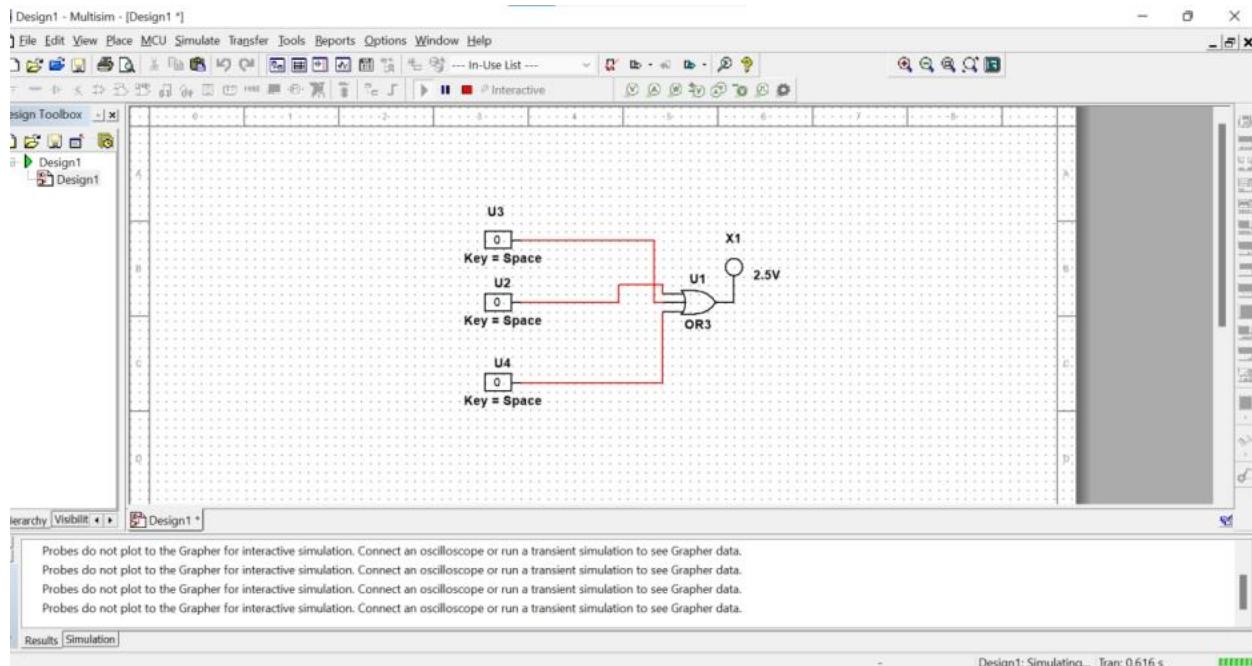
X	Y	X+Y
0	0	0
0	1	1
1	0	1
1	1	1

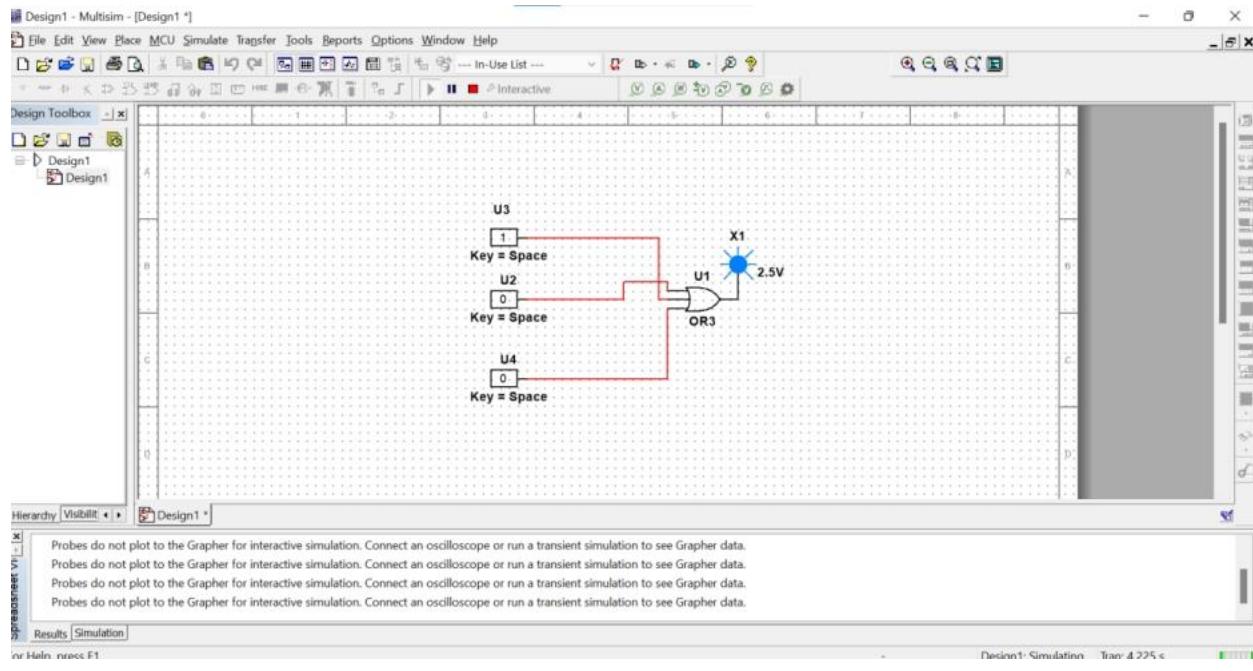




OR 3:

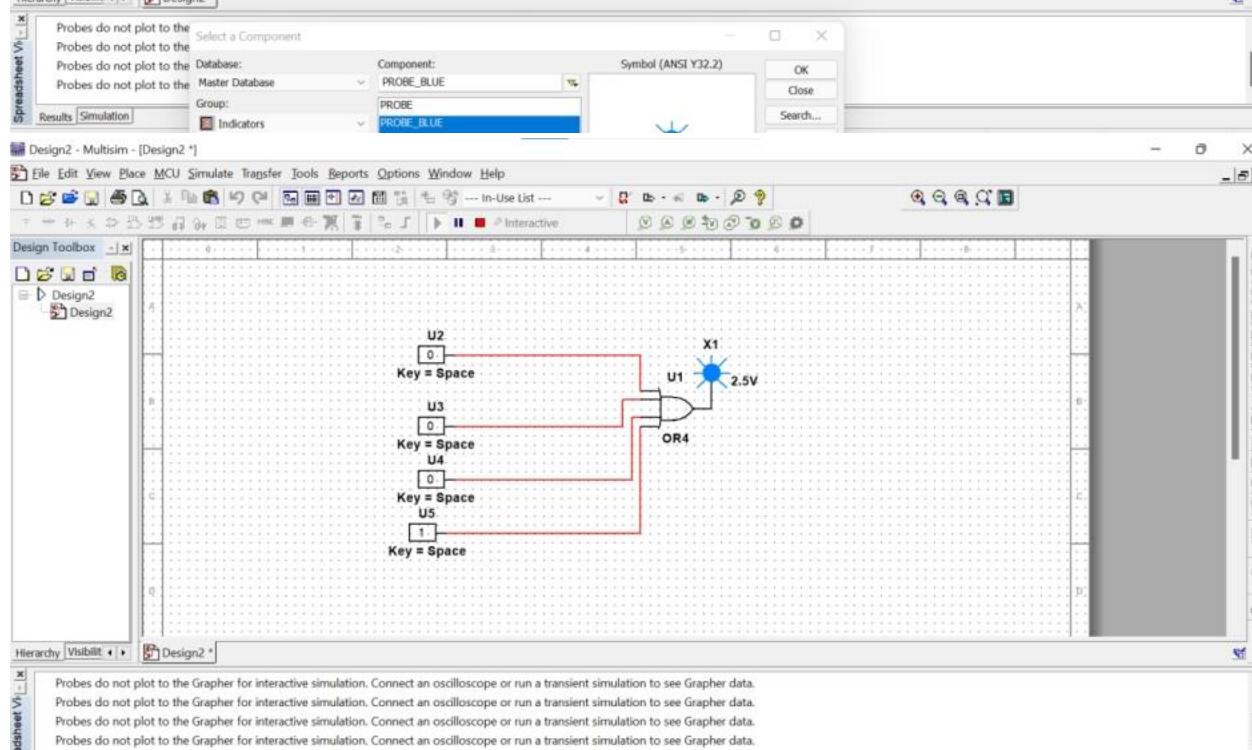
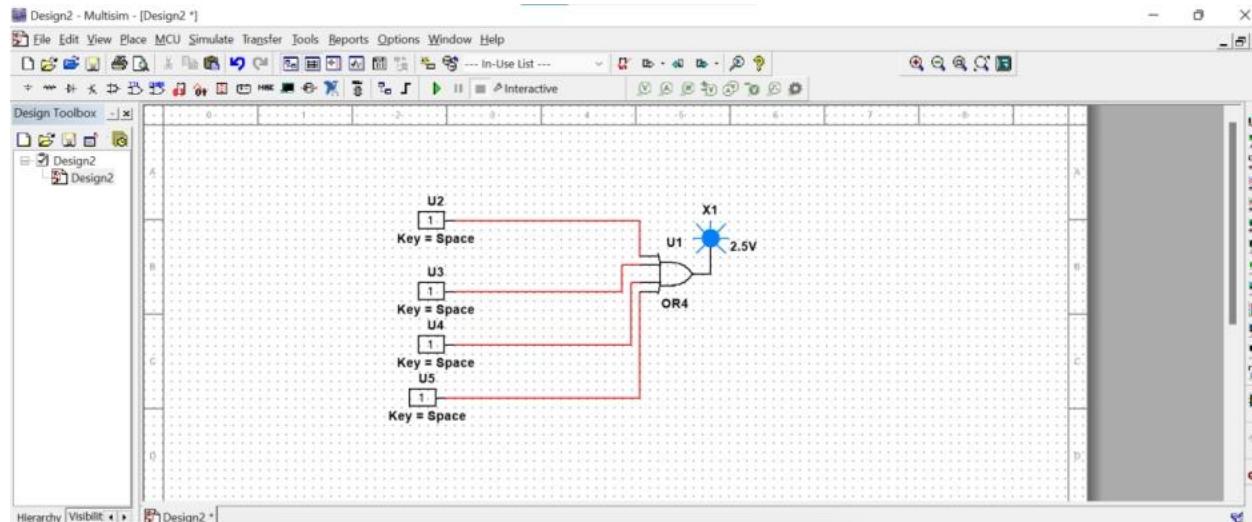
X	Y	Z	X.Y.Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

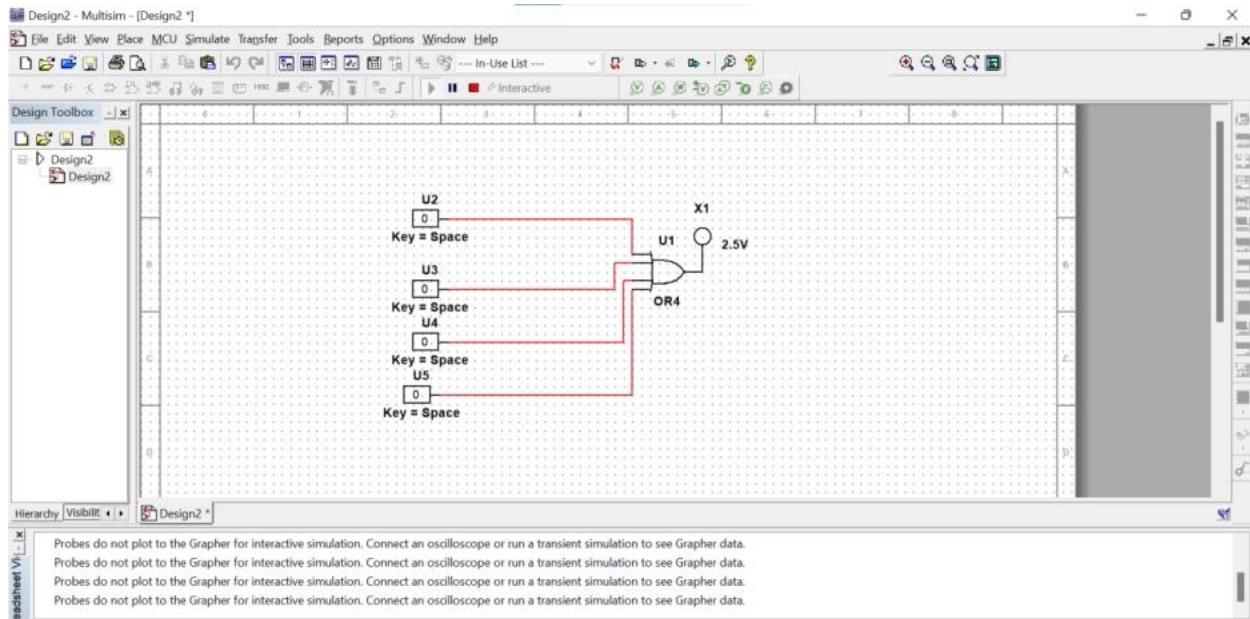




OR4:

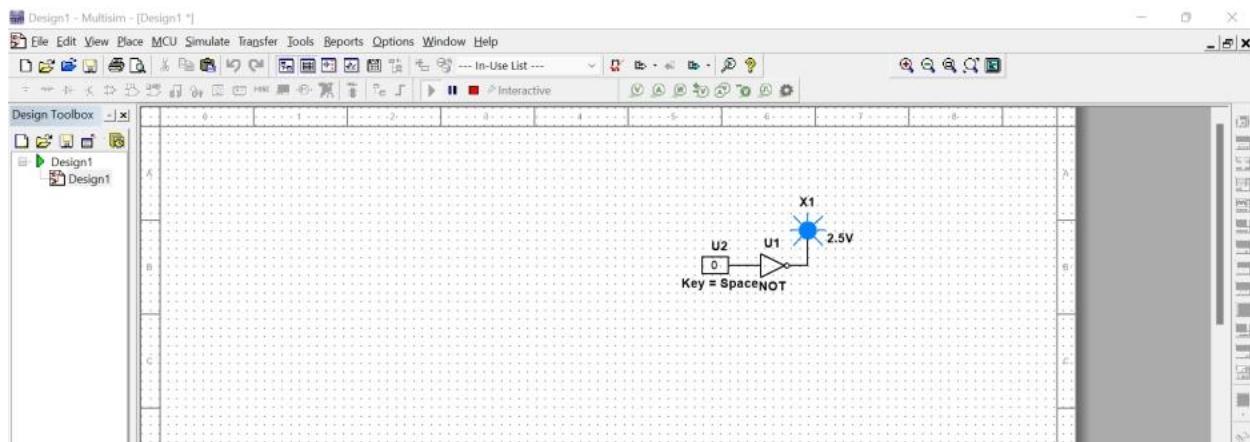
W	X	Y	Z	W+X+Z
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

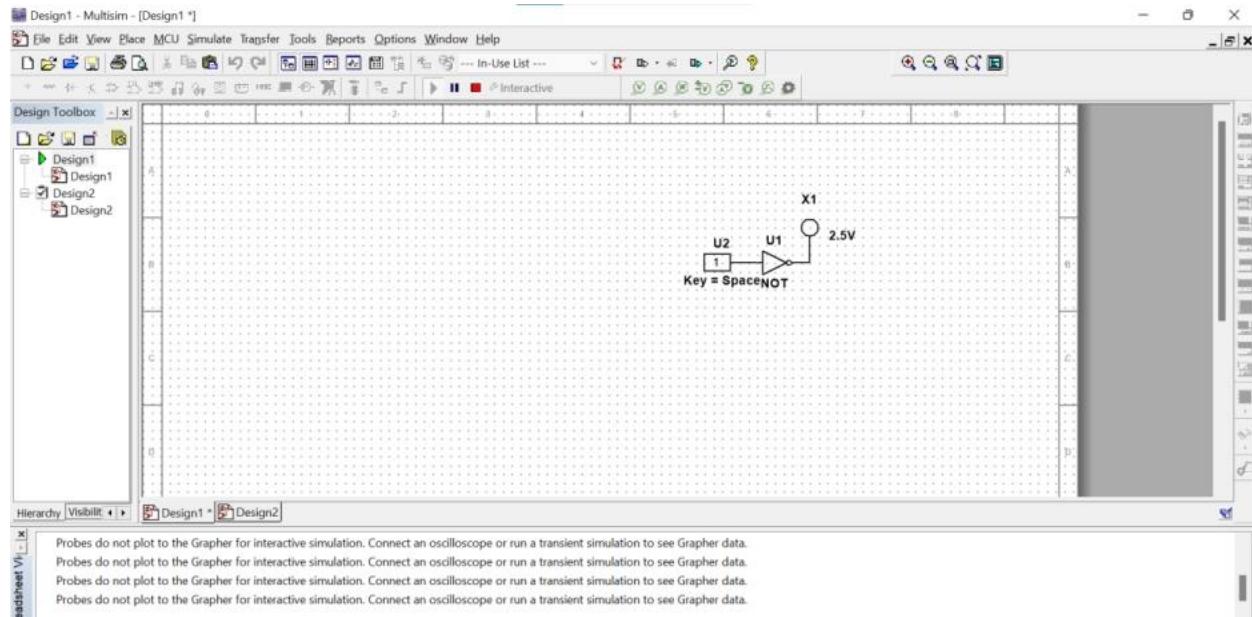




3. NOT:

X	Y
O	1
1	O

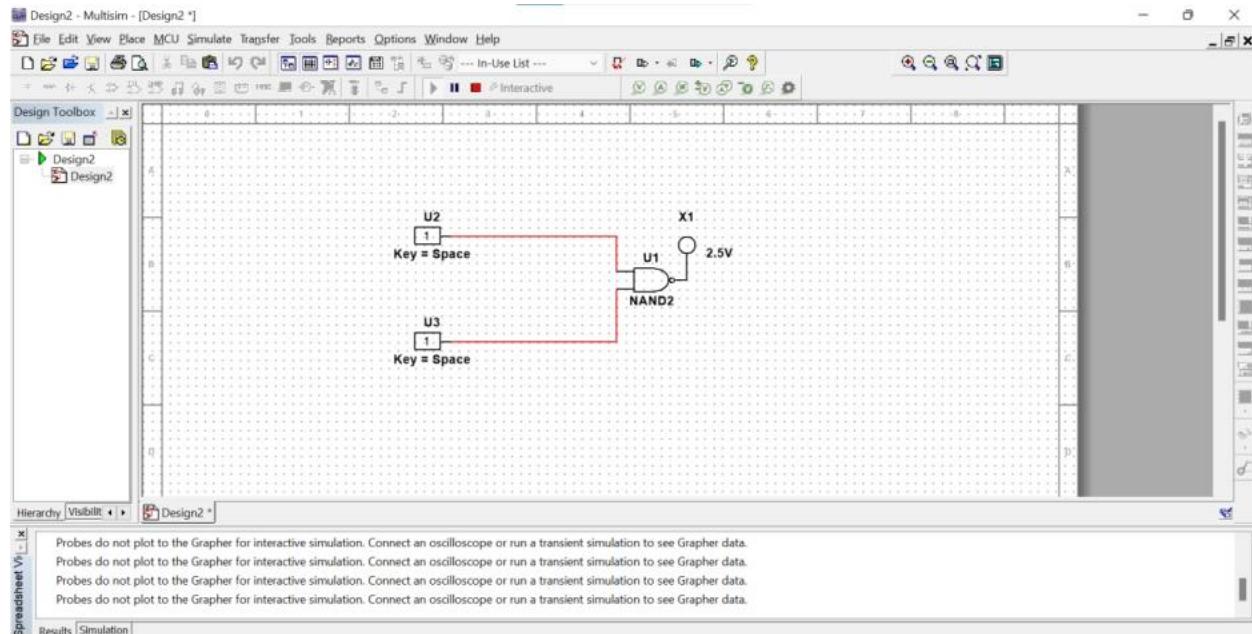


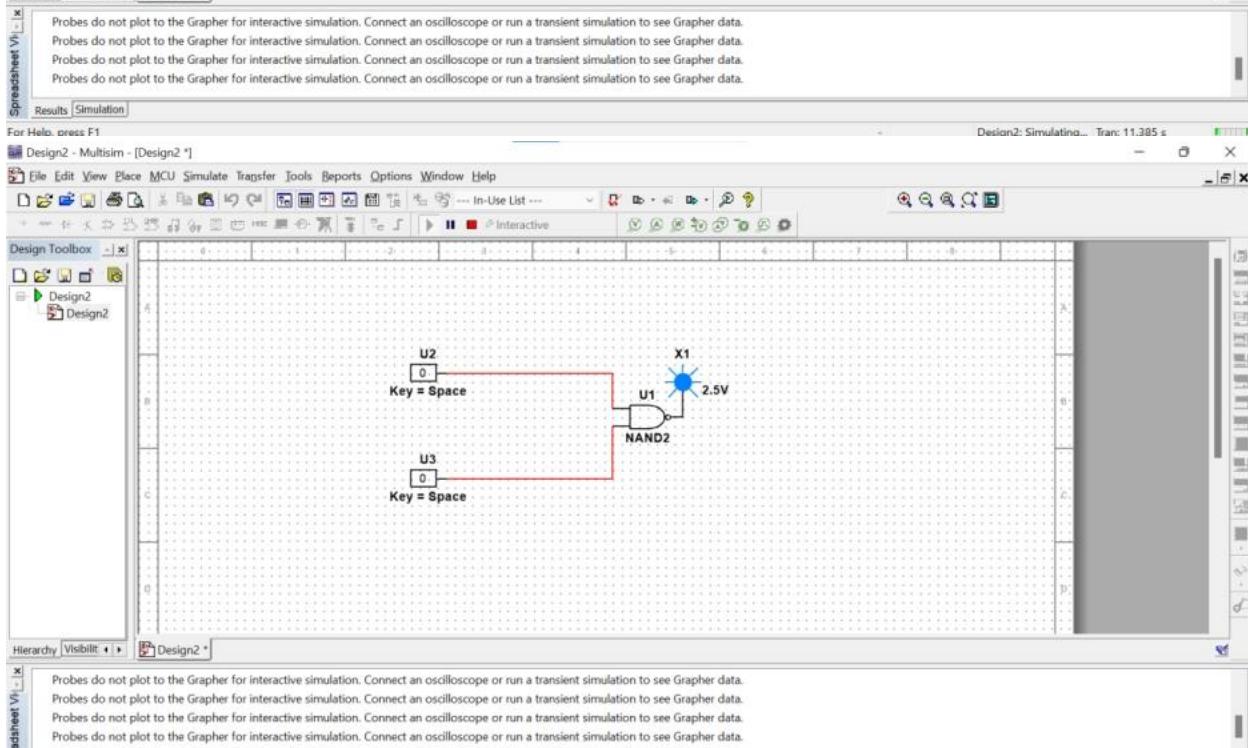
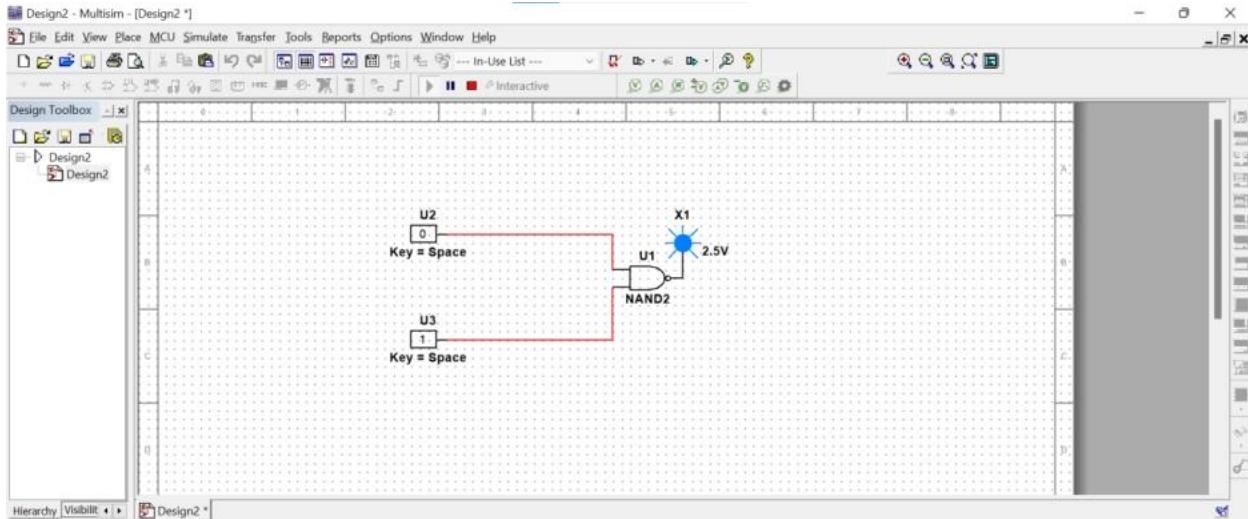


4. NAND:

NAND 2:

X	Y	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0





Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Results Simulation

For Help, press F1

Design2: Simulating... Tran: 11.385 s

Design2 - Multisim - [Design2 *]

File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help

Design Toolbox

Design2

Key = Space

Key = Space

U1 2.5V

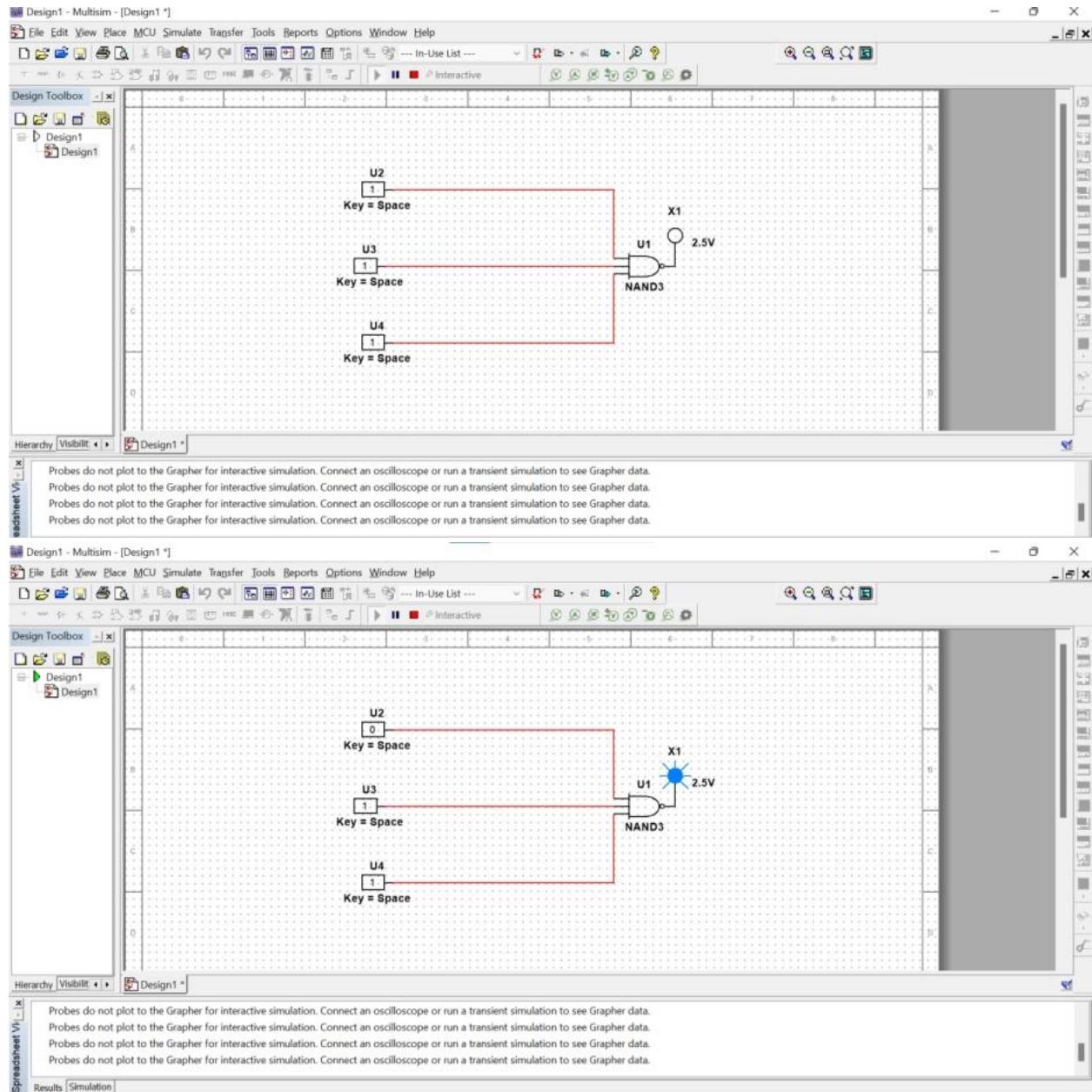
NAND2

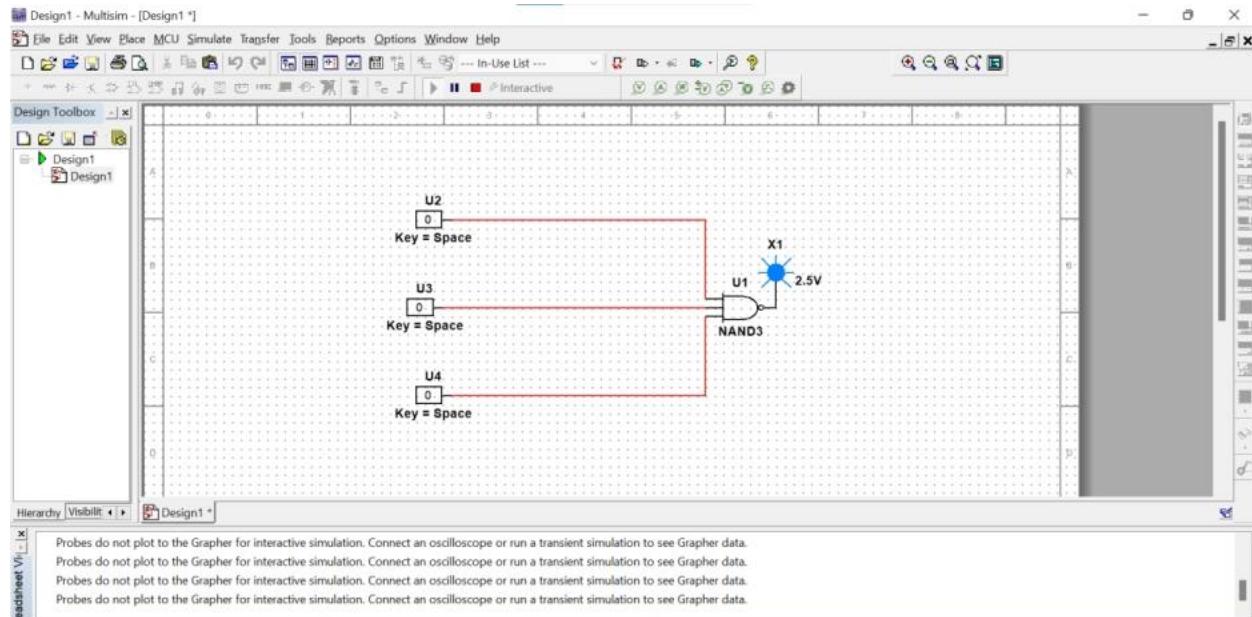
X1

Design2

NAND 3:

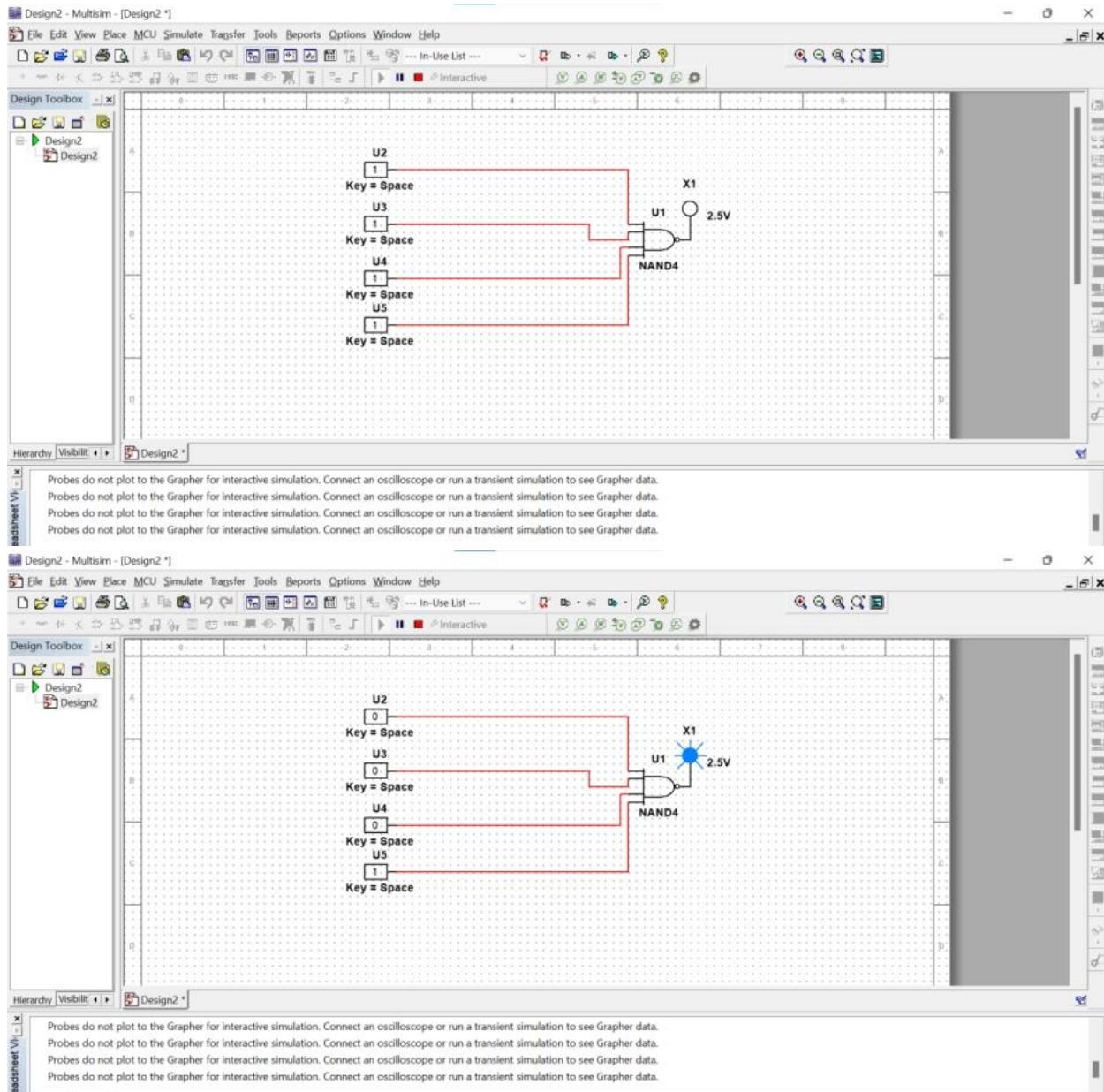
X	Y	Z	OUTPUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

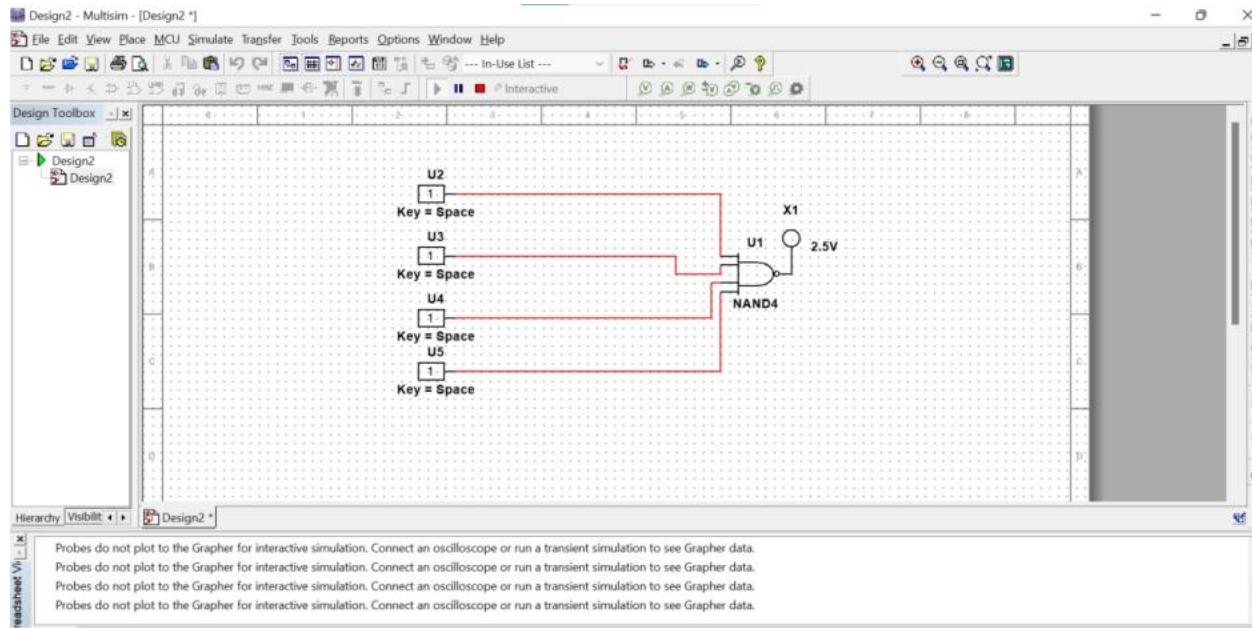




NAND 4:

W	X	Y	Z	OUTPUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	1	0	1
1	1	1	1	0

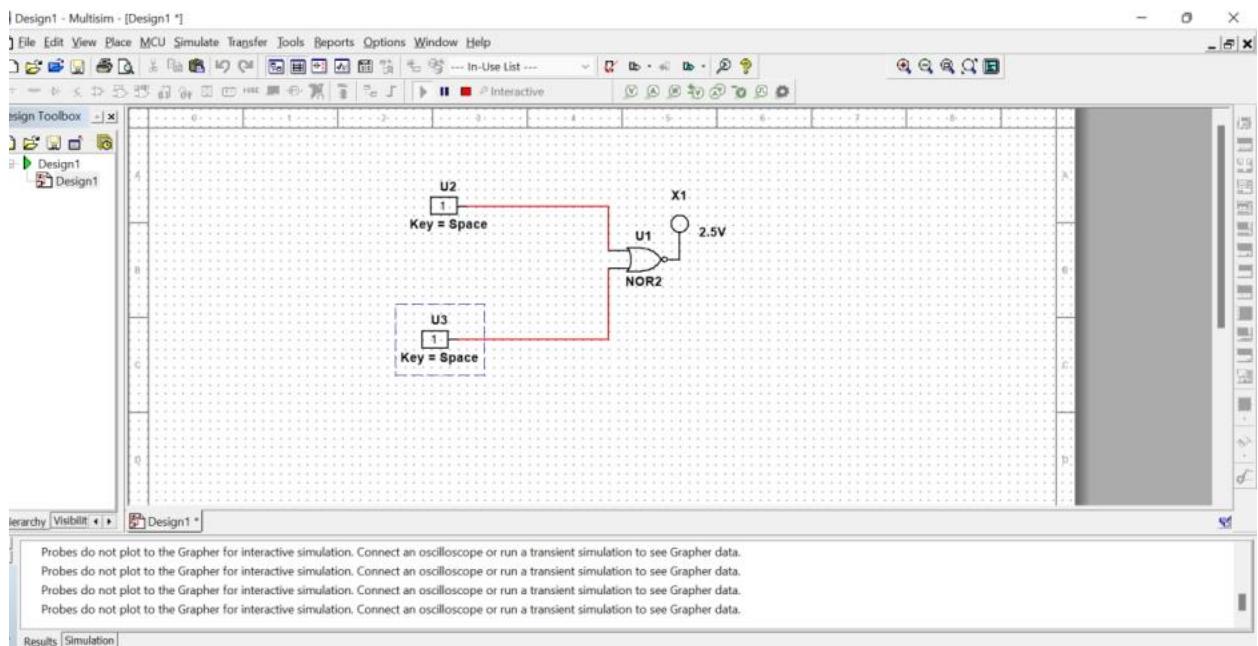


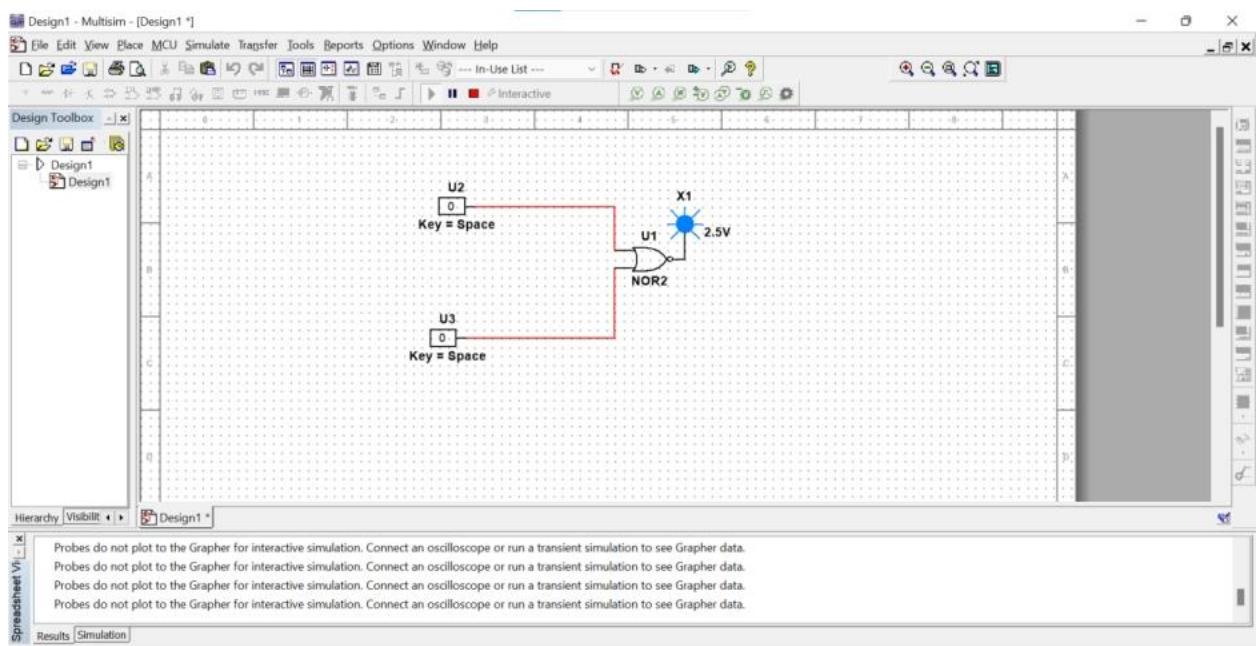
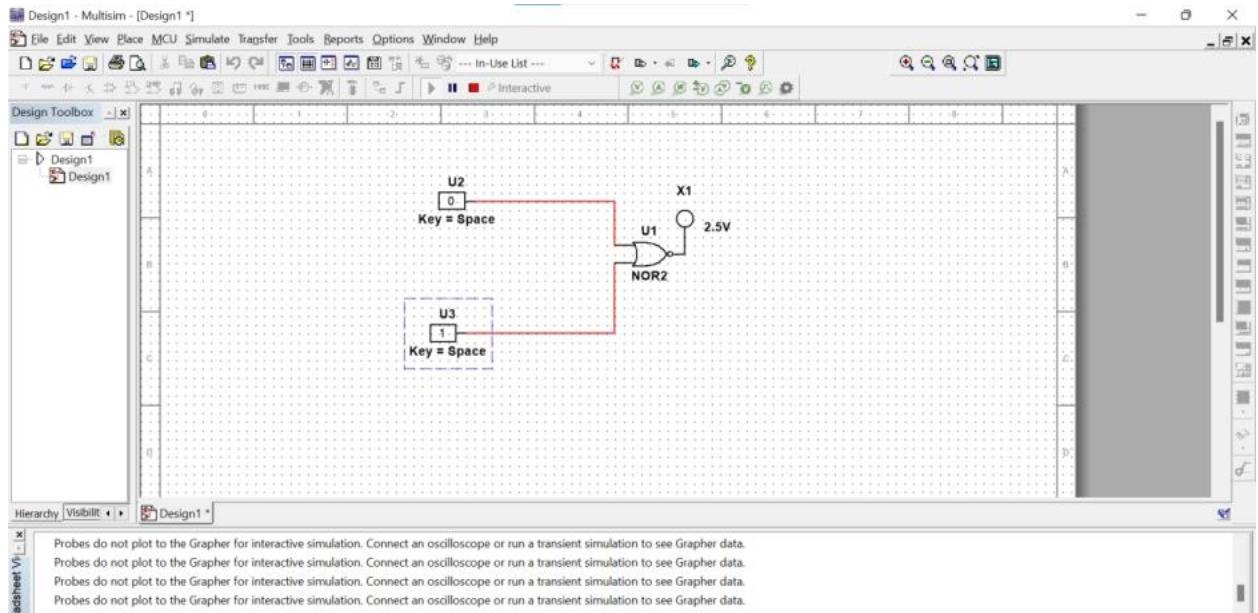


5. NOR:

NOR 2

X	Y	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

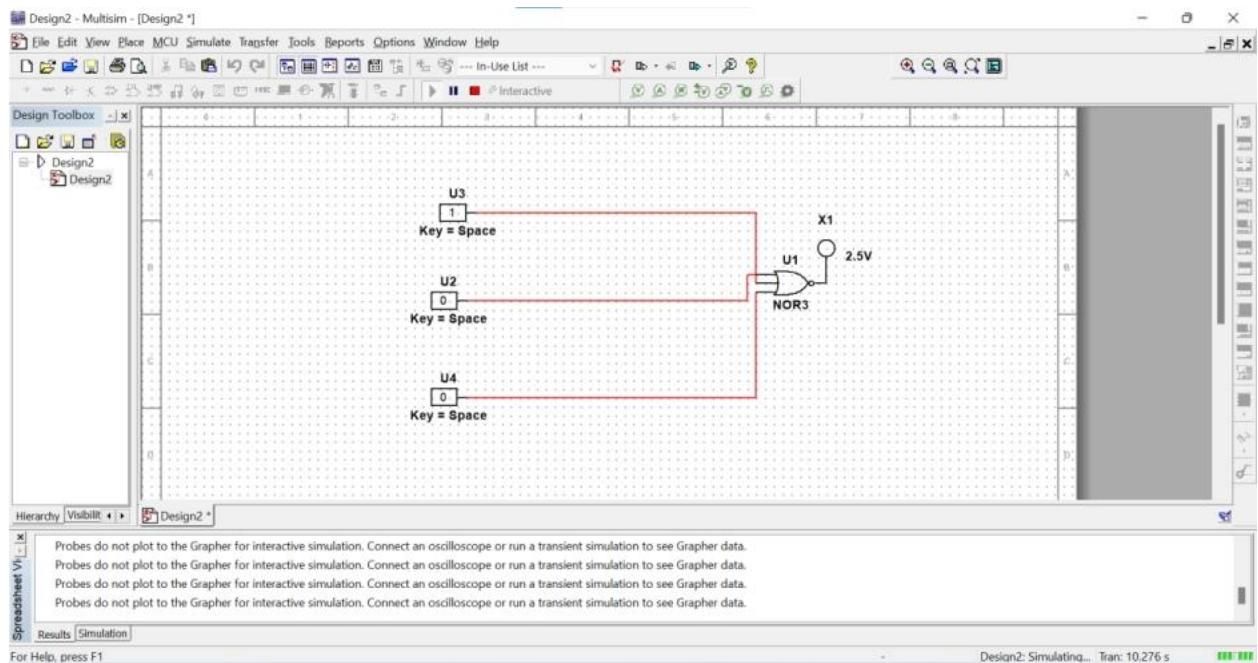
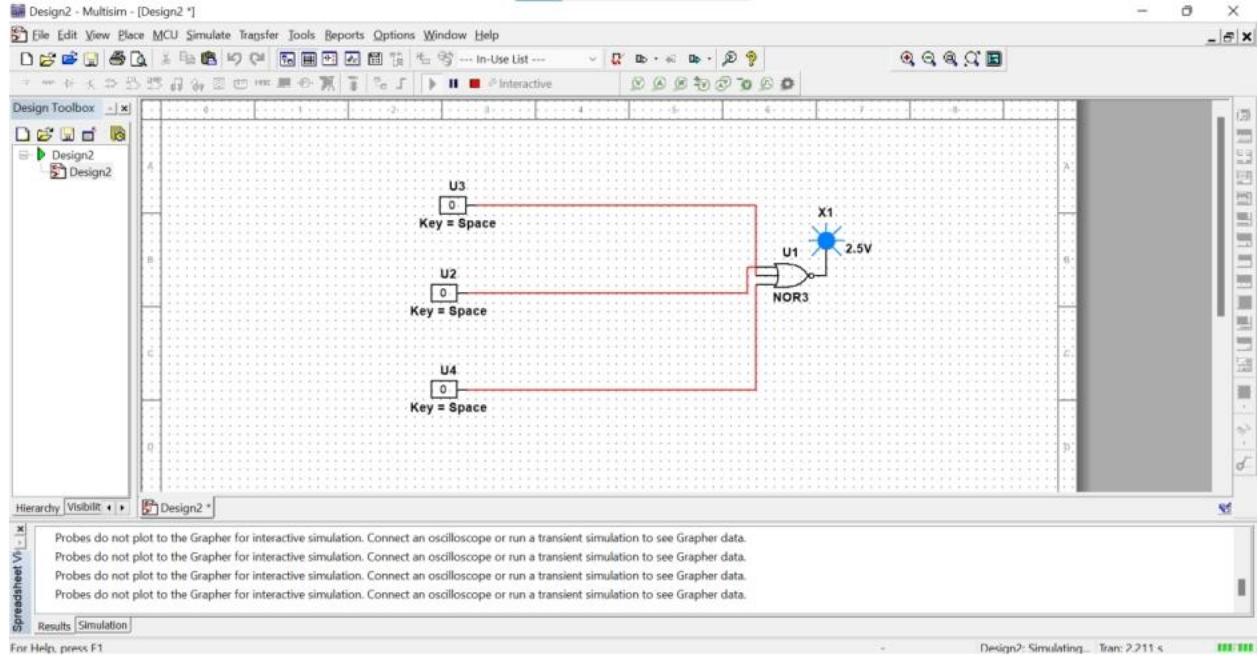


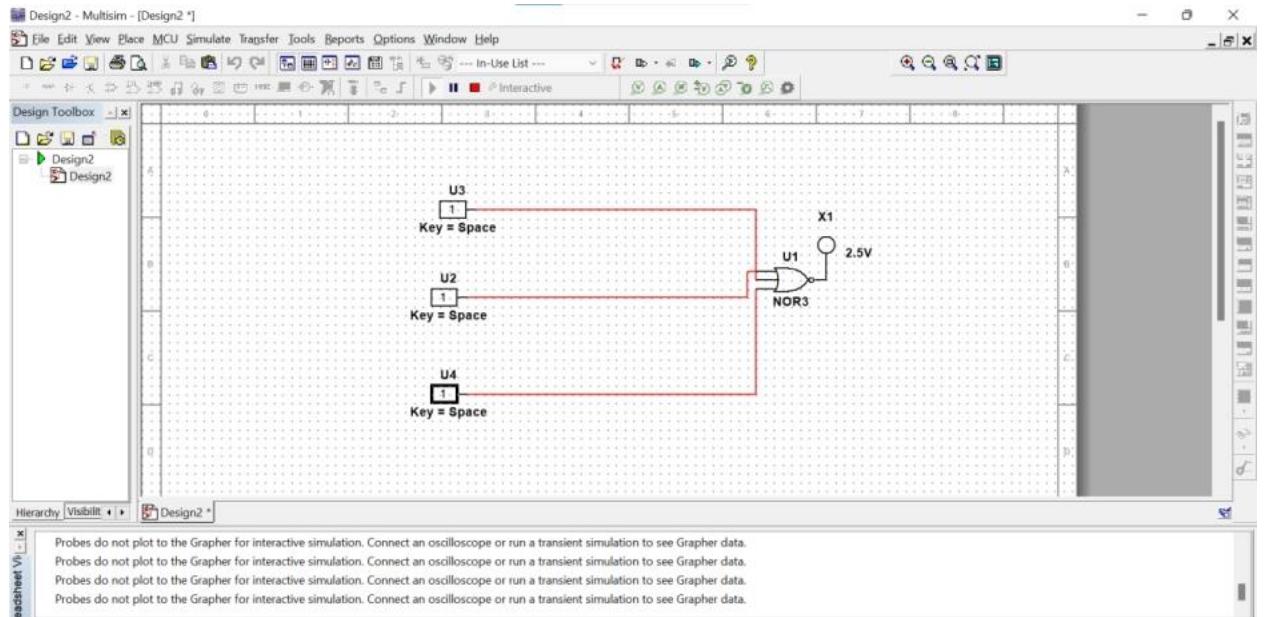


NOR 3:

X	Y	Z	OUTPUT
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0

1	1	0	0
1	1	1	0





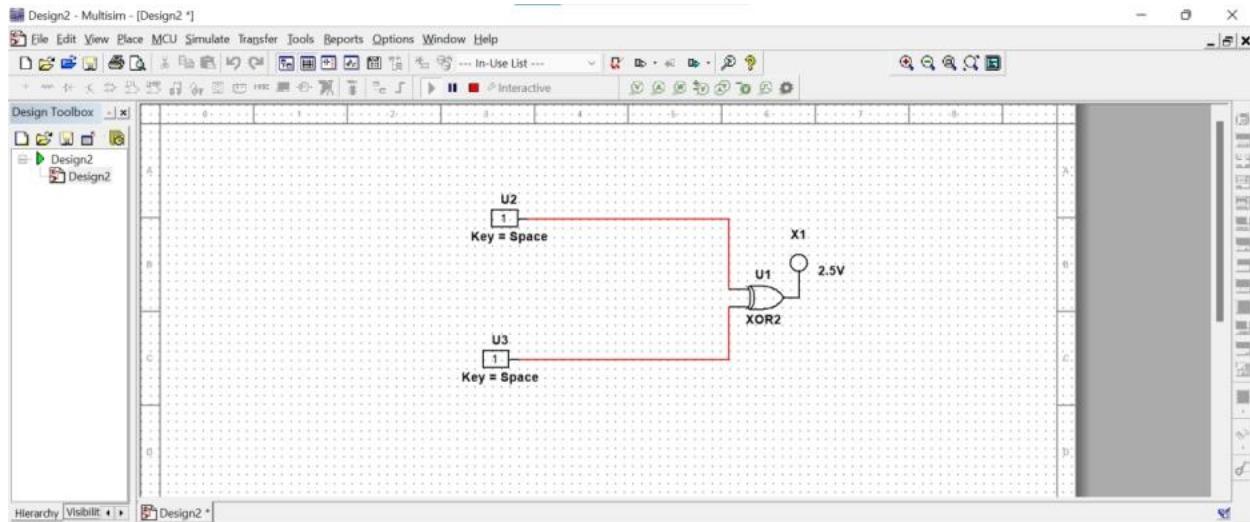
NOR 4:

W	X	Y	Z	OUTPUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0

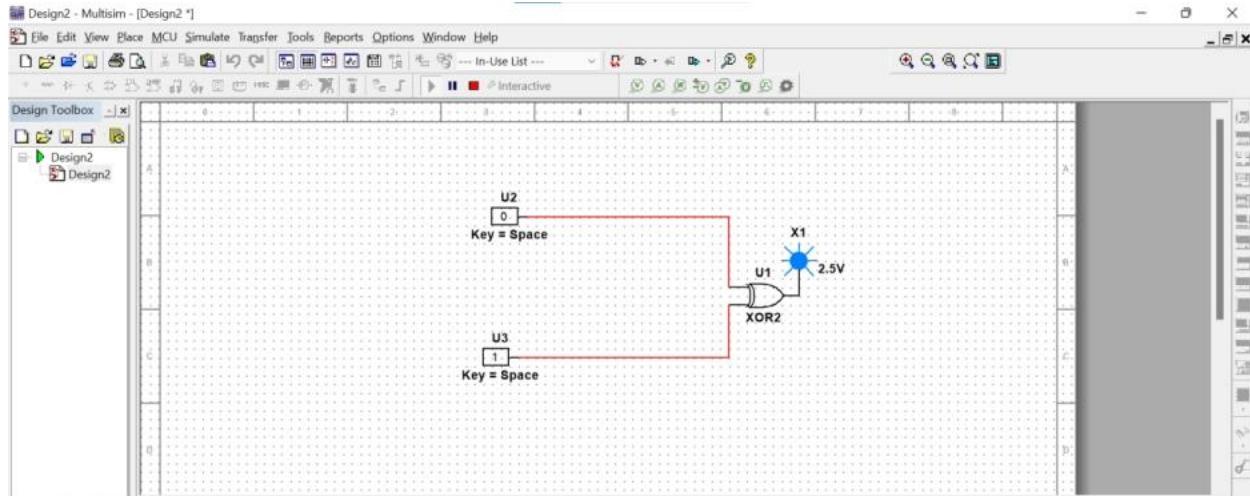
6. XOR

XOR 2:

X	Y	OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

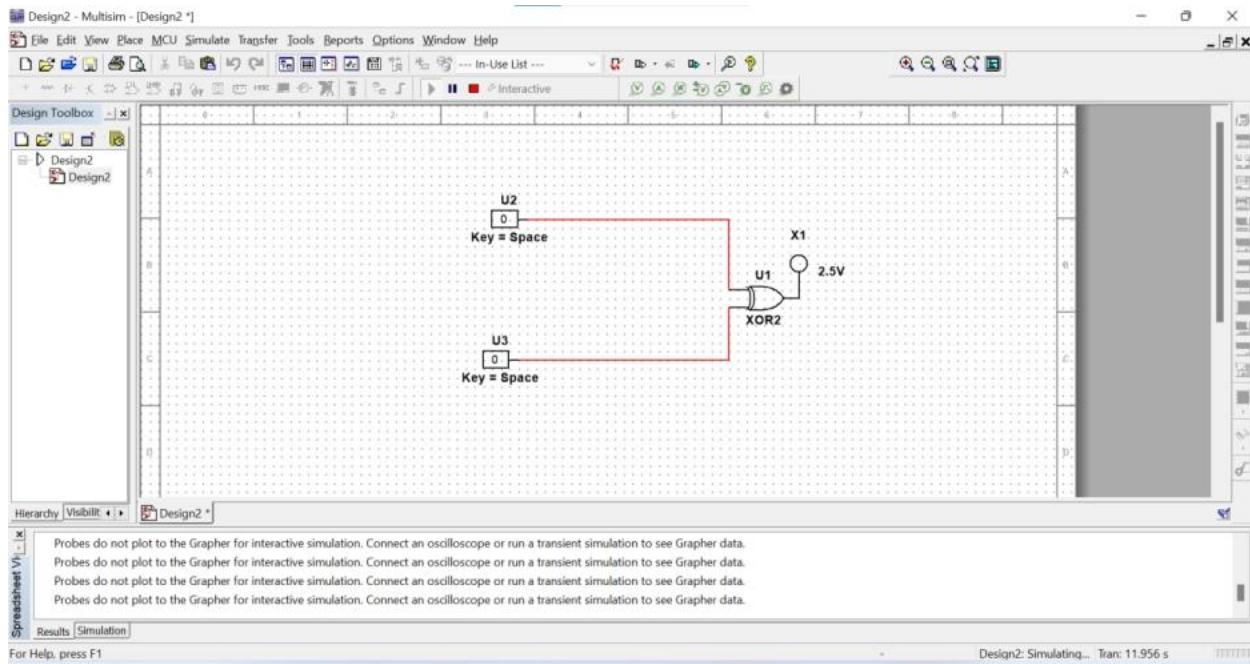


Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.



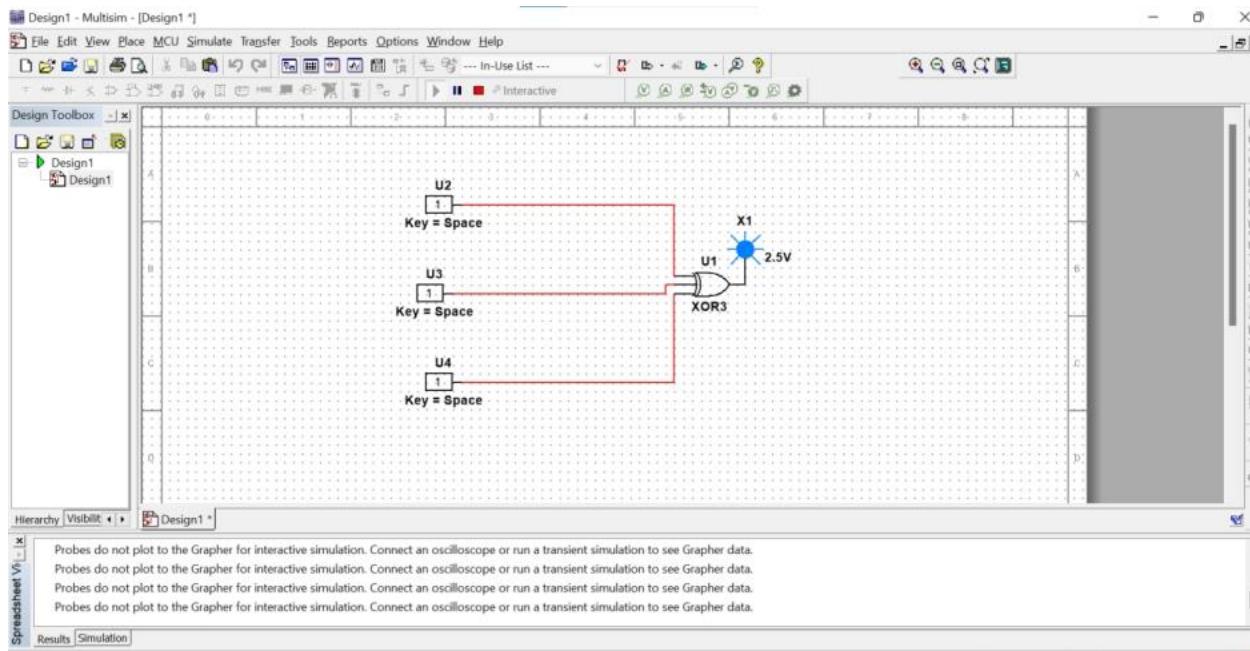
Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

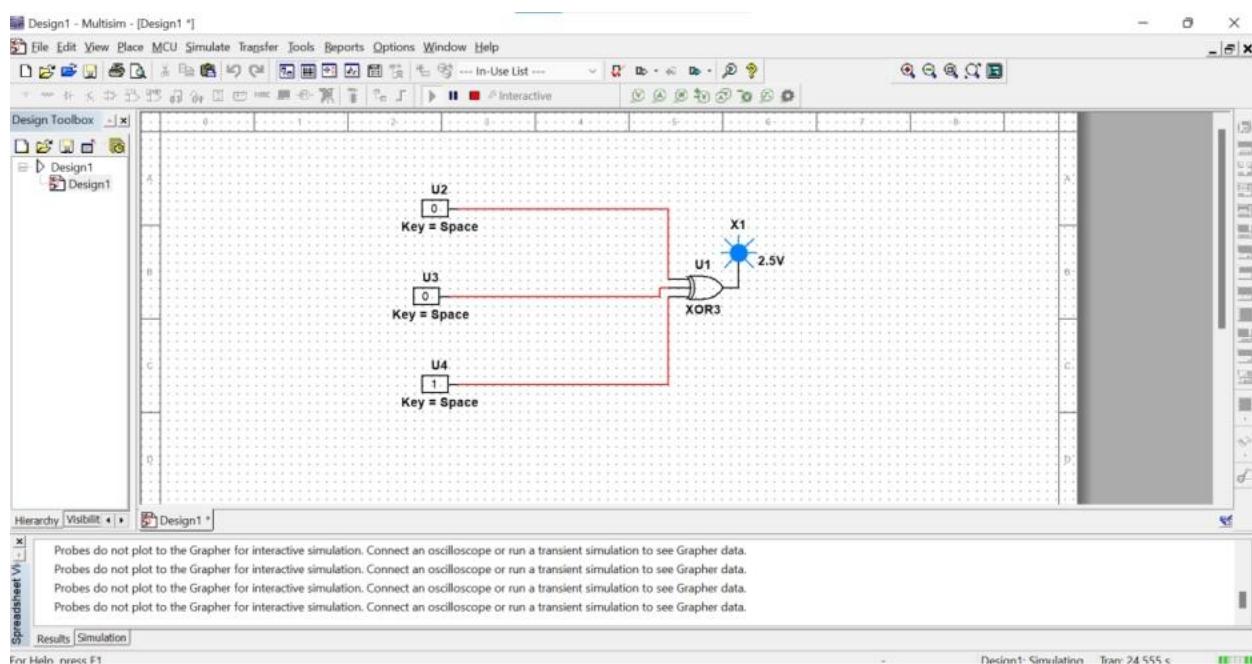
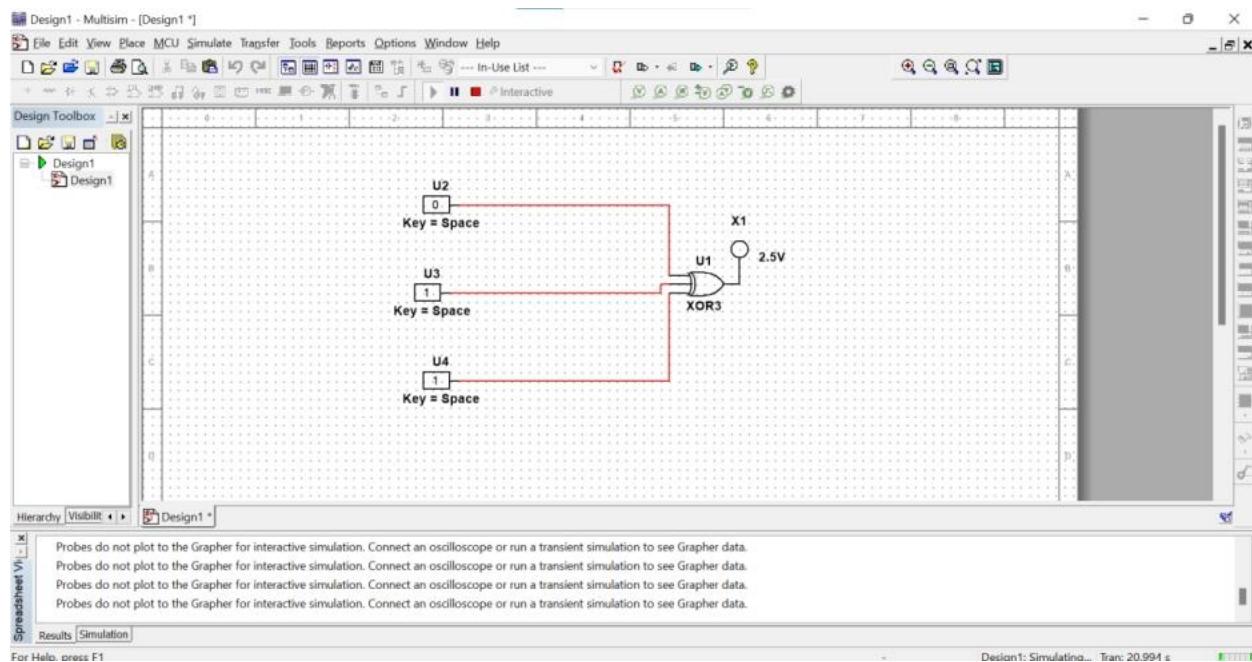
Results Simulation
For Help, press F1 Design2: Simulating... Tran: 6.995 s

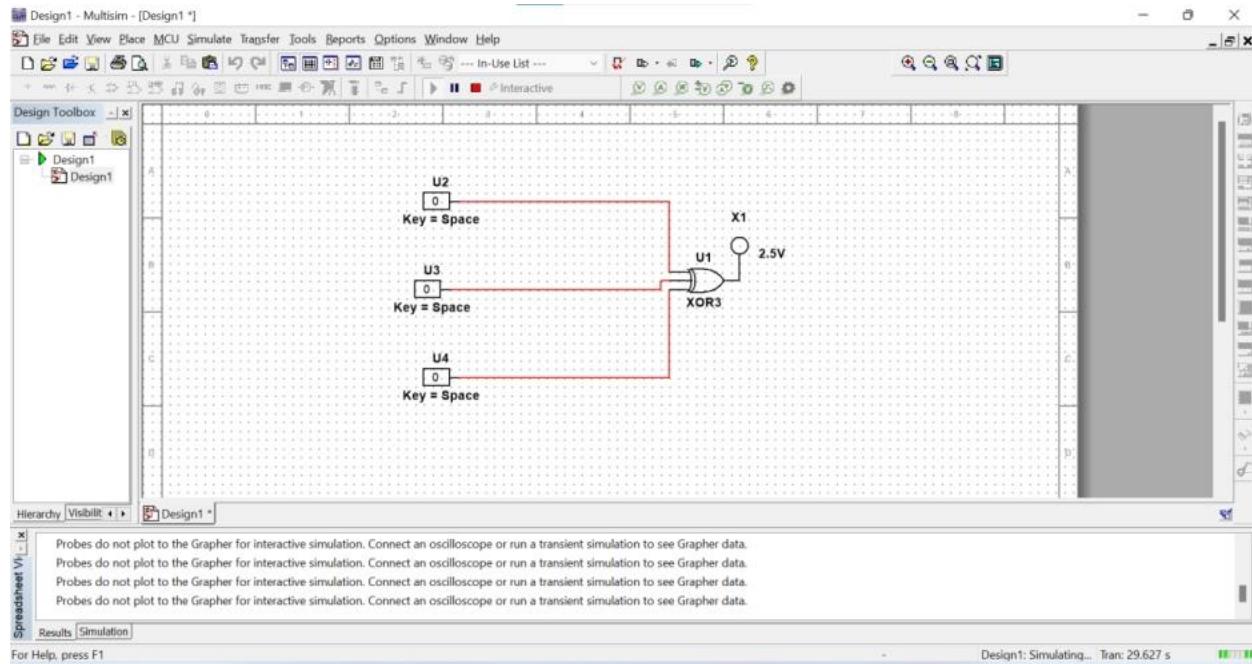


XOR 3:

X	Y	Z	OUTPUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

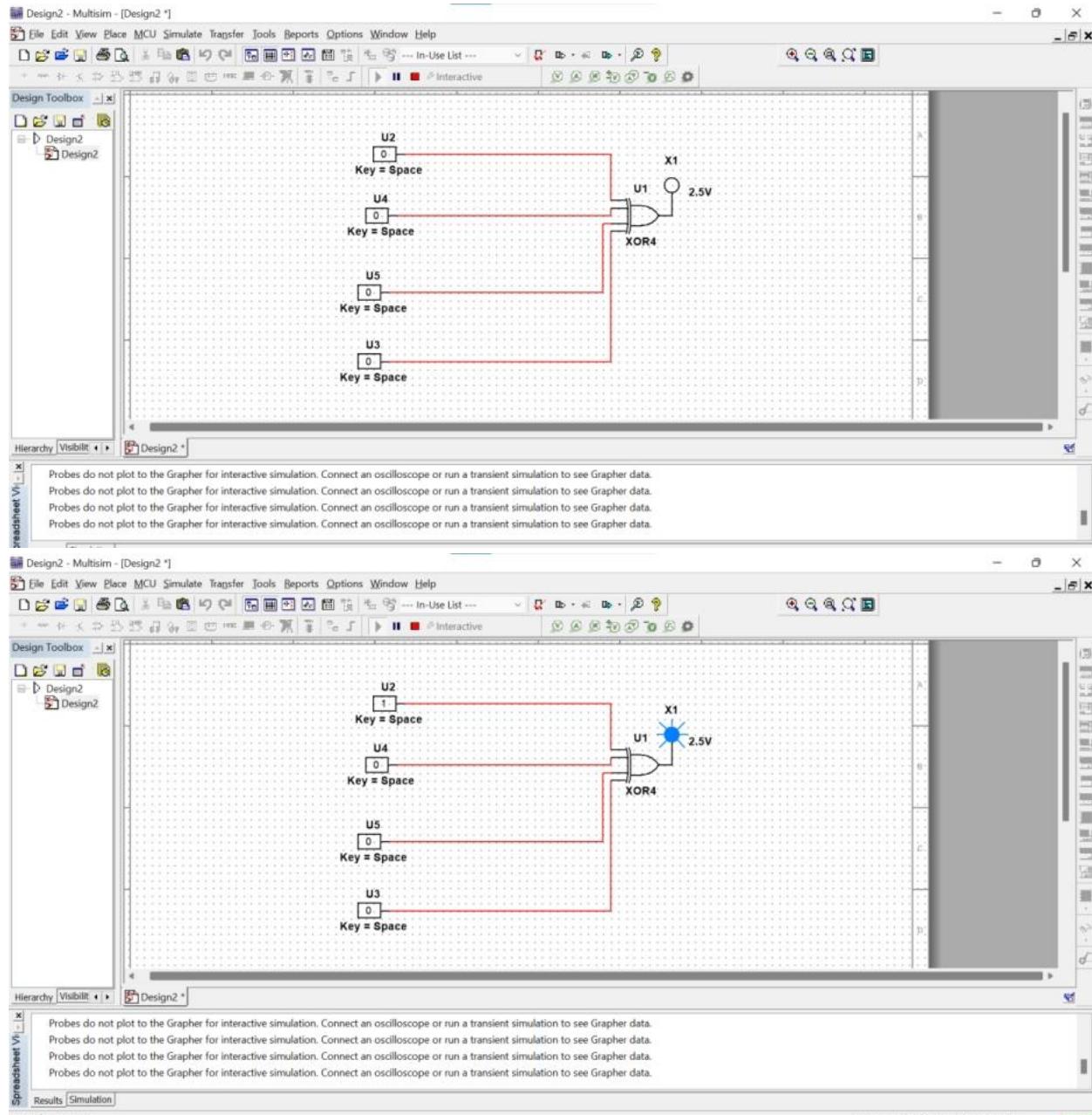


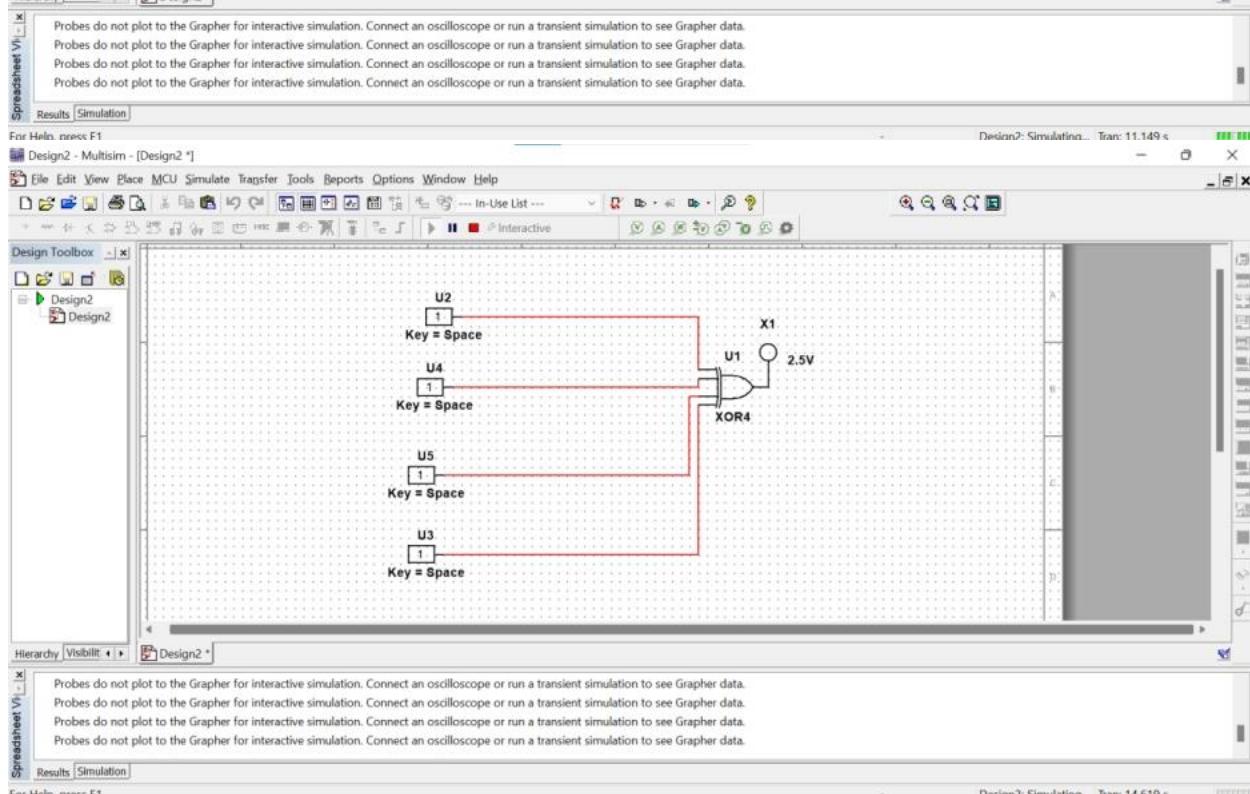
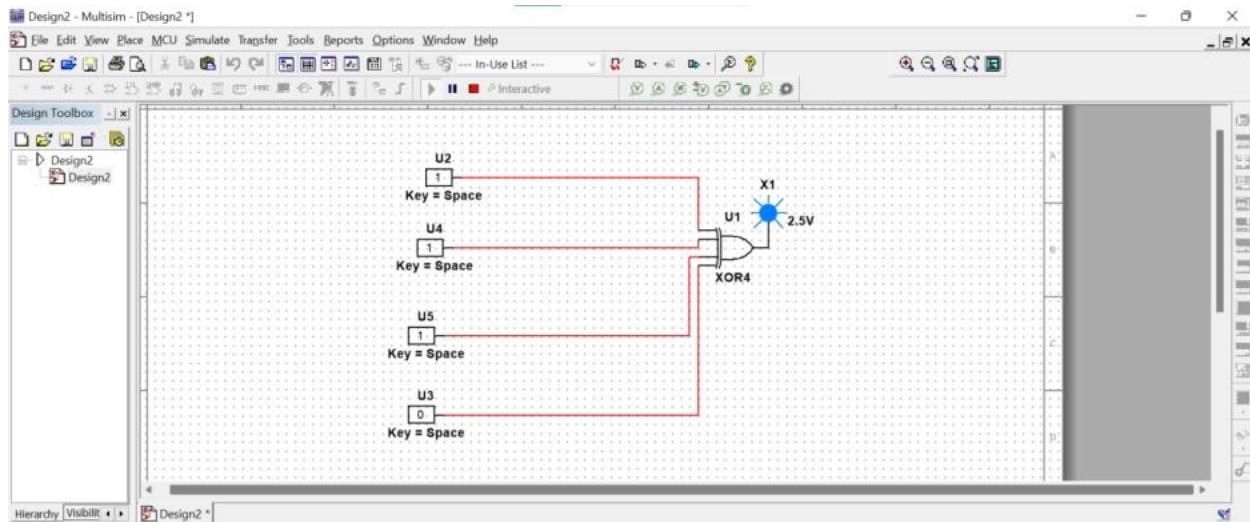


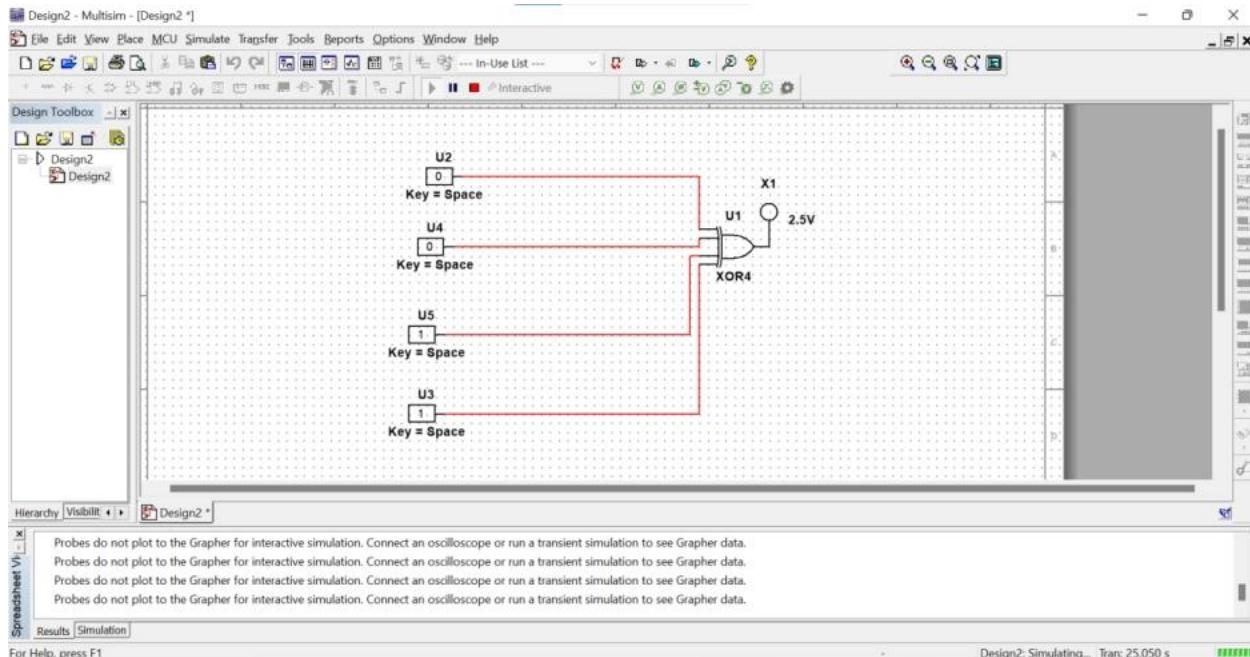


XOR 4:

W	X	Y	Z	OUTPUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



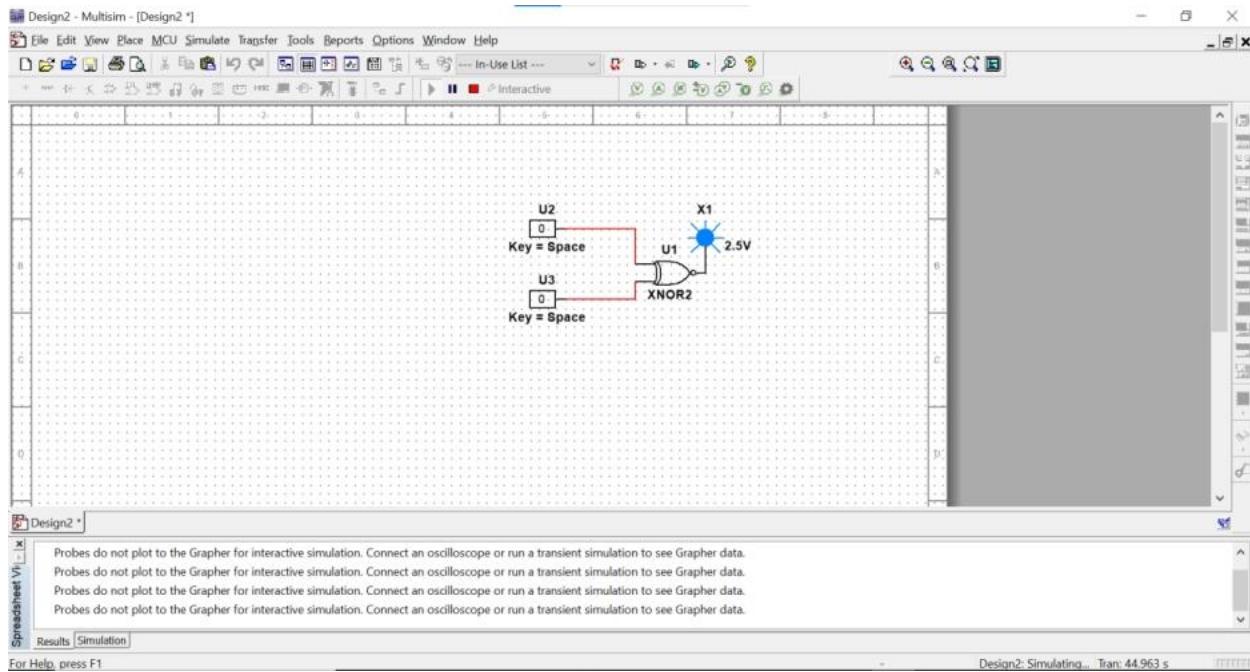


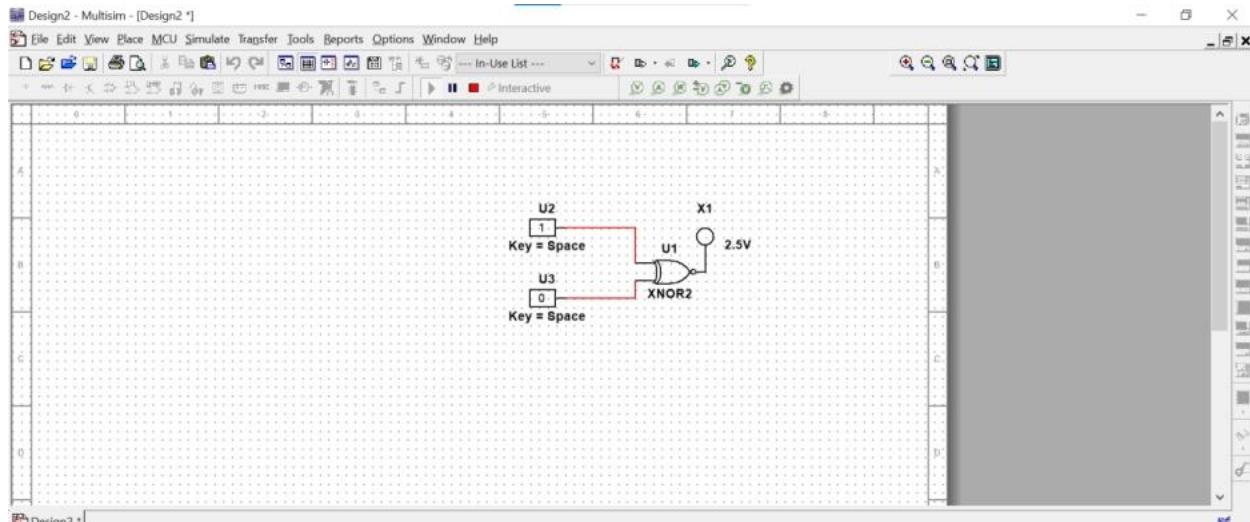


7. XNOR:

XNOR 2:

X	Y	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	1





Design2 *

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

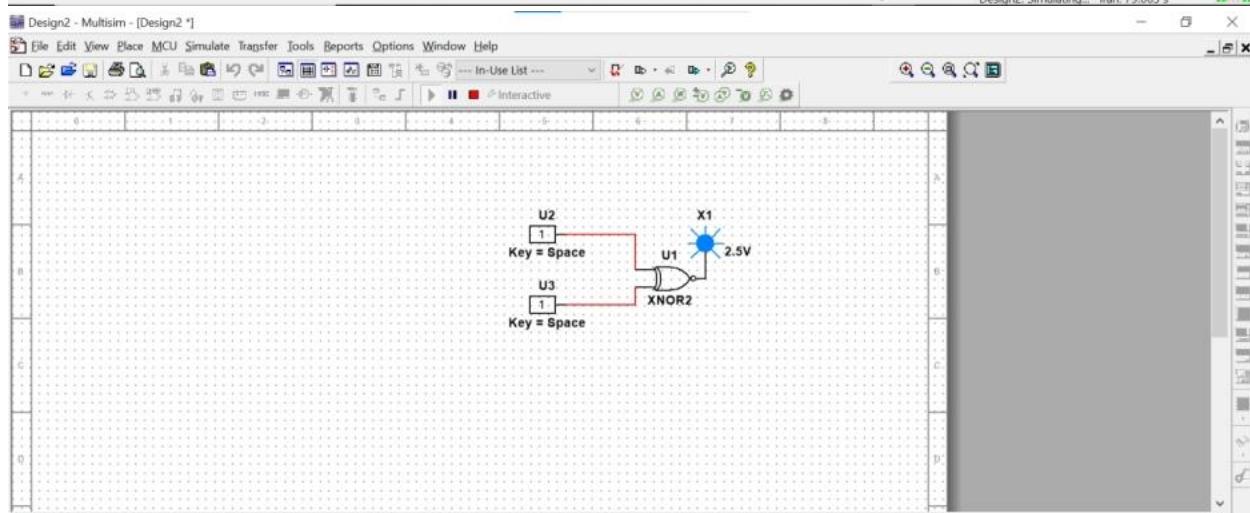
Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Results Simulation

Design2: Simulating... Tran: 79.063 s



Design2 *

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

Results Simulation

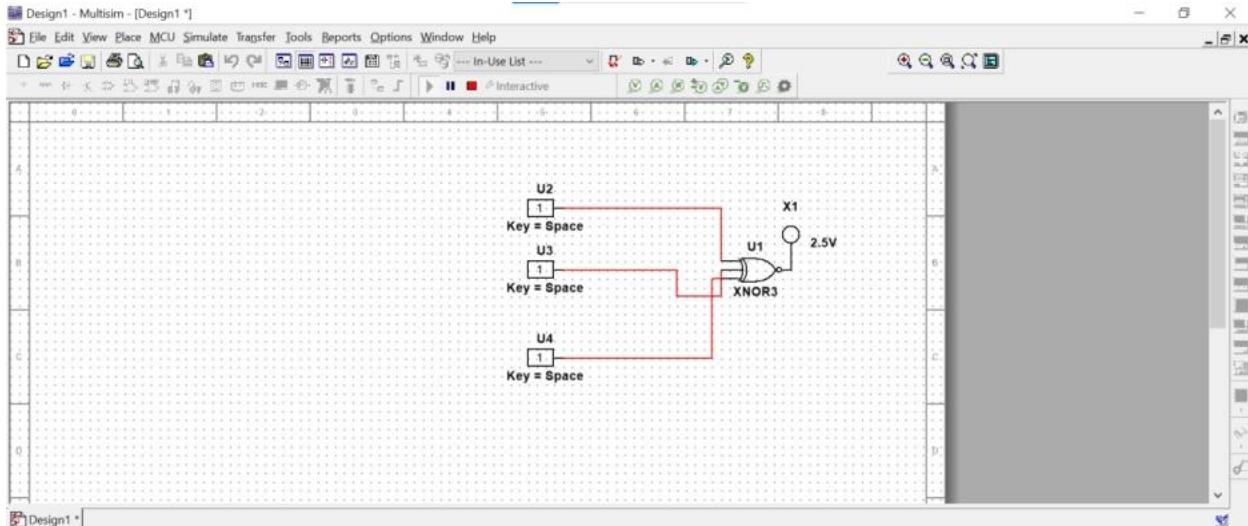
For Help, press F1

Design2: Simulating... Tran: 93.479 s

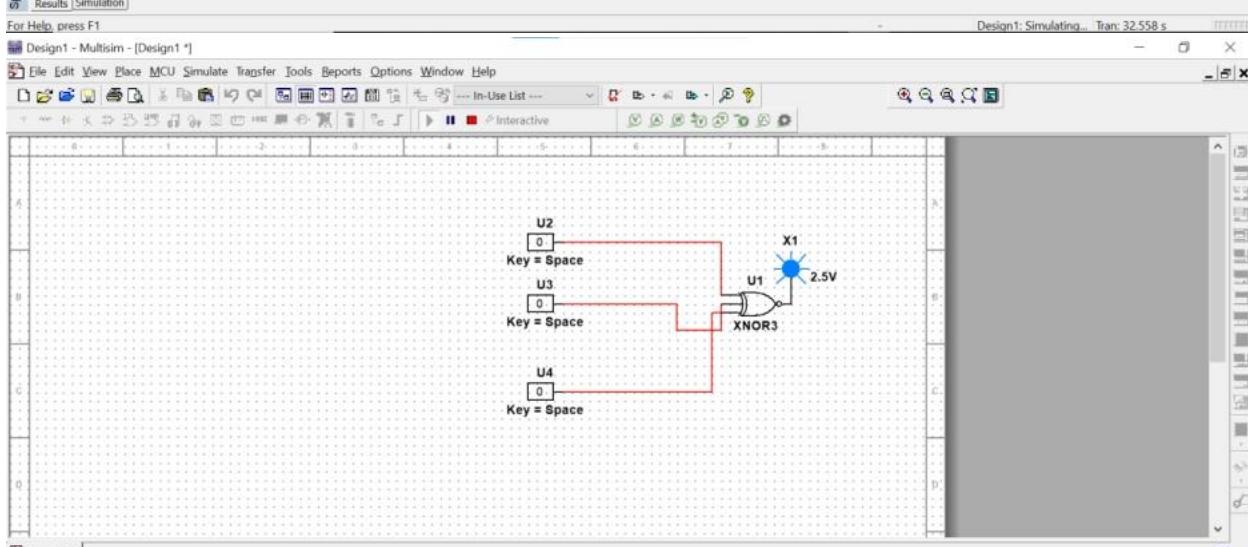
XNOR 3:

X	Y	Z	OUTPUT
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1

1	1	1	0
---	---	---	---

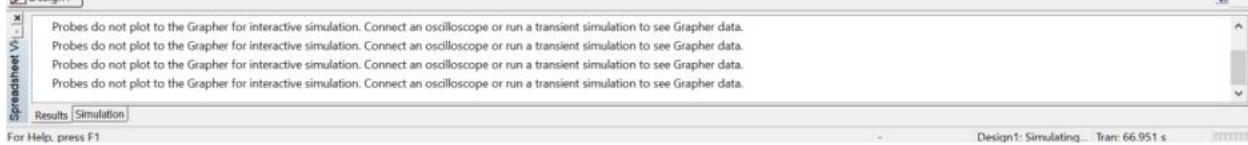
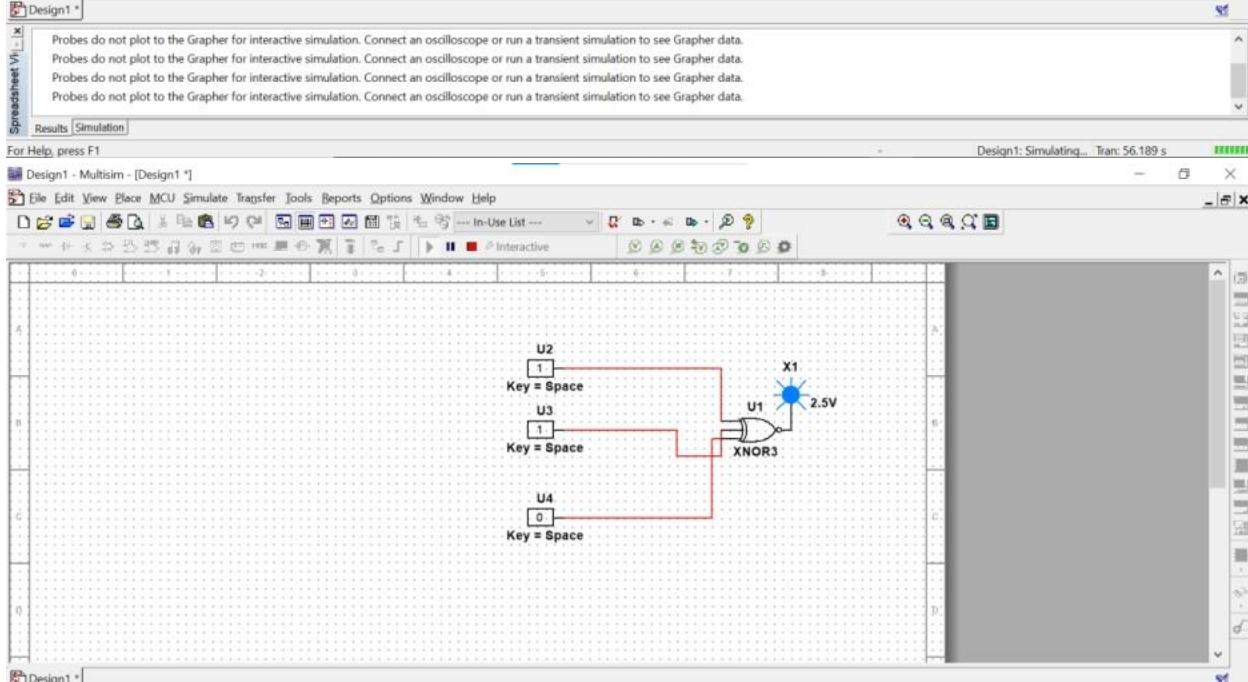
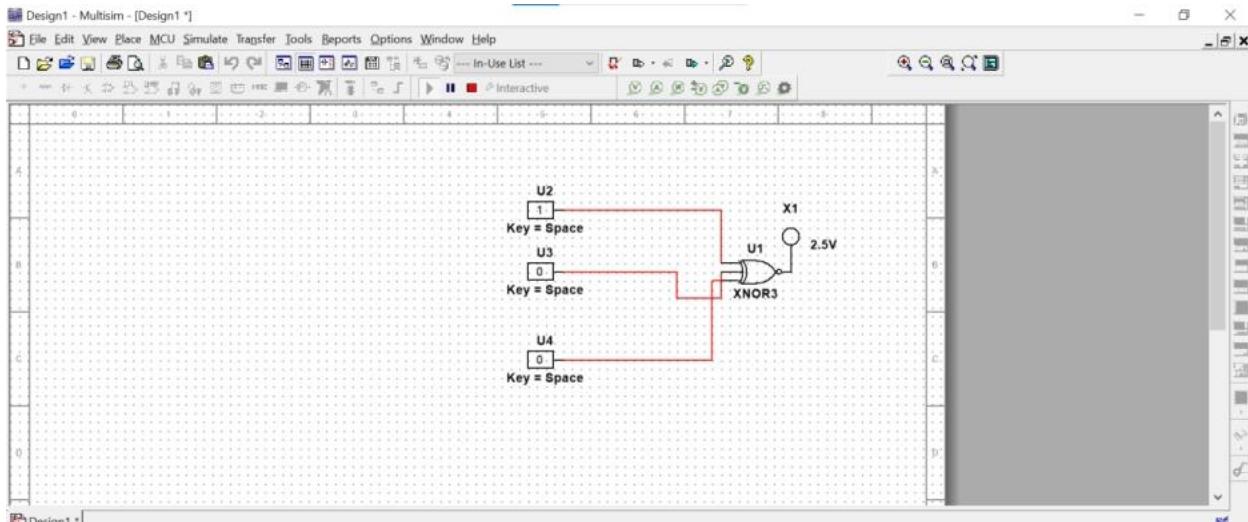


Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.



Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.
 Probes do not plot to the Grapher for interactive simulation. Connect an oscilloscope or run a transient simulation to see Grapher data.

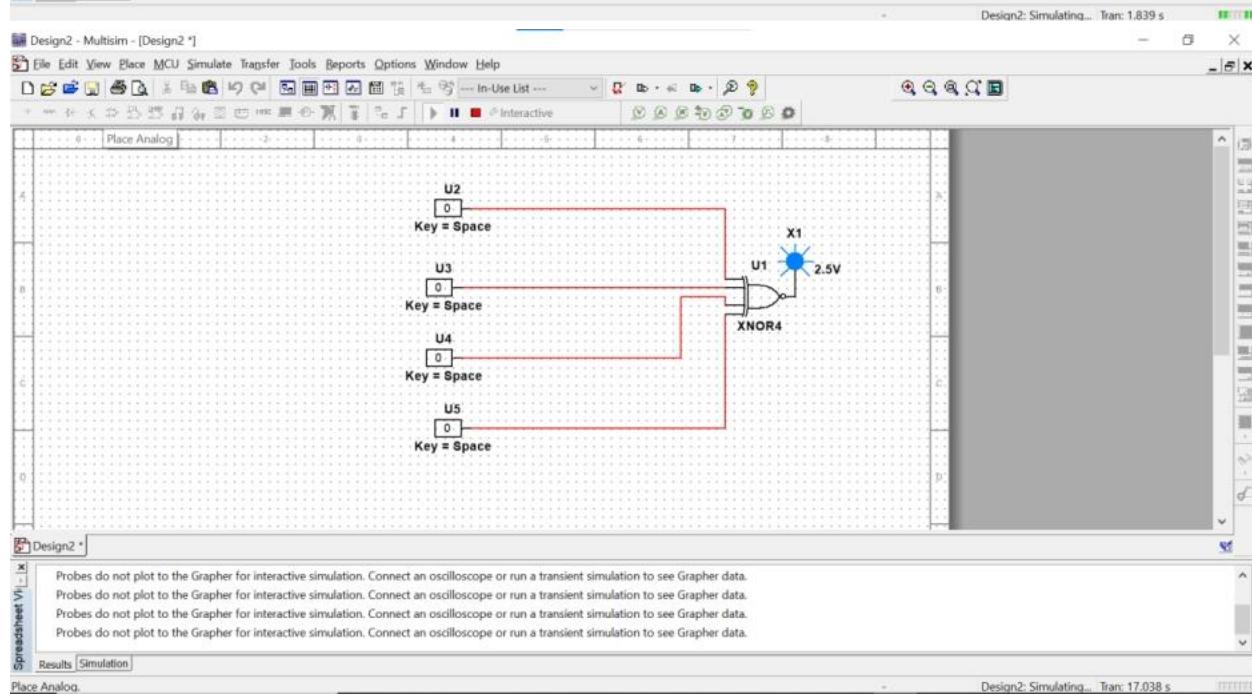
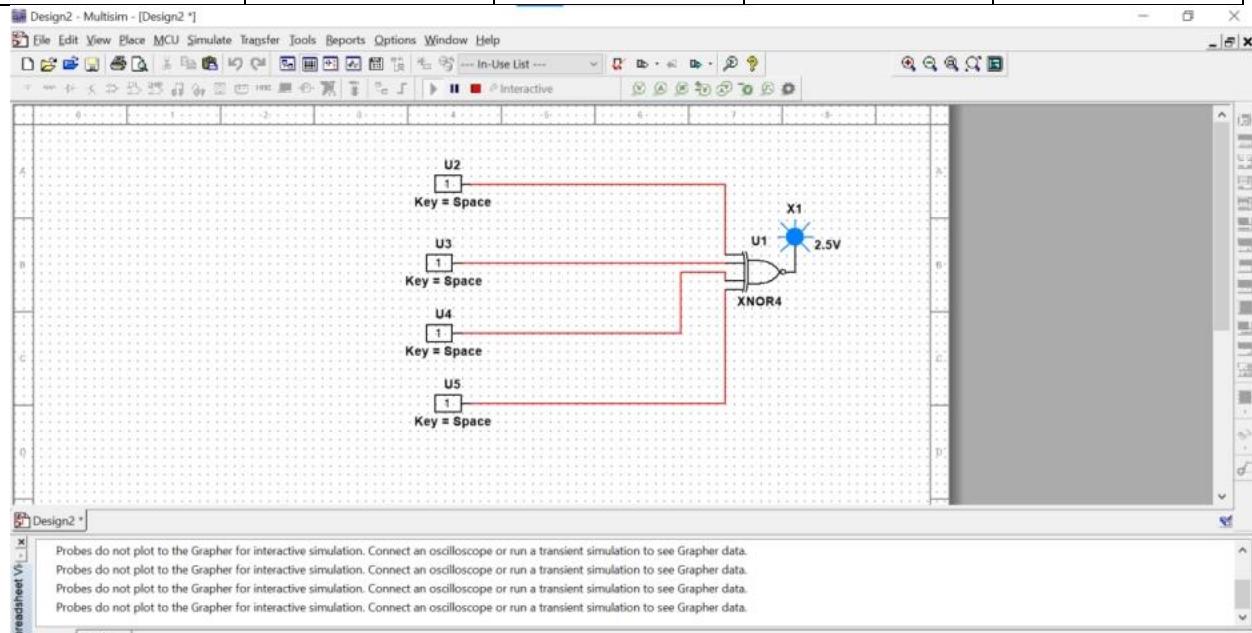
Design1: Simulating... Tran: 44.559 s

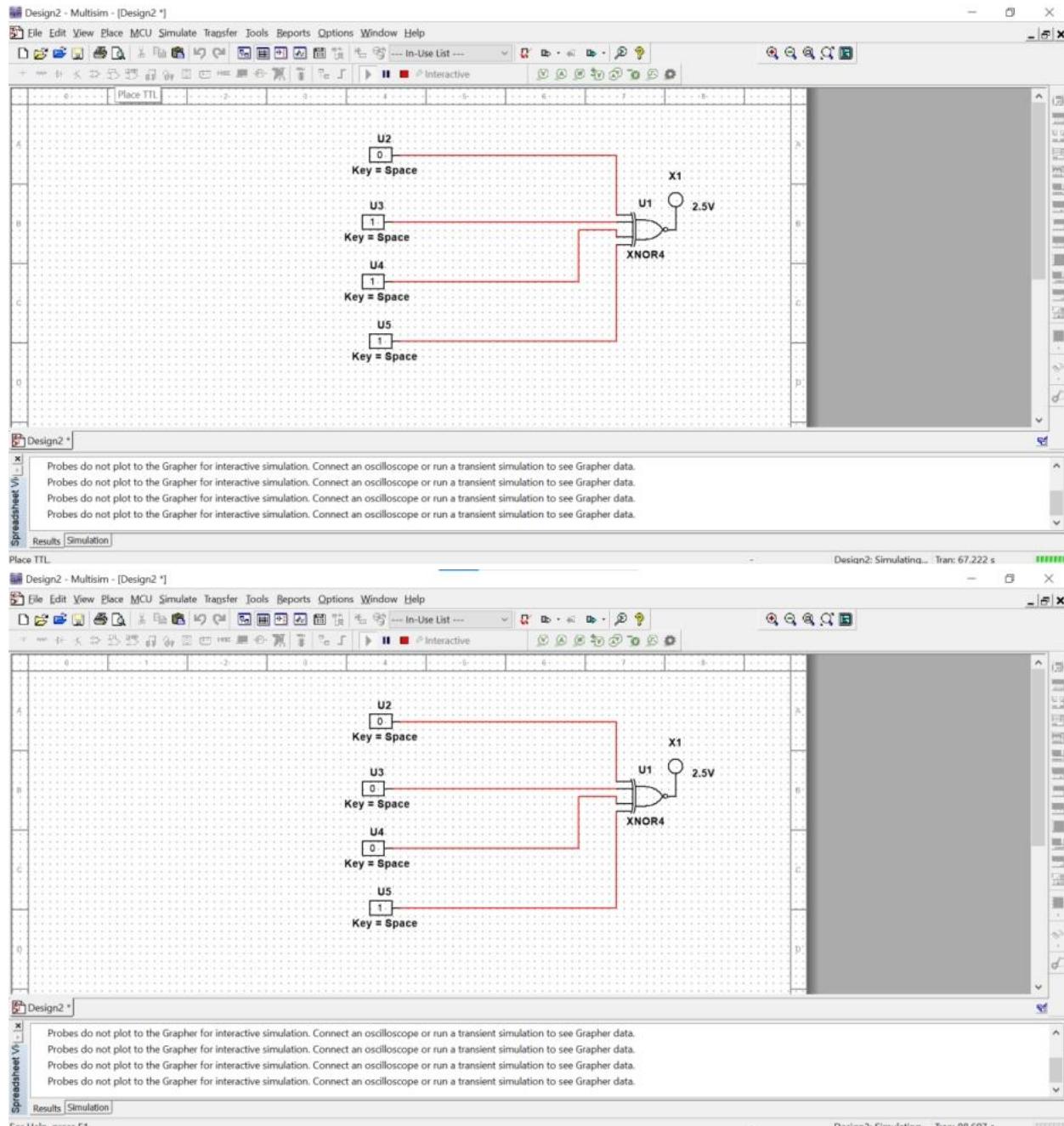


XNOR 4:

W	X	Y	Z	OUTPUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1

0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

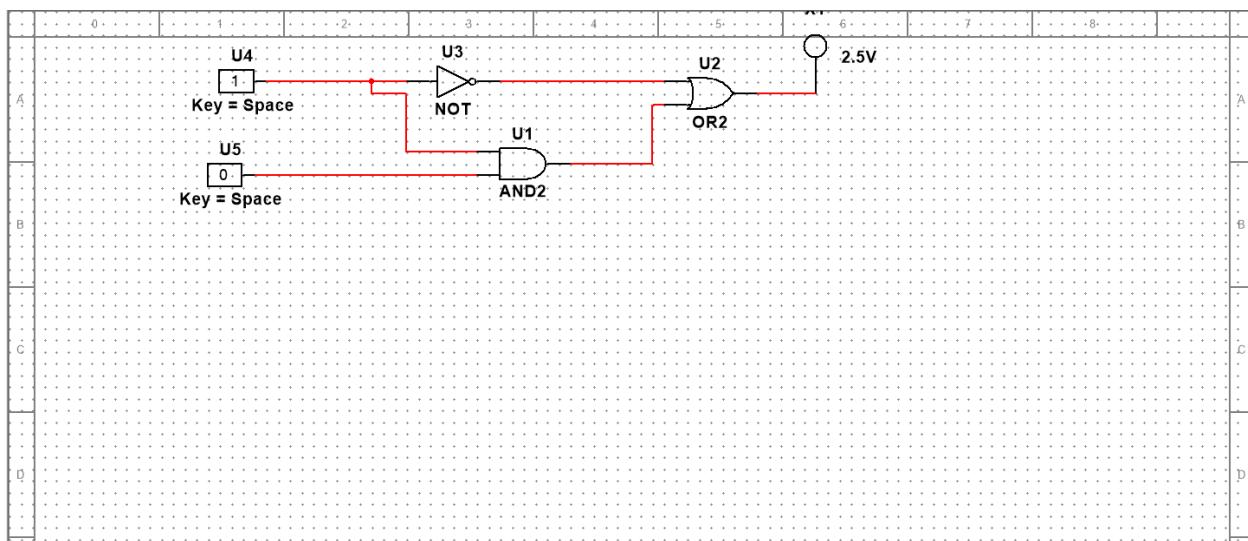
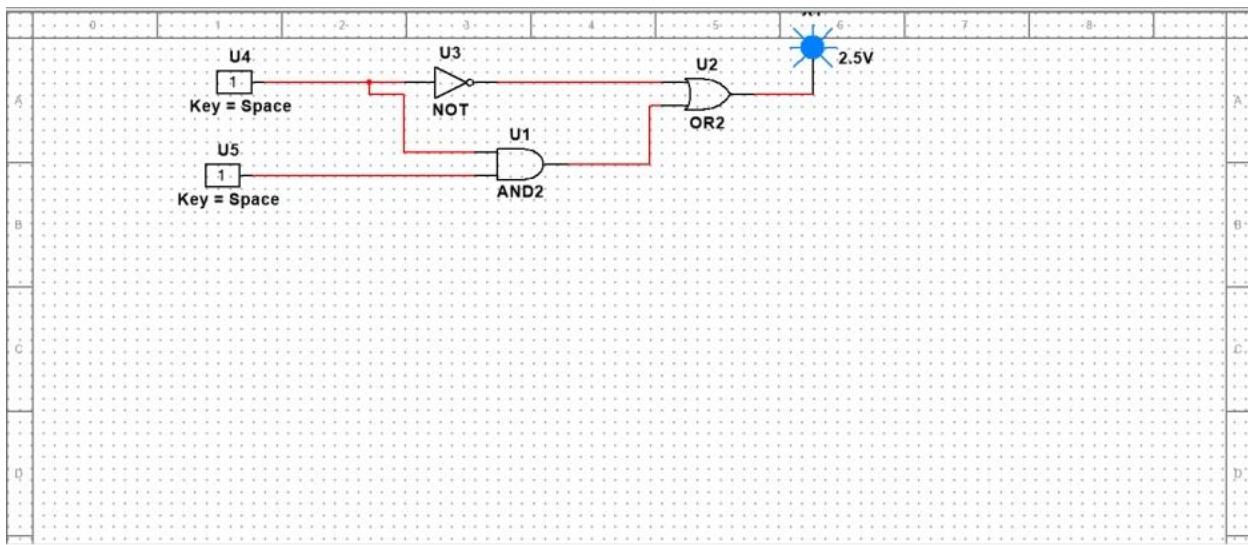




Lab report 4

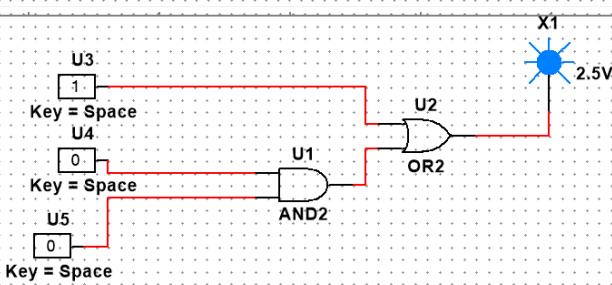
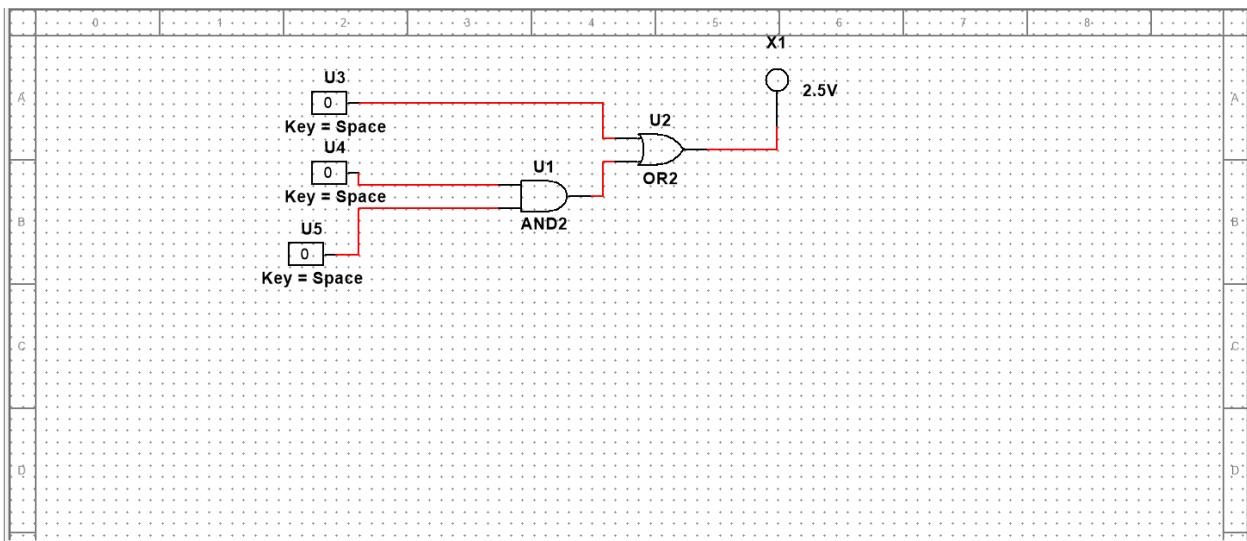
Expression: $Y = A \cdot B + \neg A$

A	B	$A \cdot B$	A'	$Y = A \cdot B + A'$
0	0	0	1	1
0	1	0	1	1
1	0	0	0	0
1	1	1	0	1



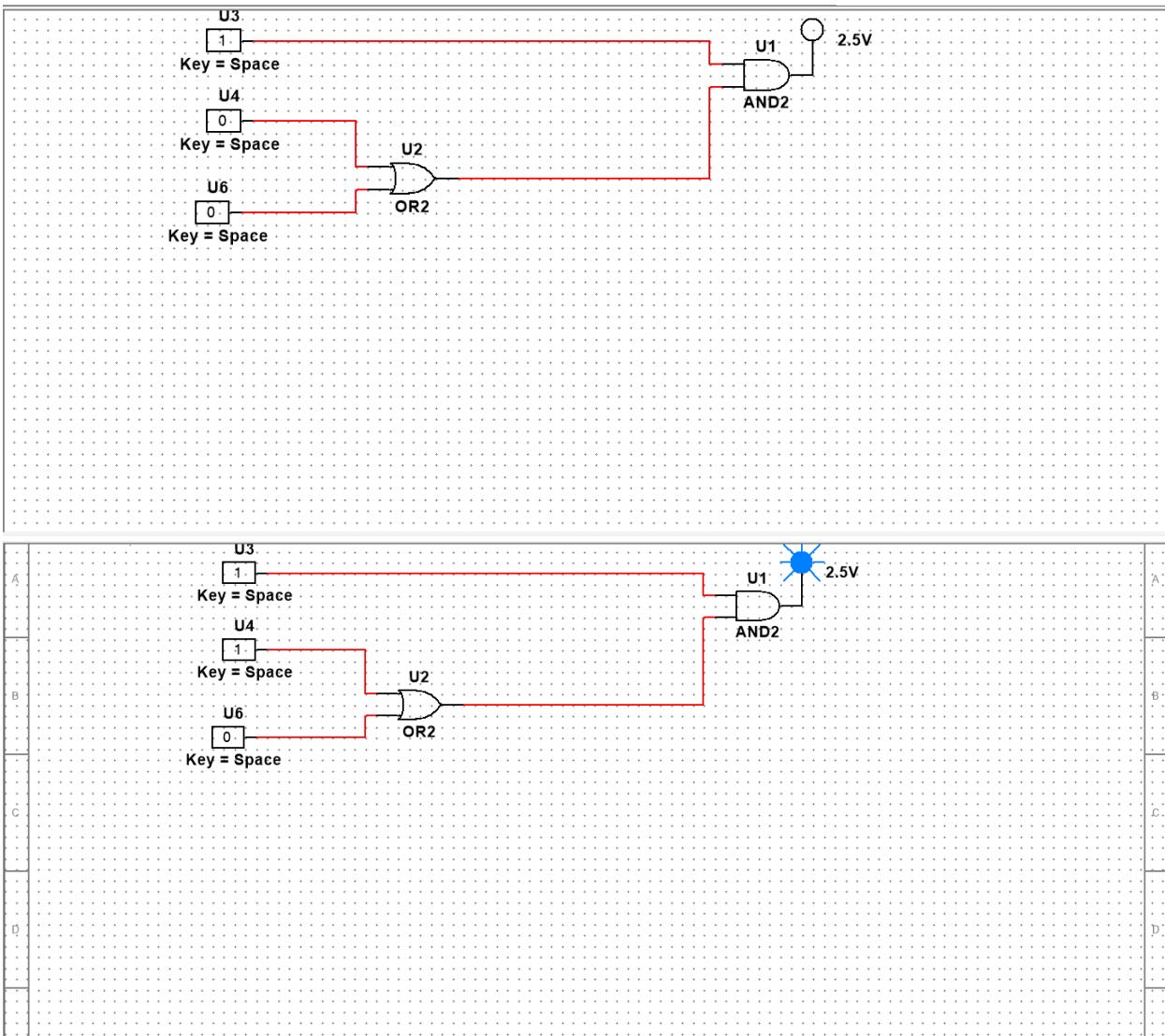
Expression: $Y = A + B \cdot C$

A	B	C	B.C	A+B.C
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Expression: $Y = A \cdot (B + C)$

A	B	C	B+C	A(B+C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1



Lab number 5

Boolean Algebra: Verification and Simplification of Expressions Using NI Multisim

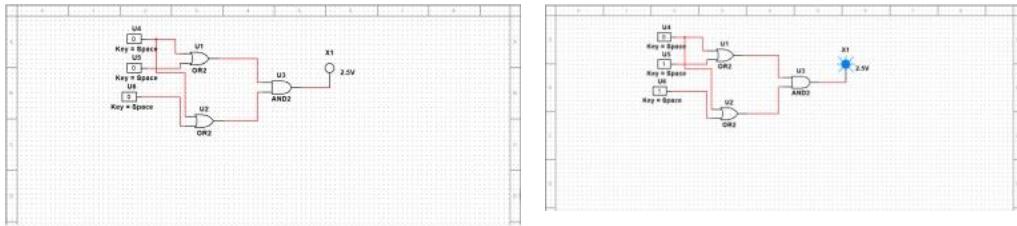
Boolean Expressions and Corresponding Circuits:

1. Expression 1: $Y = (A + B)(A + C)$

- Circuit Components: AND gate, OR gate

A	B	C	A+B	A+C	(A+B)(A+C)
0	0	1	0	1	0
0	0	0	0	0	0
0	1	1	1	1	1
0	1	0	1	0	0

1	0	1	1	1	1
1	0	0	1	1	1
1	1	1	1	1	1
1	1	0	1	1	1



Simplification

$$Y = (A + B)(A + C)$$

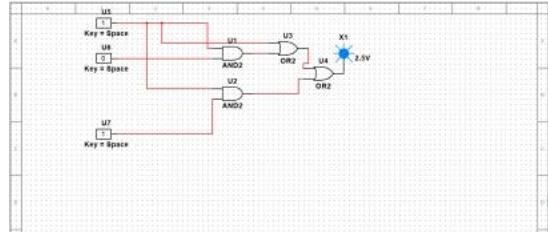
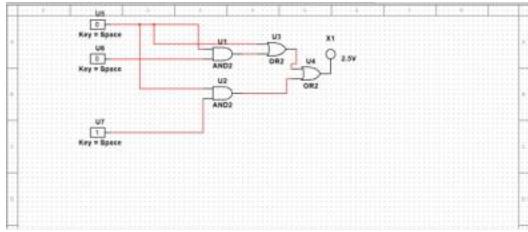
$$=A+BC$$

A	B	C	BC	A+BC
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

2. Expression 2: $Y = A + AB + AC$

- Circuit Components: OR gate

A	B	C	AB	A+AB	AC	A+AB+ AC
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	0	1	0	1
1	0	1	0	1	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	1



Simplification

$$Y = A + AB + AC$$

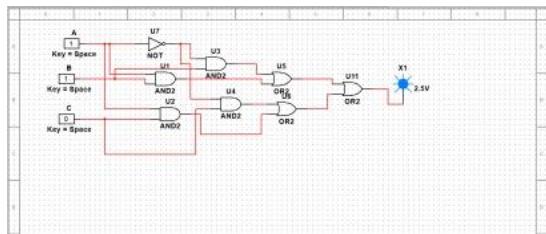
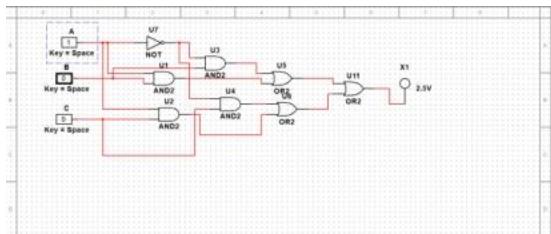
$$= A + AC \text{ (by absorption law)}$$

$$= A \text{ (by absorption law)}$$

3. Expression 3: $Y = AB + A'B + AC + A'C$

- Circuit Components: AND gate, OR gate, NOT gate

A	B	C	A'	AB	$A'B$	$AB+A'B$	AC	$A'C$	$AC+A'C$	$(AB+A'B)+(AC+A'C)$
0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	1	1	1
0	1	0	1	0	1	1	0	0	0	1
0	1	1	1	0	1	1	0	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	1	0	1	1
1	1	0	0	1	0	1	0	0	0	1
1	1	1	0	1	0	1	1	0	1	1



Simplification

$$Y = AB + A'B + AC + A'C$$

$$= B(A+A') + C(A+A') \text{ (Inverse law)}$$

$$= B+C$$

Expression 4: $Y = (A + B)(\neg A + C)(\neg B + D)$

- Circuit Components: AND gate, OR gate

A	B	C	D	A'	B'	$A+B$	$A'+C$	$B'+D$	$(A+B)(A'+C)$	$(A+B)(A'+C)(B'+D)$
0	0	0	0	1	1	0	1	1	0	0

0	0	0	1	1	1	0	1	1	0	0
0	0	1	0	1	1	0	1	1	0	0
0	0	1	1	1	1	0	1	1	0	0
0	1	0	0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1	1	1	1
0	1	1	0	1	0	1	1	0	1	0
0	1	1	1	1	1	0	1	1	1	1
1	0	0	0	0	1	1	0	1	0	0
1	0	0	1	0	1	1	0	1	0	0
1	0	1	0	0	1	1	1	1	1	1
1	0	1	1	0	1	1	1	1	1	1
1	1	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	1	0	0
1	1	1	0	0	0	1	1	0	1	0
1	1	1	1	0	0	1	1	1	1	1

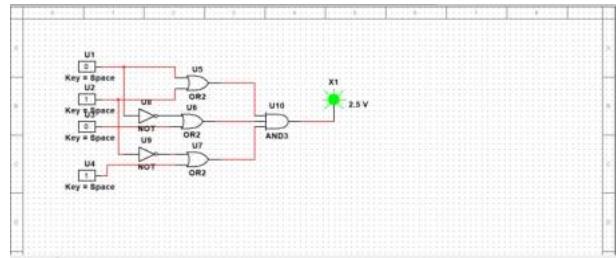
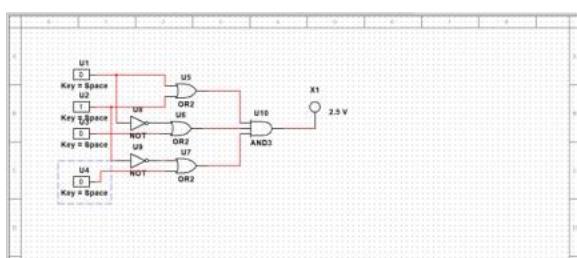
Simplification

$$Y = (A + B) (\neg A + C) (\neg B + D)$$

$$= AA' + AC + BA' + BC (B' + D)$$

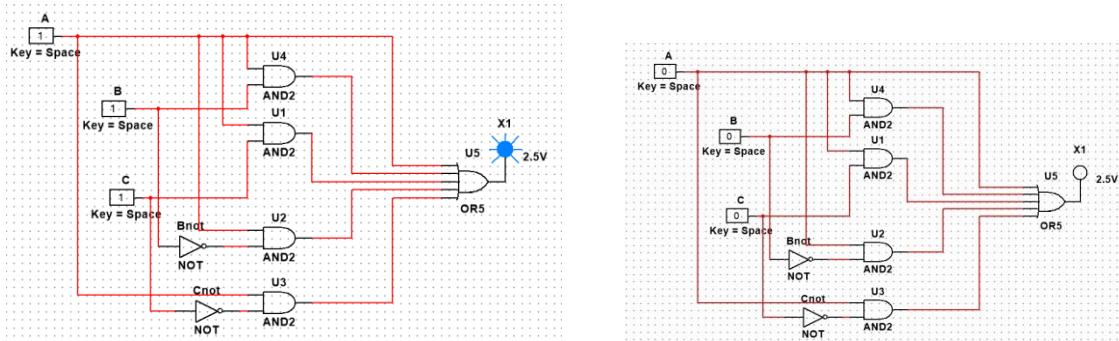
$$= ACB' + BA'B' + BCB' + ACD + BA'D + BCD$$

$$= ACB' + ACD + BA'D + BC$$



5. EXPRESSION: A+AB+AC+AB'+AC'

A	B	C	B'	C'	AB	AC	AB'	AC'	RESULT
0	0	0	1	1	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0
1	0	0	1	1	0	0	1	1	1
1	0	1	1	0	0	1	1	0	1
1	1	0	0	1	1	0	0	1	1
1	1	1	0	0	0	1	1	0	1



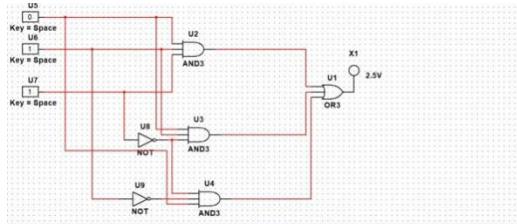
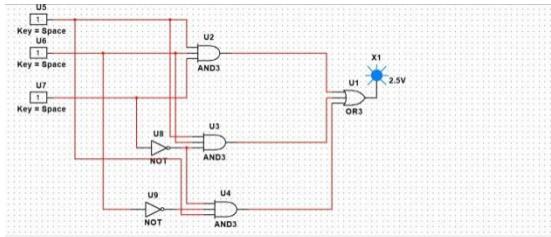
Lab number 6

Verification and Simplification Using Karnaugh Maps (K-Maps) and NI Multisim

Boolean Expressions and Corresponding Circuits:

No.	Boolean Expression	Components Needed
1.	$Y = AB\bar{C} + ABC + A\bar{B}\bar{C}$	AND, OR, NOT Gates
2.	$Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + ABC$	AND, OR, NOT Gates
3.	$Y = \sum m(0,1,2)$	AND, OR, NOT Gates
4.	$Y = \sum m(0,1,3,4,5,7)$	AND, OR, NOT Gates
5.	$Y = \sum m(1,3,4,6)$	AND, OR, NOT Gates

$$1 \quad Y = AB\bar{C} + ABC + A\bar{B}\bar{C}$$



A	B	C	B'	C'	ABC'	ABC	AB'C'	ABC' + ABC + AB'C'
0	0	0	1	1	0	0	0	0 m0
0	0	1	1	0	0	0	0	0 m1
0	1	0	0	1	0	0	0	0 m2
0	1	1	0	0	0	0	0	0 m3
1	0	0	1	1	0	0	1	1 m4
1	0	1	1	0	0	0	0	0 m5

1	1	0	0	1	1	0	0	1 m6
1	1	1	0	0	0	1	0	1 m7

K-Map

	B'		B	
A'	u m0	u m1	u m3	u m2
A	1 m4	0 m5	1 m7	1 m6

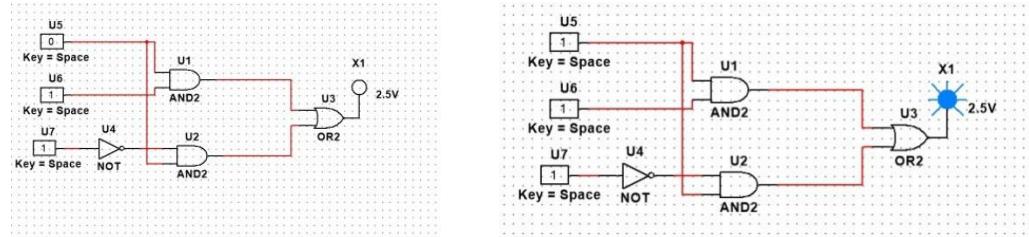
C' C C'

$$=(xy'z') + (xyz') = xz'$$

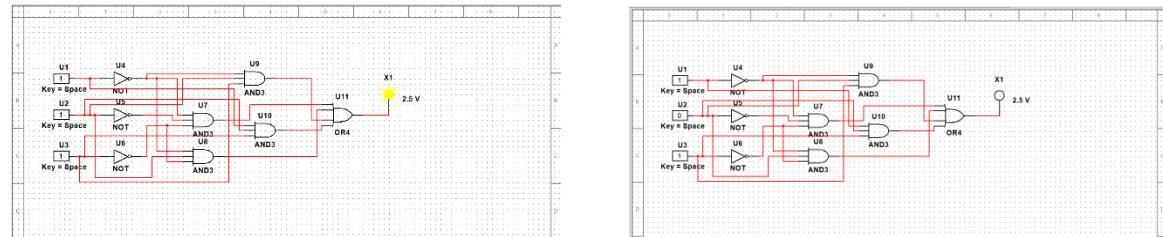
$$=(xyz') + (xyz) = xy$$

$$F(x,y,z) = xz' + xy$$

Simplification



$$2. \quad Y = \neg A \neg B \neg C + \neg A B \neg C + A \neg B C + A B C$$



A	B	C	A'	B'	C'	$A'B'C'$	$A'BC'$	$AB'C$	ABC	$A'B'C' + A'BC' + AB'C + ABC$
0	0	0	1	1	1	1	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0
0	1	0	1	0	1	0	1	0	0	1
0	1	1	1	0						
1	0	0	0	1	1	0	0	0	0	0
1	0	1	0	1	0	0	0	1	0	1
1	1	0	0	0	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1

K-Map

	B'		B	
A'	u m0	u m1	u m3	1 m2
A	0 m4	1 m5	1 m7	0 m6

C' C C'

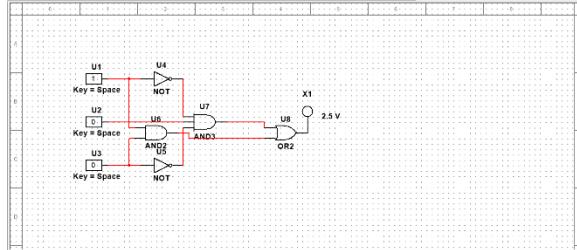
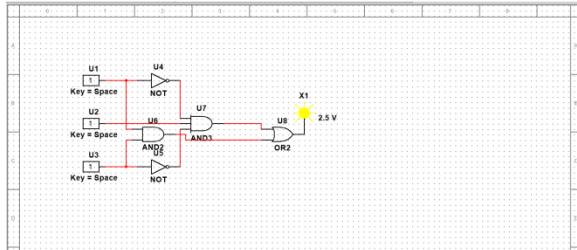
C'

C

C'

$$F(x,y,z) = AC + A'B'C'$$

Simplified

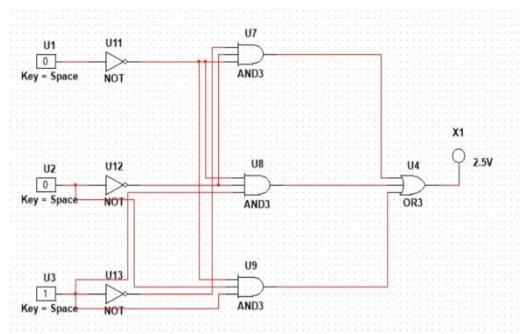
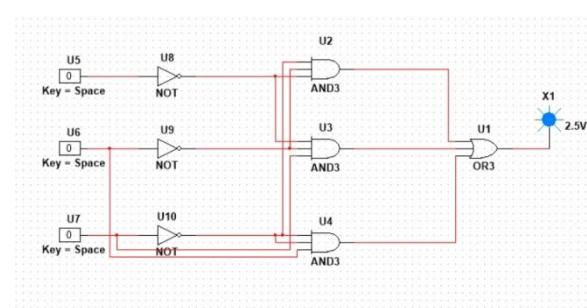


$$\text{Expression No 3: } Y = \sum m(0,1,2)$$

$$\text{Expression: } X'Y'Z' + X'Y'Z + X'YZ$$

Truth Table:

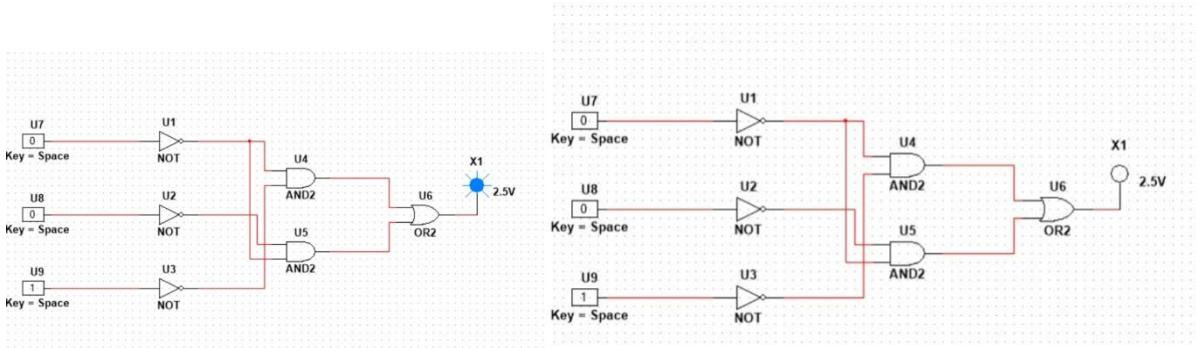
X	Y	Z	X'	Y'	Z'	$X'Y'Z' + X'Y'Z + X'YZ$	$X'Z' + X'Y'$
0	0	0	1	1	1	1	1
0	0	1	1	1	0	1	1
0	1	0	1	0	1	1	1
0	1	1	1	0	0	0	0
1	0	0	0	1	1	0	0
1	0	1	0	1	0	0	0
1	1	0	0	0	1	0	0
1	1	1	0	0	0	0	0



K-Map

	B'	B	
A'	1 m0	1 m1	0 m2
A	0 m4	0 m5	0 m6
	C'	C	

Simplified Expression: $X'Z' + X'Y'$

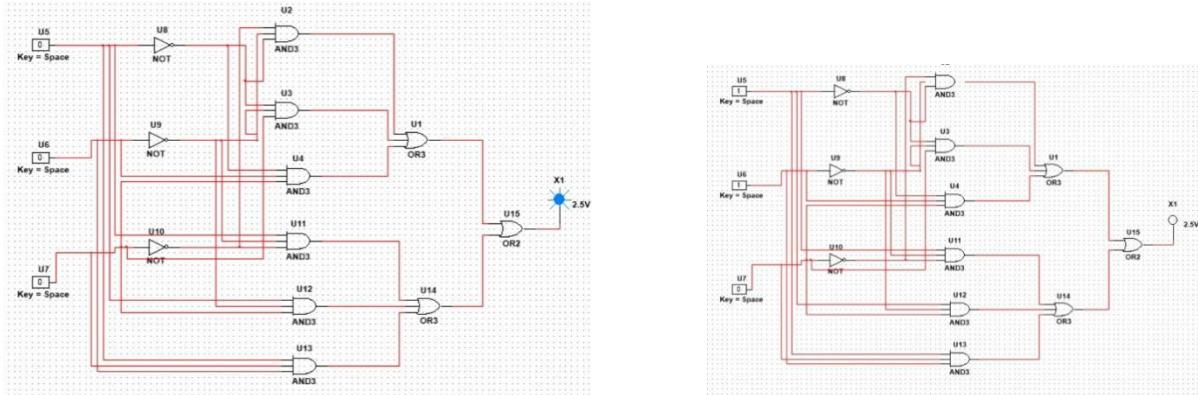


$$\text{Expression No 4: } Y = \sum m(0,1,3,4,5,7)$$

$$\text{Expression: } X'Y'Z' + X'Y'Z + X'YZ + XY'Z' + XY'Z + XYZ$$

Truth Table: For proving.

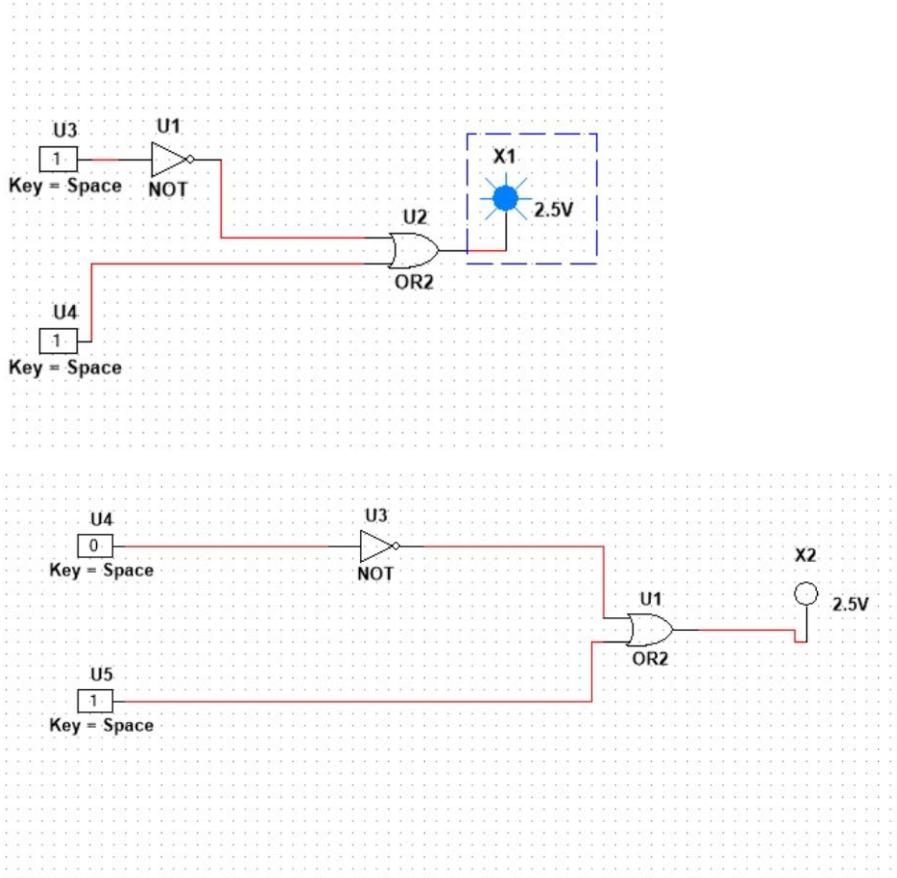
X	Y	Z	X'	Y'	Z'	$X'Y'Z' + X'Y'Z + X'YZ + XY'Z' + XY'Z + XYZ$	$Y' + Z$
0	0	0	1	1	1	1	1
0	0	1	1	1	0	0	0
0	1	0	1	0	1	0	0
0	1	1	1	0	0	1	1
1	0	0	0	1	1	0	0
1	0	1	0	1	0	1	1
1	1	0	0	0	1	0	0
1	1	1	0	0	0	1	1



K-Map

		B'	B			
		A'	1 m0	1 m1	1 m3	0 m4
		A	1 m4	1 m5	1 m7	0 m6
C'	C	C'				

Simplified Expression: Y' + Z

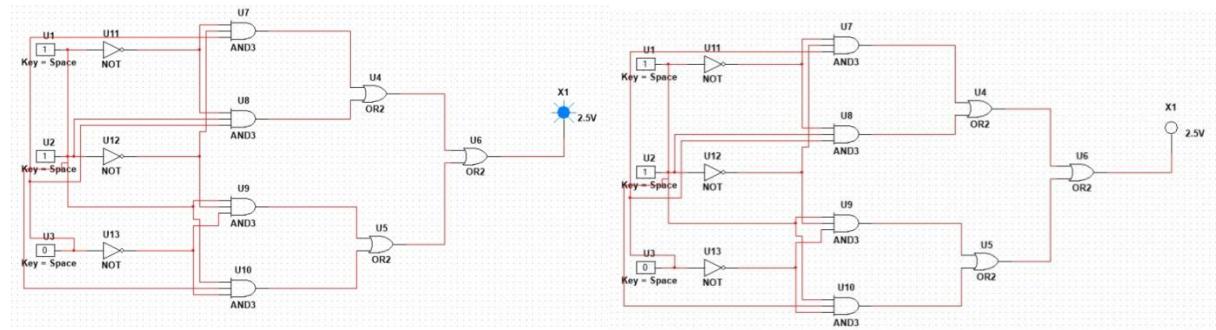


Expression No. 5: $Y = \sum m(1,3,4,6)$

Expression: $X'Y'Z + X'YZ + XY'Z' + XYZ'$

Truth Table: For proving.

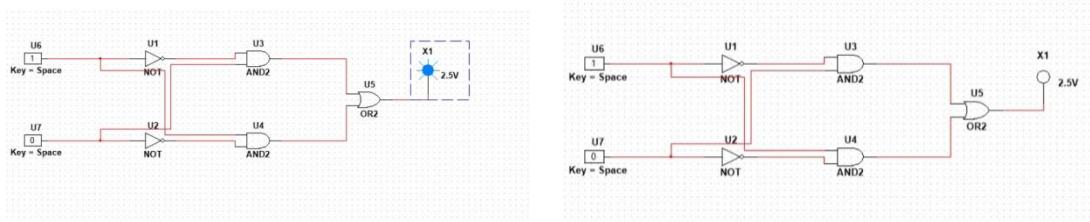
X	Y	Z	X'	Y'	Z'	$X'Y'Z + X'YZ + XY'Z' + XYZ'$	$X'Z + XZ'$
0	0	0	1	1	1	0	0
0	0	1	1	1	0	1	1
0	1	0	1	0	1	0	0
0	1	1	1	0	0	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	0	0	0
1	1	0	0	0	1	1	1
1	1	1	0	0	0	0	0



K-Map

		B'	B	
		A'	m4	m5
		A	1	0
			m4	m5
			1	0

Simplified Expression: $X'Z + XZ'$



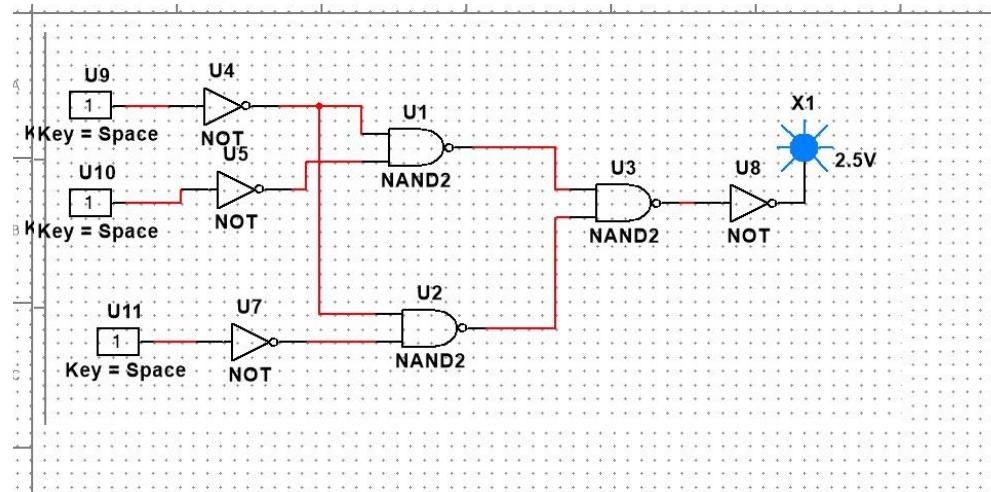
Lab Report: 07

Boolean Expressions and Corresponding Circuits:

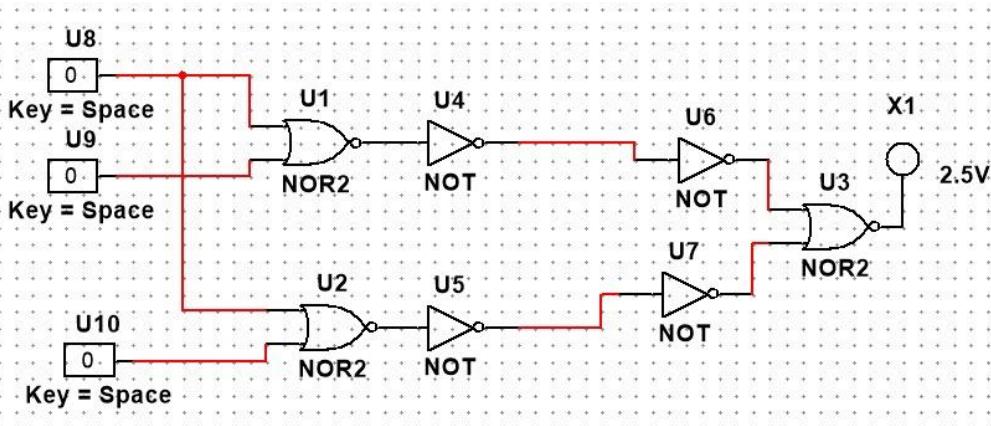
- Expression 1: $Y = (A + B)(A + C)$ implement using
 - NAND gates
 - NOR gates

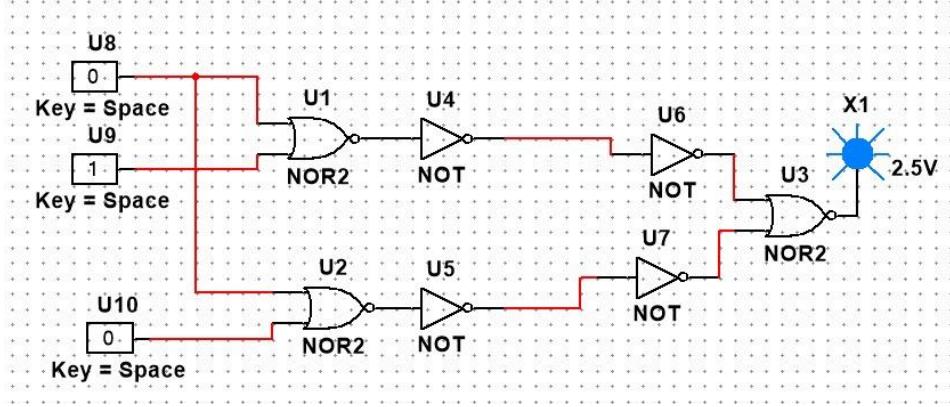
A	B	C	A+B	A+C	$(A + B)(A + C)$
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1

1. NAND gate:



2. NOR gate:

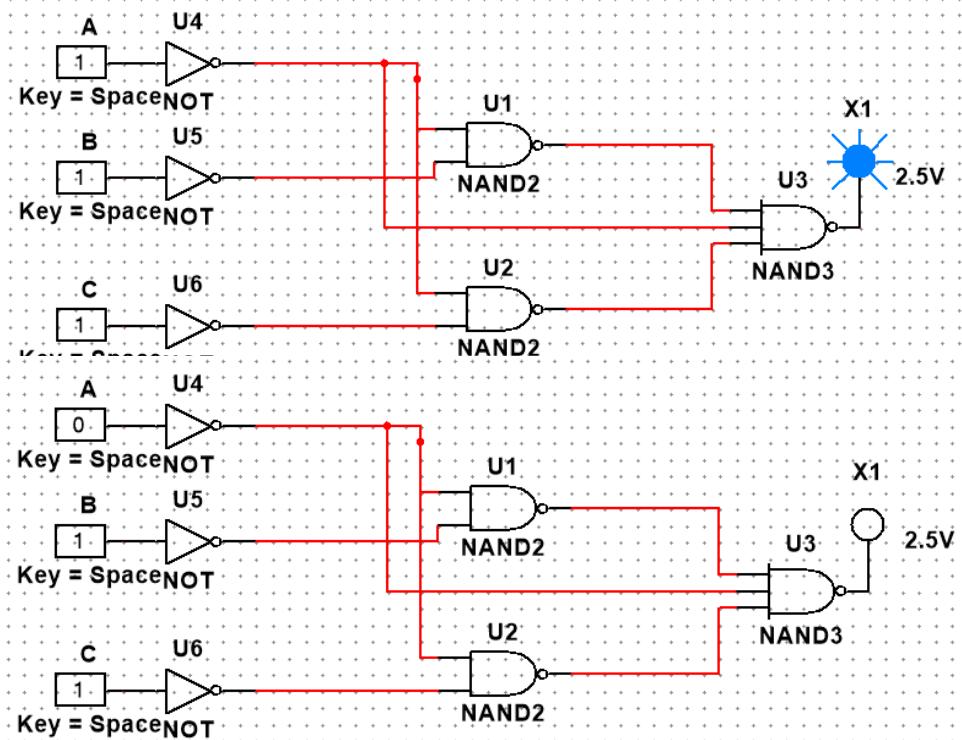




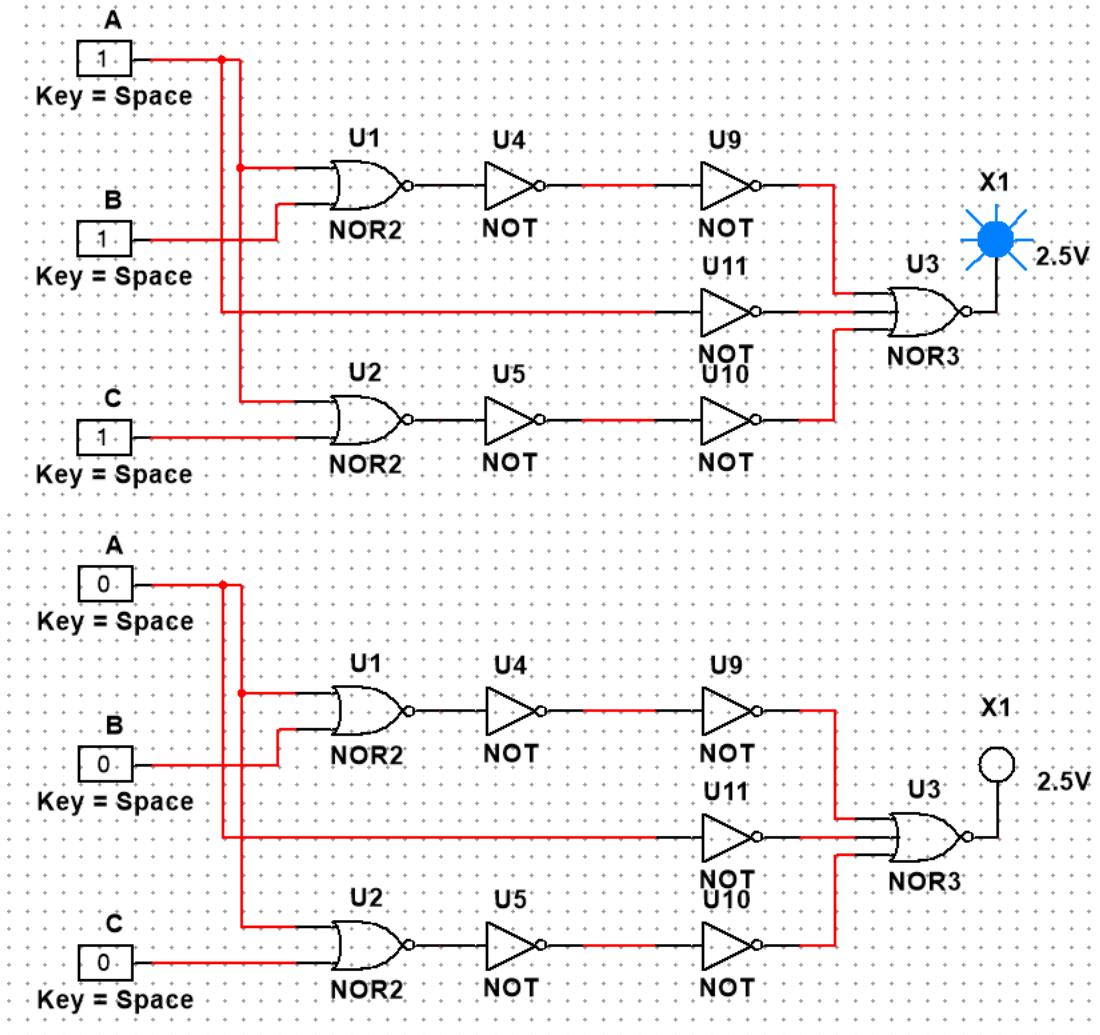
- Expression 2: $Y = A + AB + AC$
 - NAND gates
 - NOR gates

A	B	C	A.B	A.C	A+AB+AC
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

1. NAND gate:



2. NOR gate:

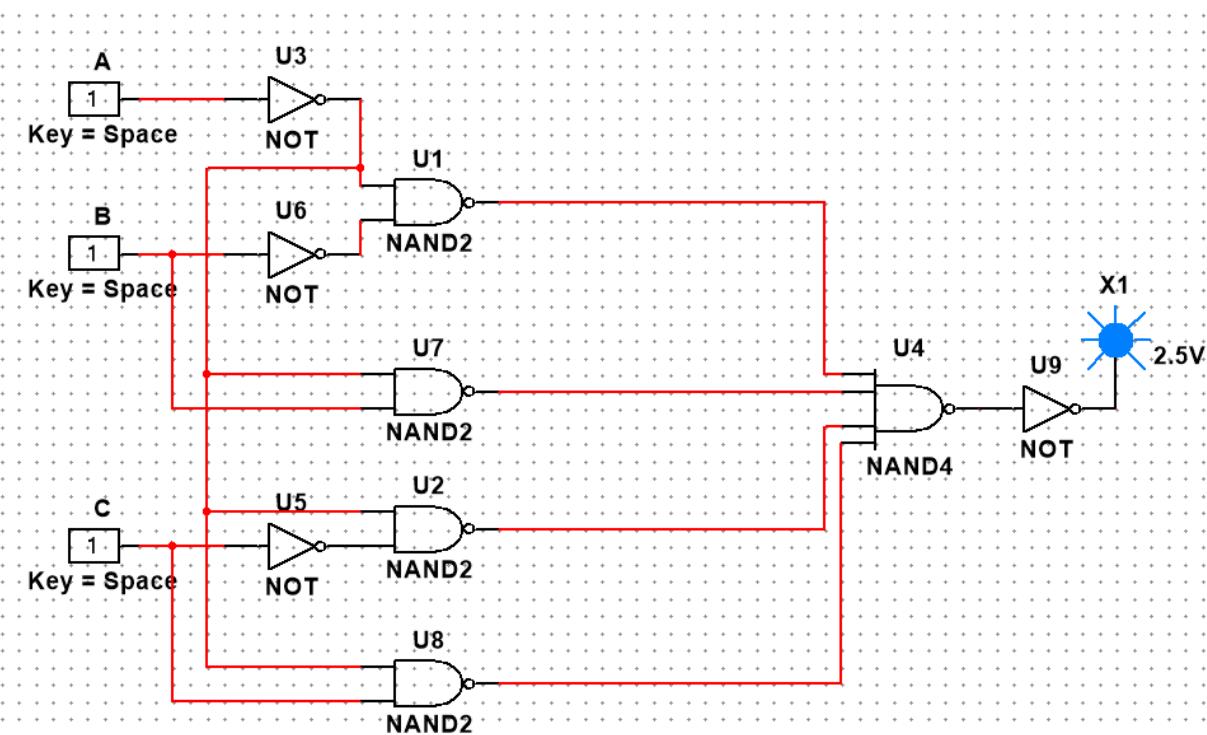


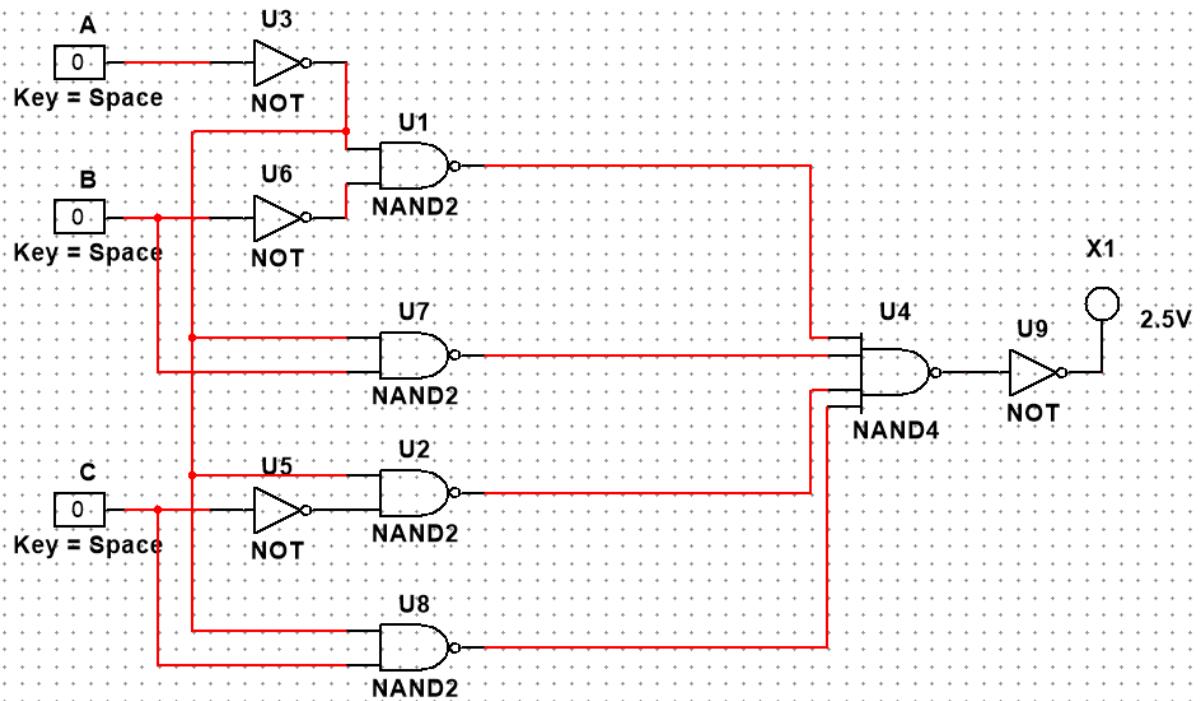
- Expression 3: $Y = AB + A\bar{B} + AC + A\bar{C}$
 - NAND gates
 - NOR gates

A	B	C	B'	C'	AB	AB'	AC	AC'	AB + A\bar{B} + AC + A\bar{C}
---	---	---	----	----	----	-----	----	-----	-------------------------------

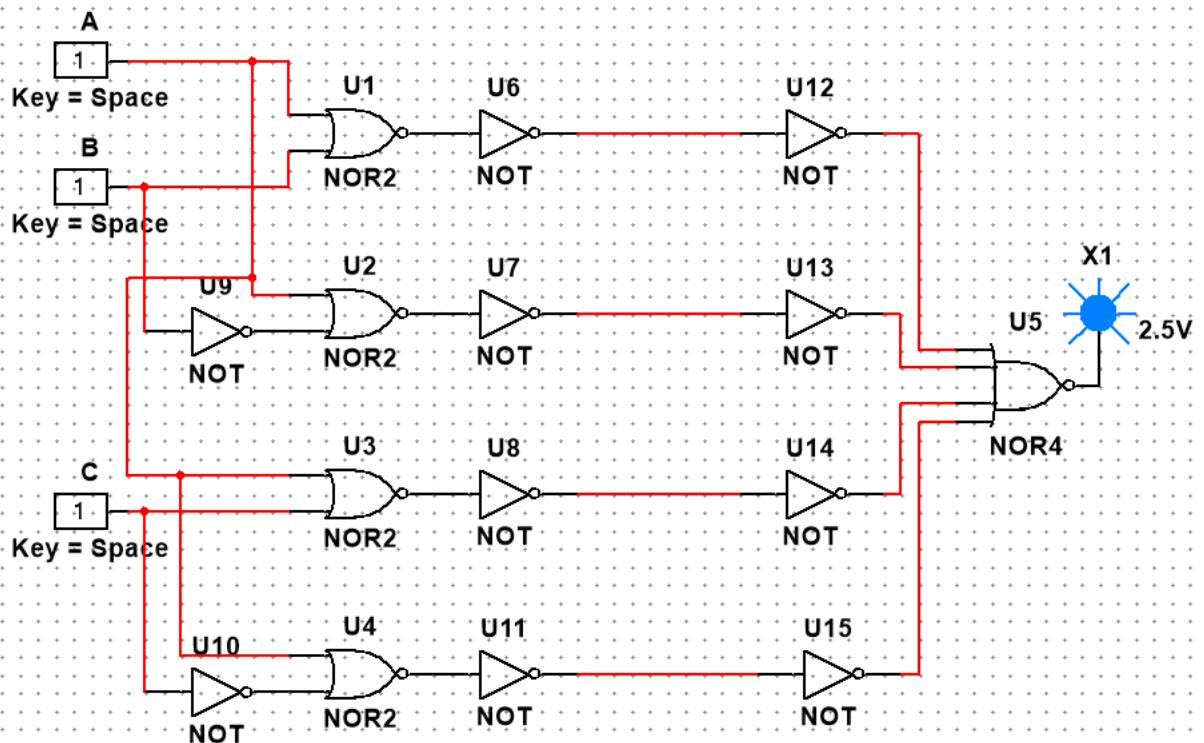
									A-C
0	0	0	1	1	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	1	1
1	0	1	1	0	0	1	1	0	1
1	1	0	0	1	1	0	0	1	1
1	1	1	0	0	1	0	1	0	1

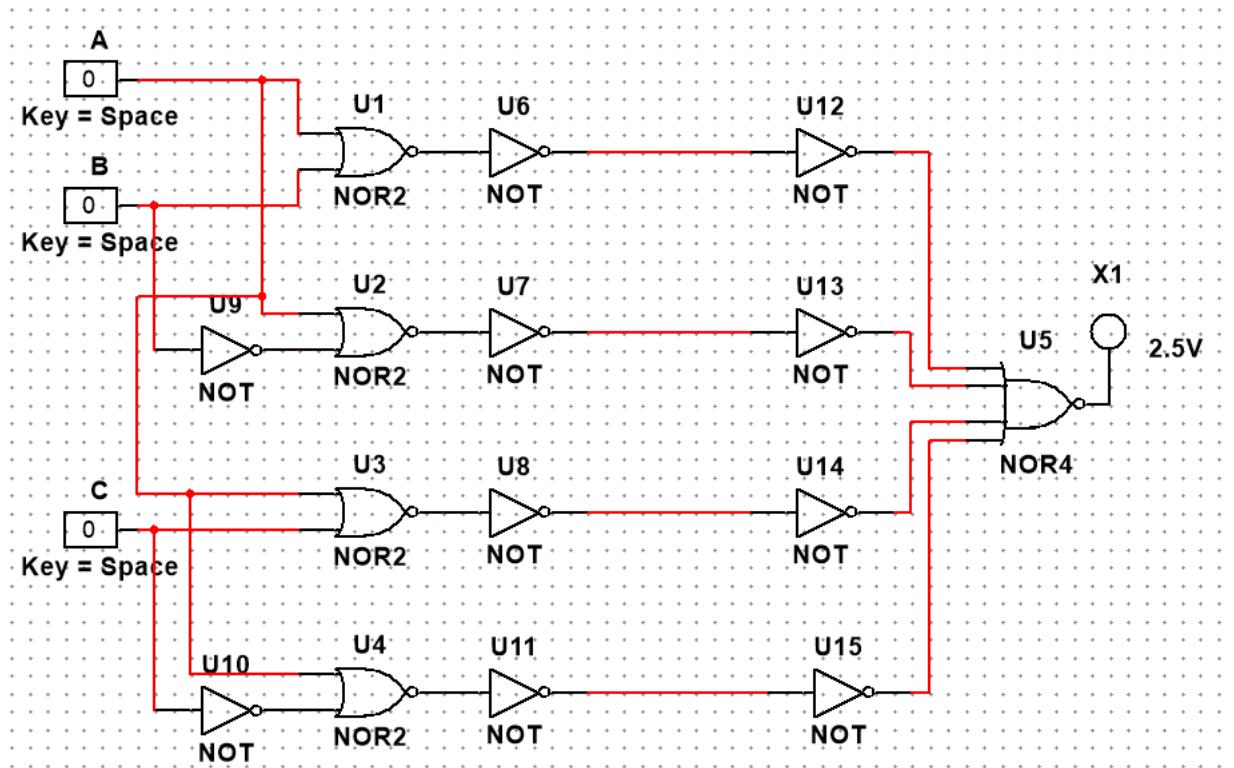
1. NAND gate:





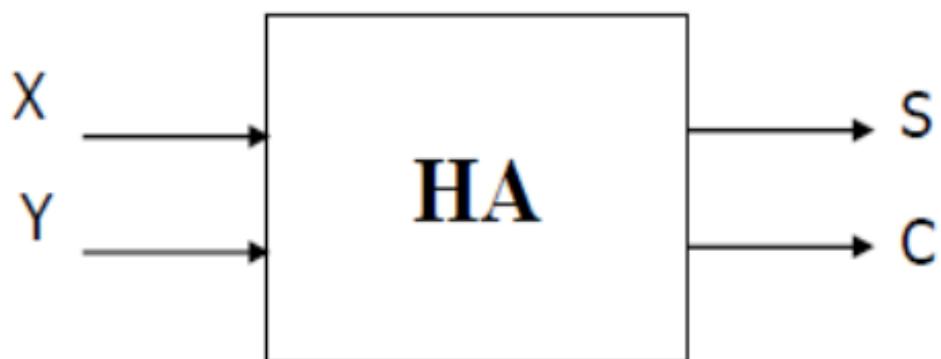
2. NOR gate:





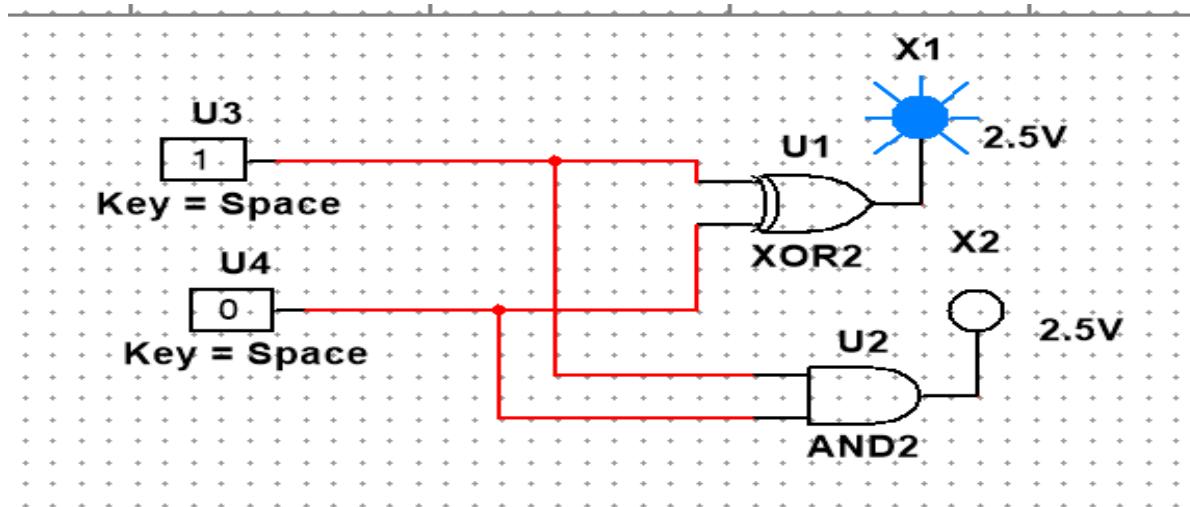
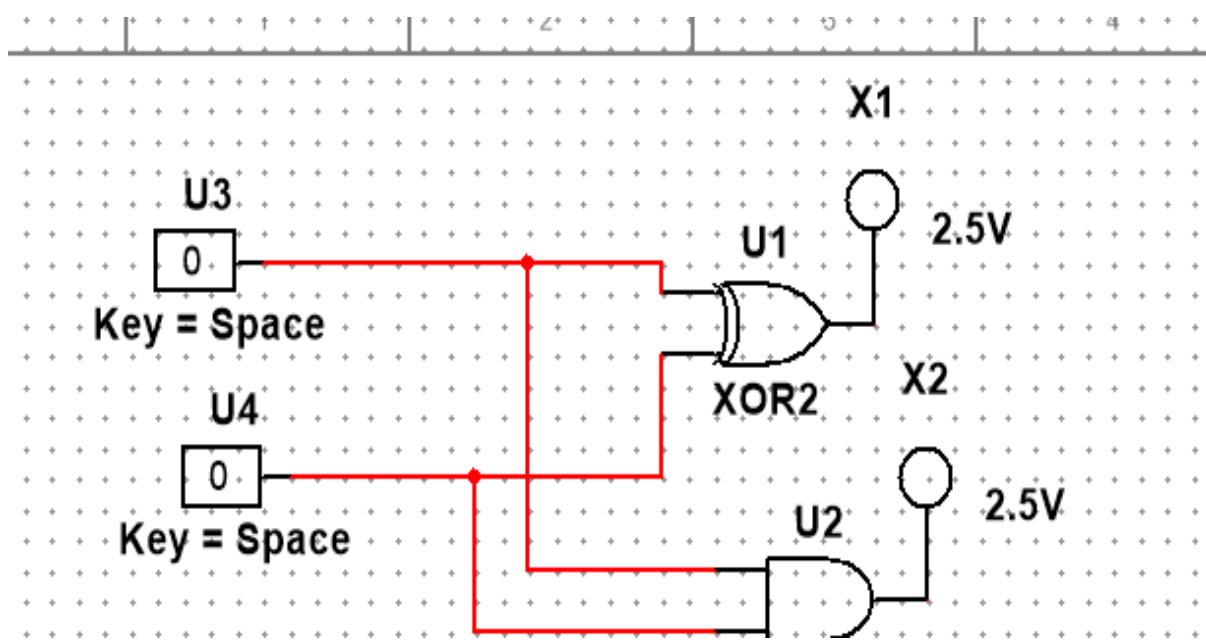
Topics: Half Adder, Full Adder and Multiplier

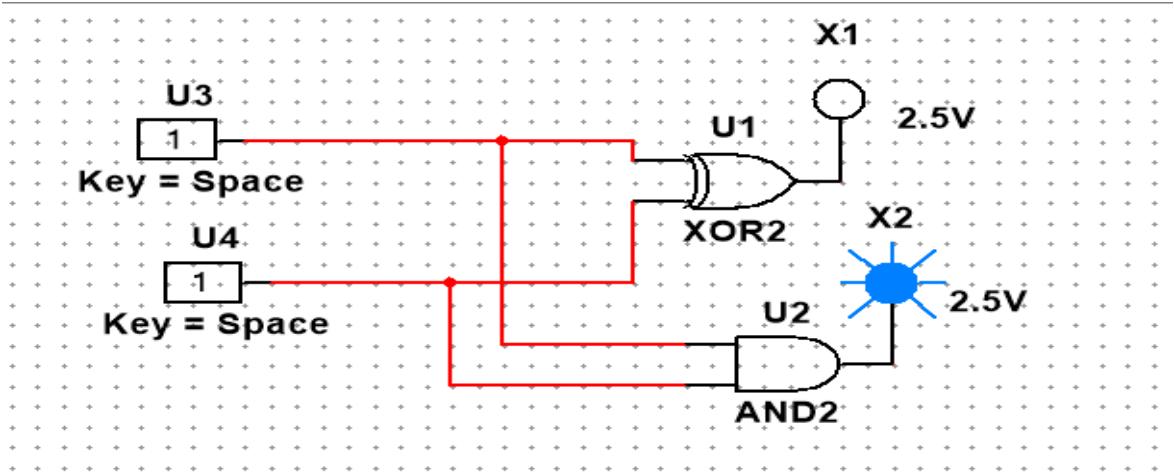
Half Adder:



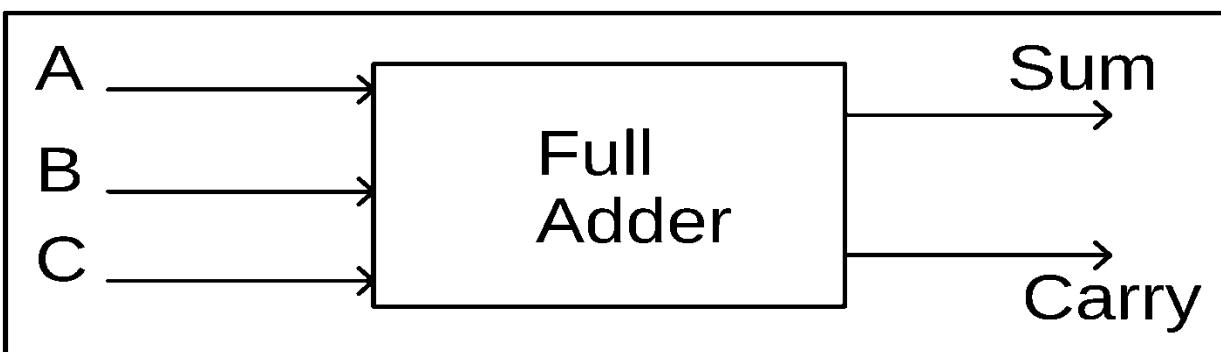
Inputs		Output	
A	B	Sum	Carry

0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

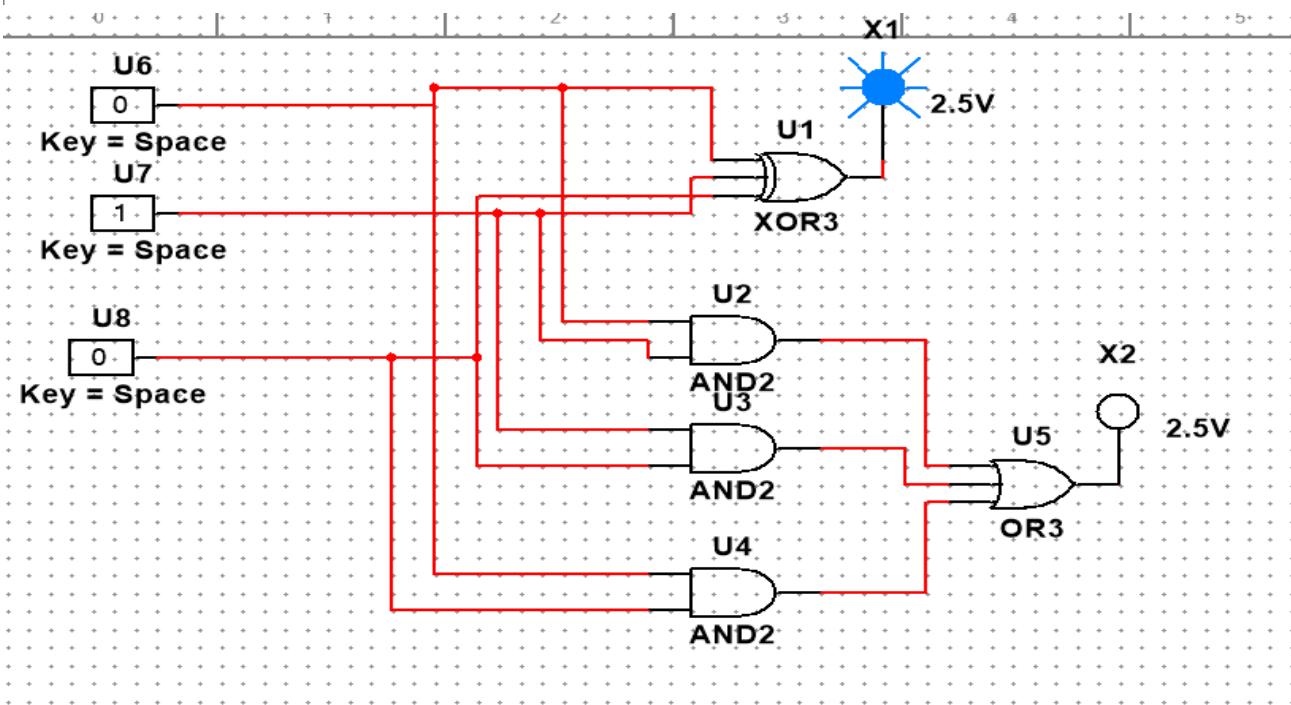
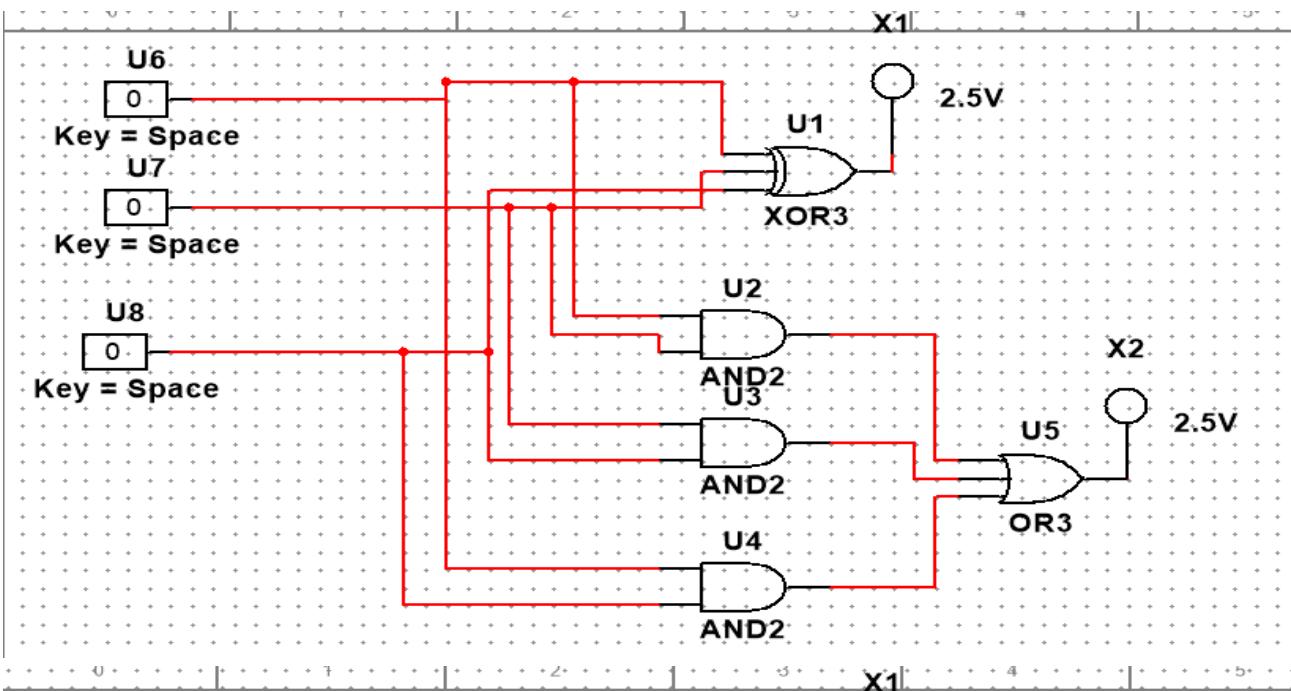


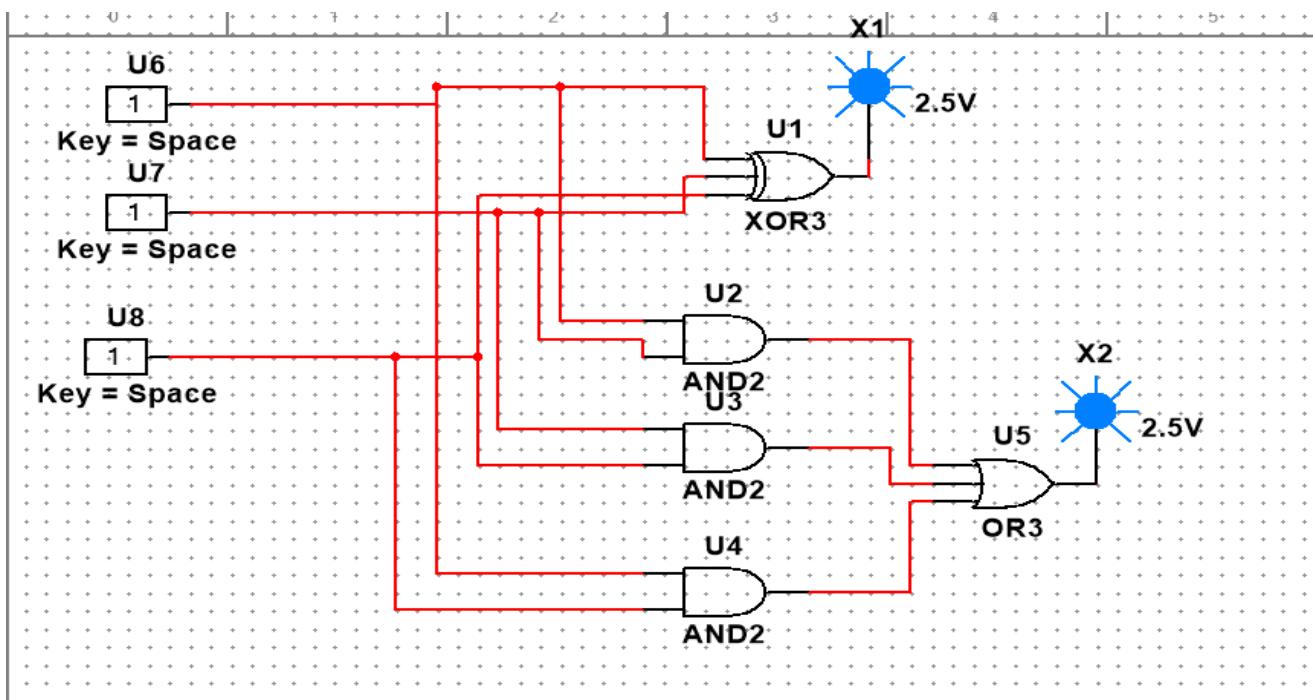
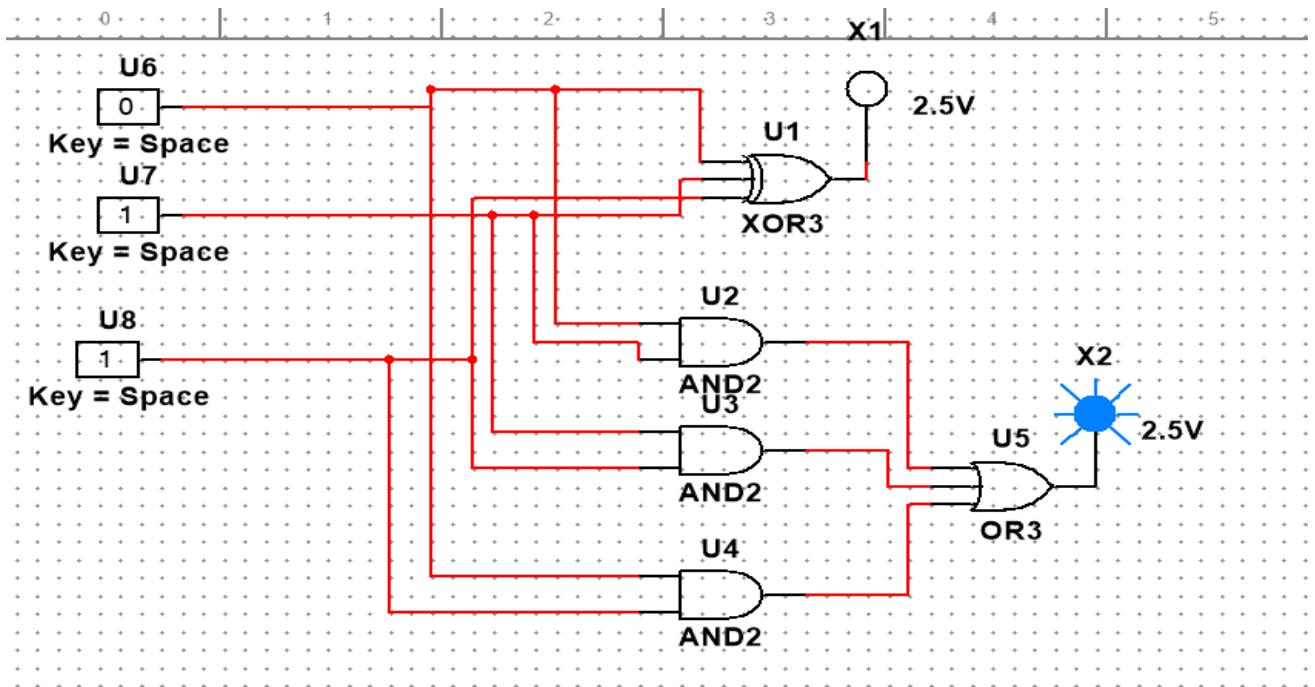


Full Adder:



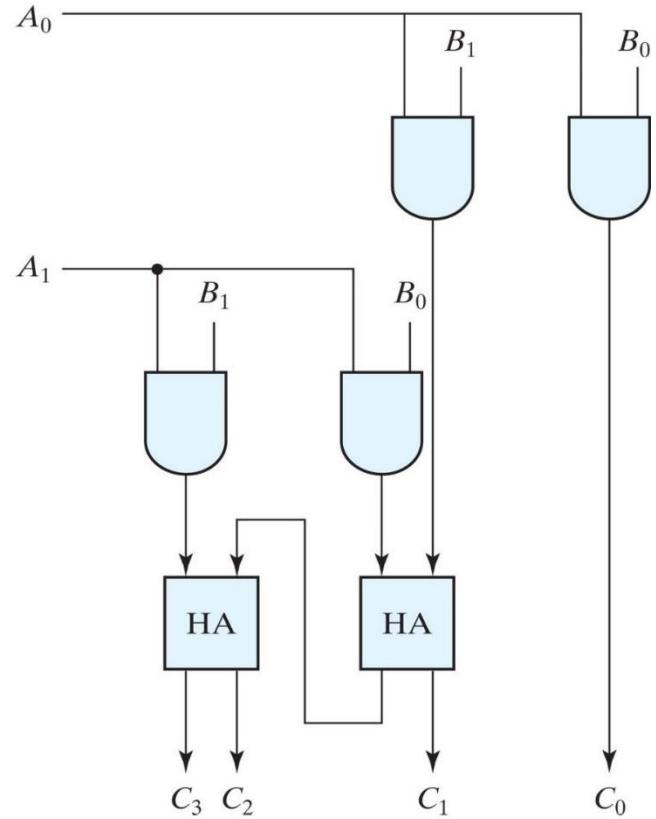
Inputs			Output	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1





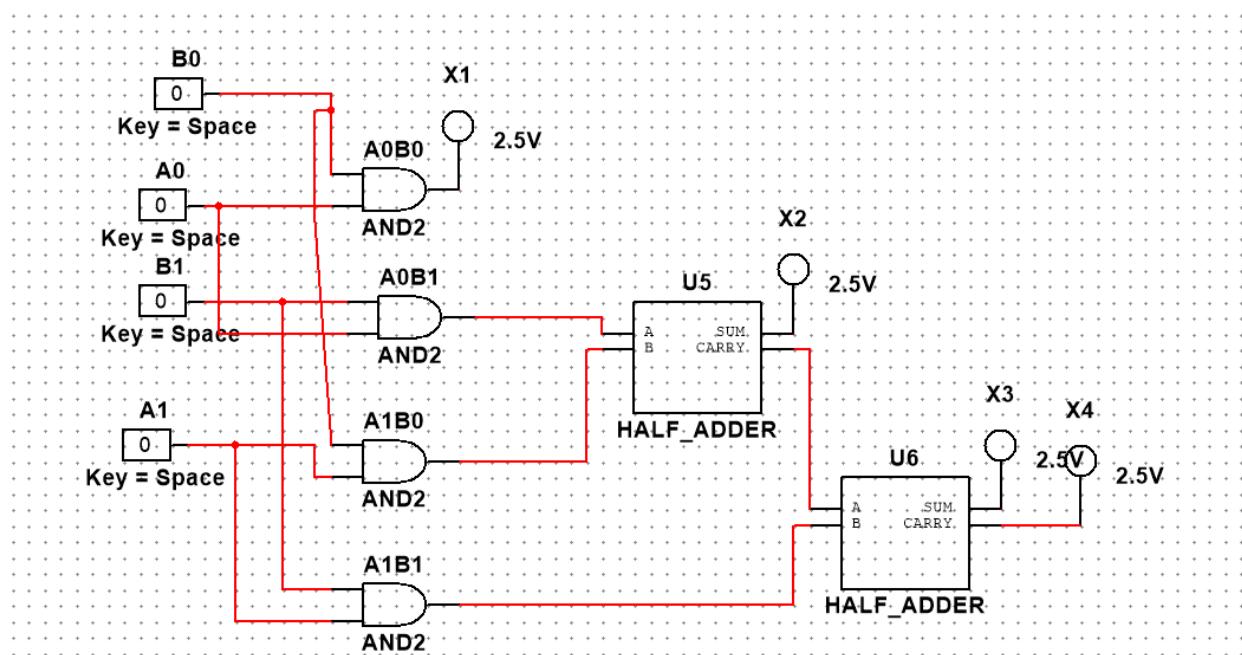
Multiplier:

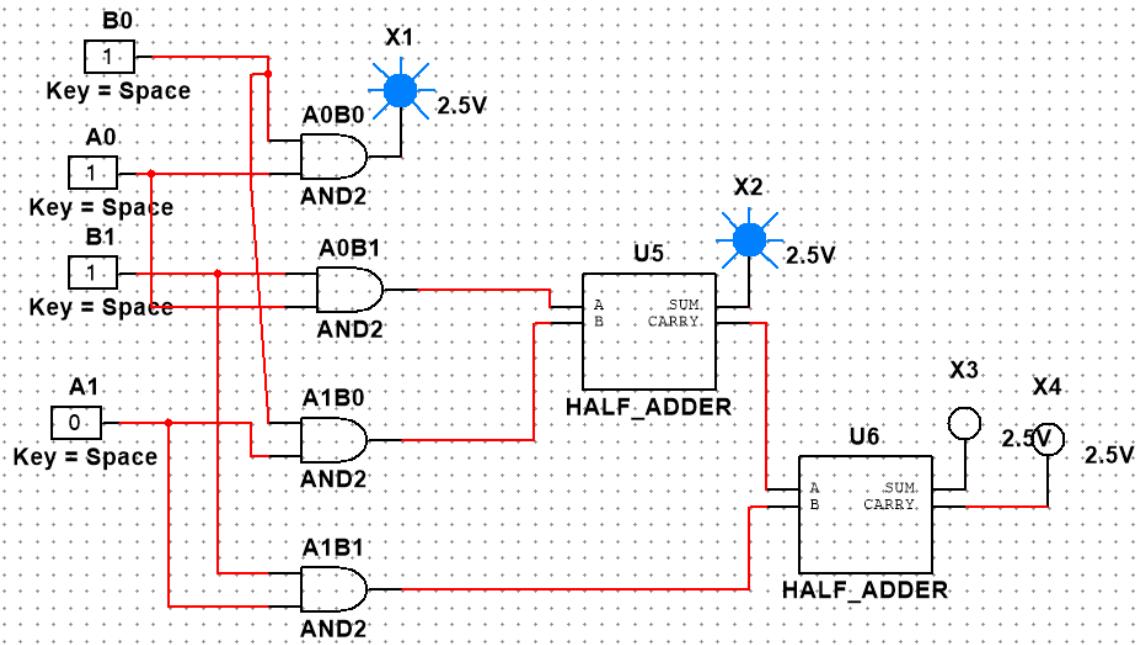
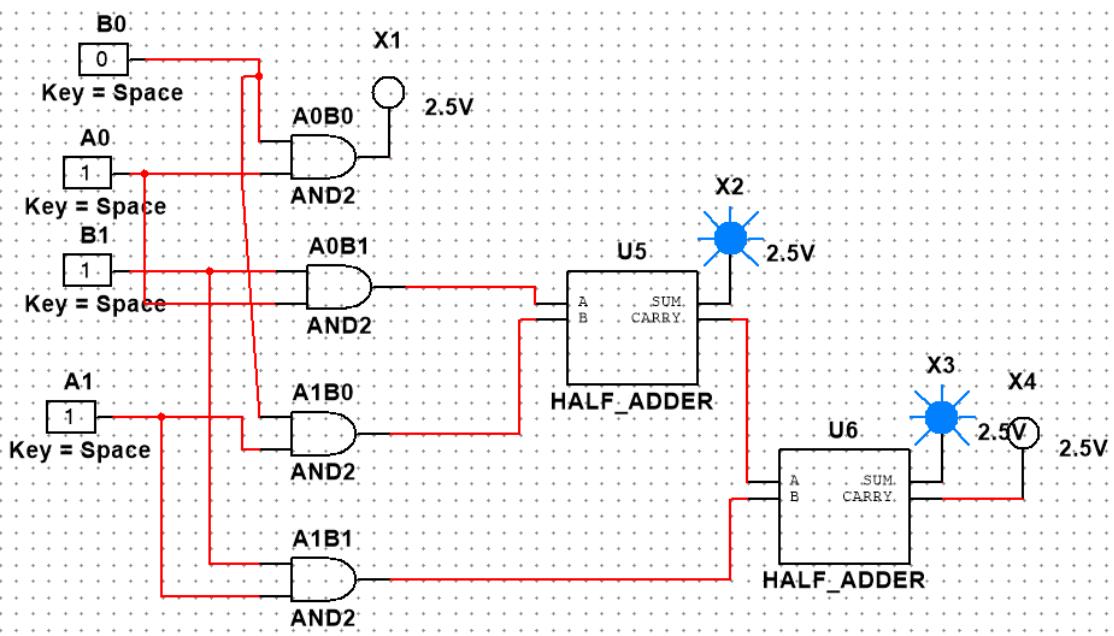
$$\begin{array}{r}
 & B_1 & B_0 \\
 & \underline{A_1} & \underline{A_0} \\
 A_0B_1 & & A_0B_0 \\
 \\
 \hline
 & A_1B_1 & A_1B_0 \\
 \hline
 C_3 & C_2 & C_1 & C_0
 \end{array}$$

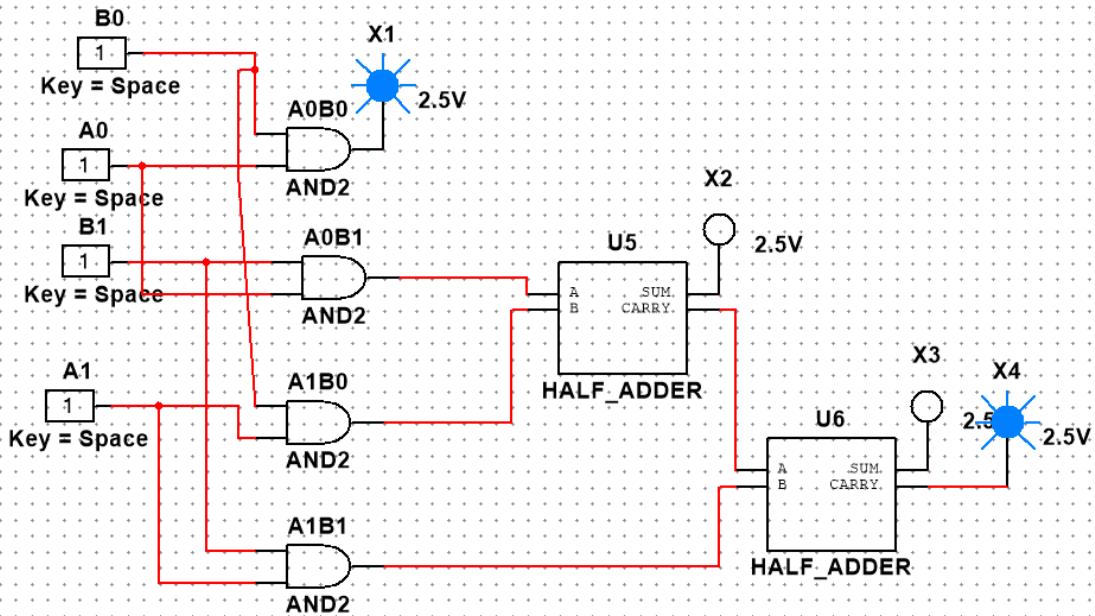


Inputs				Outputs			
A0	A1	B0	B1	A0B0	A0B1	A1B0	A1B1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0

1	0	1	0	1	0	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	1	0	1
1	1	1	0	1	0	1	0
1	1	1	1	1	1	1	1







LAB REPORT : 8

MULTIPLEXER:

2-BIT:

Truth Table:

INPUTS	Output
S_0	Y
0	A_0
1	A_1

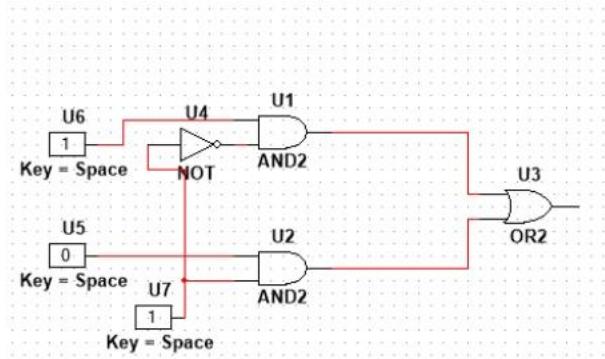
The logical expression of the term Y is as follows:

$$Y = S_0'.A_0 + S_0.A_1$$

- **4-BIT MUX:**

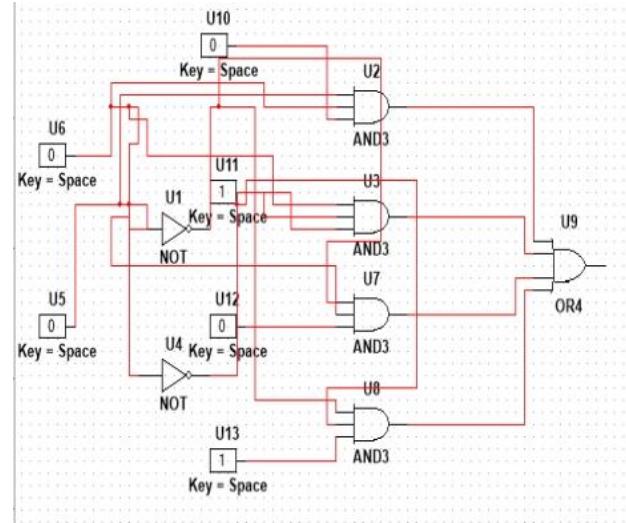
The logical expression of the term Y is as follows:

$$Y = S_1 \cdot S_0 \cdot A_0 + S_1 \cdot S_0 \cdot A_1 + S_1 \cdot S_0 \cdot A_2 + S_1 \cdot S_0 \cdot A_3$$



Truth Table:

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

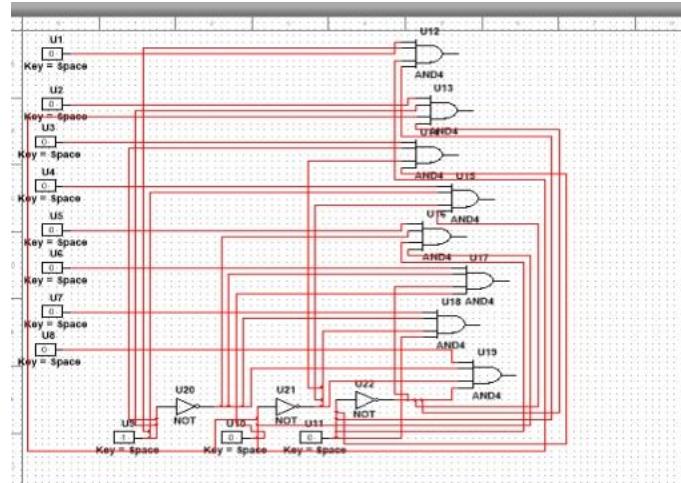


- 8-bit MUX:

The logical expression of the term Y is as follows:

$$Y = S_0 \cdot S_1 \cdot S_2 \cdot A_0 + S_0 \cdot S_1 \cdot S_2 \cdot A_1 + S_0 \cdot S_1 \cdot S_2 \cdot A_2 + S_0 \cdot S_1 \cdot S_2 \cdot A_3 + S_0 \cdot S_1 \cdot S_2 \cdot A_4 + S_0 \cdot S_1 \cdot S_2 \cdot A_5 + S_0 \cdot S_1 \cdot S_2 \cdot A_6 + S_0 \cdot S_1 \cdot S_2 \cdot A_7$$

INPUTS			Output
S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7



- DE-MULTIPLEXER:
- 2-BIT DE MUX:

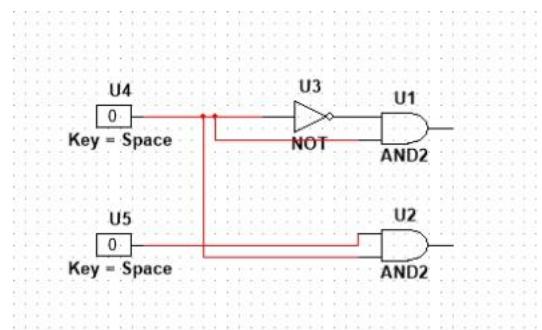
The logical expression of the term Y is as follows:

$$Y_0 = S_0 \cdot A$$

$$Y_1 = S_0 \cdot A$$

Truth Table:

INPUTS		Output	
S_1	S_0	Y_1	Y_0
0	0	0	A
1	1	A	0



- **4-BIT DE MUX:**

The logical expression of the term Y is as follows:

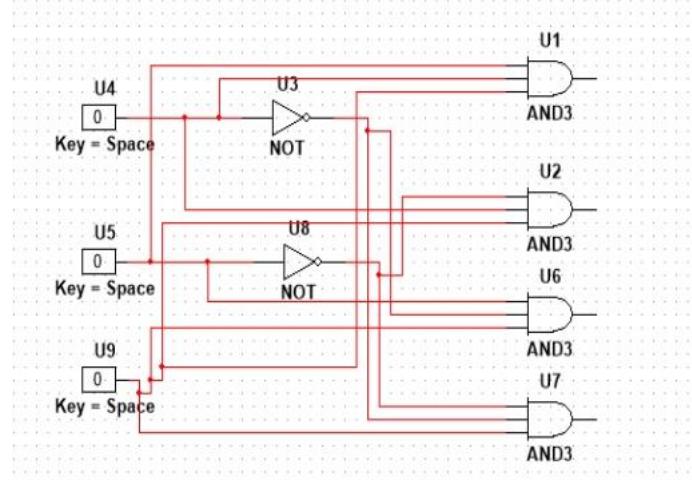
$$Y_0 = S_1' S_0' A$$

$$y_1 = S_1' S_0 A$$

$$y_2 = S_1 S_0' A$$

$$y_3 = S_1 S_0 A$$

INPUTS		Output			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	A
0	1	0	0	A	0
1	0	0	A	0	0
1	1	A	0	0	0



- **8-BIT DE MUX:**

- **MAGNITUDE COMPARATOR:**

- **1-BIT COMPARATOR:**

Expression for A < B

$$Y = A'B$$

Expression for A = B

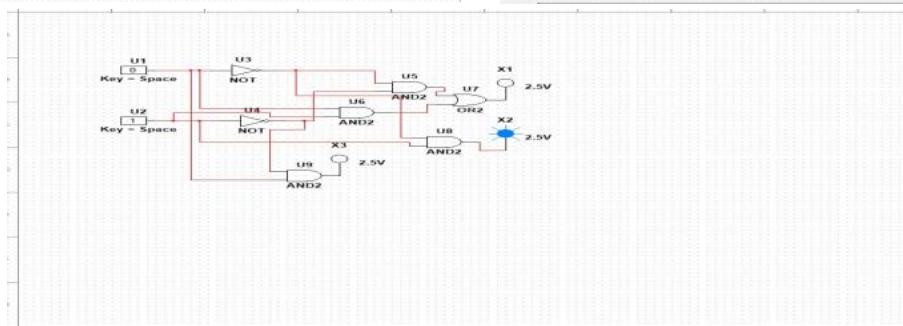
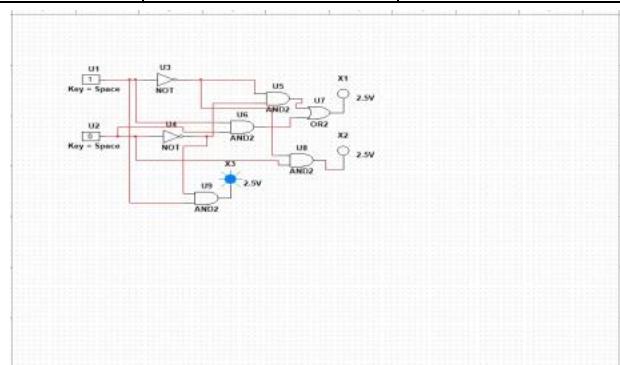
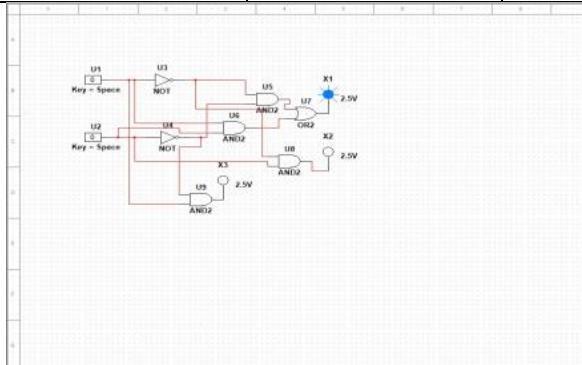
$$Y = A'B' + AB$$

Expression for A > B

$$Y = AB'$$

TRUTH TABLE:

A	B	A < B	A = B	A > B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0



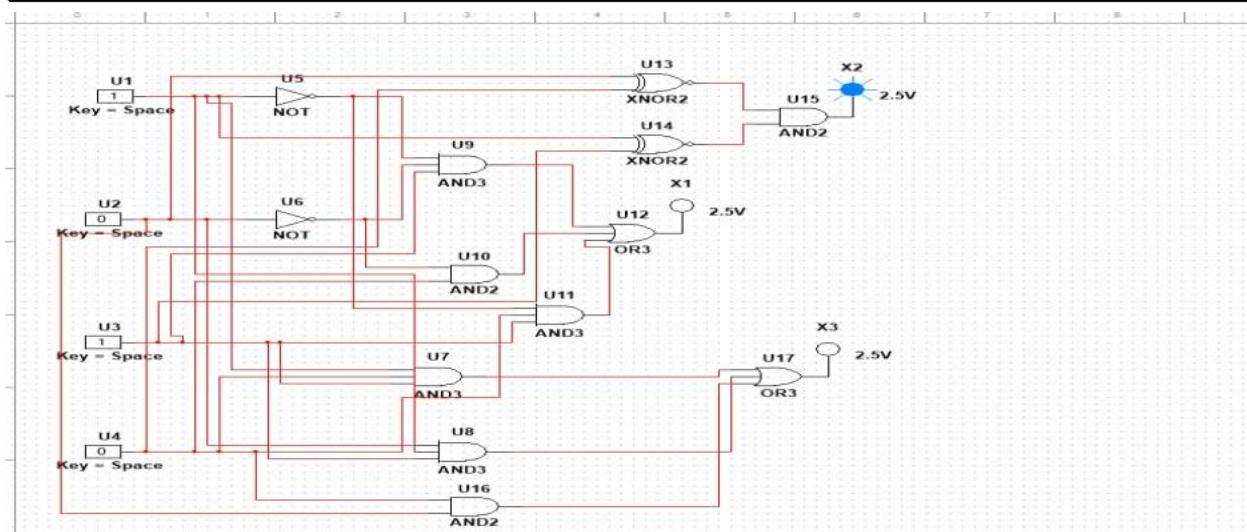
- 2-BIT COMPARATOR:

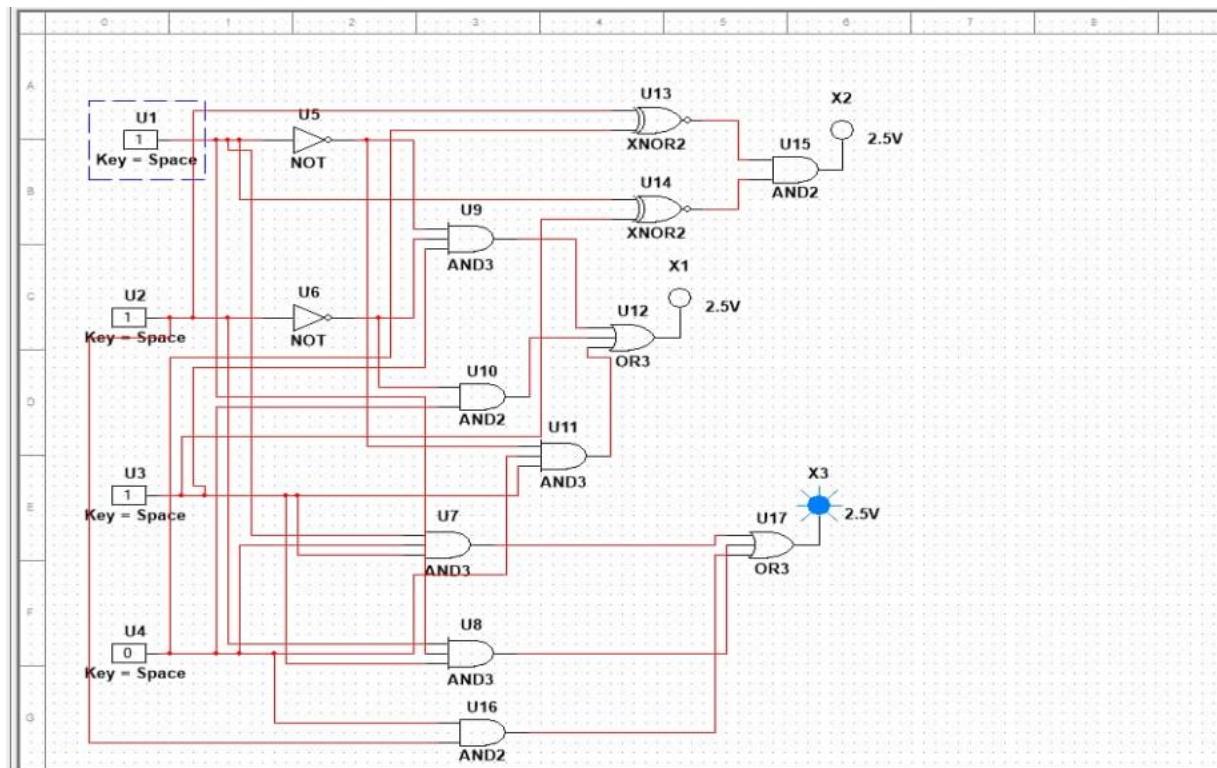
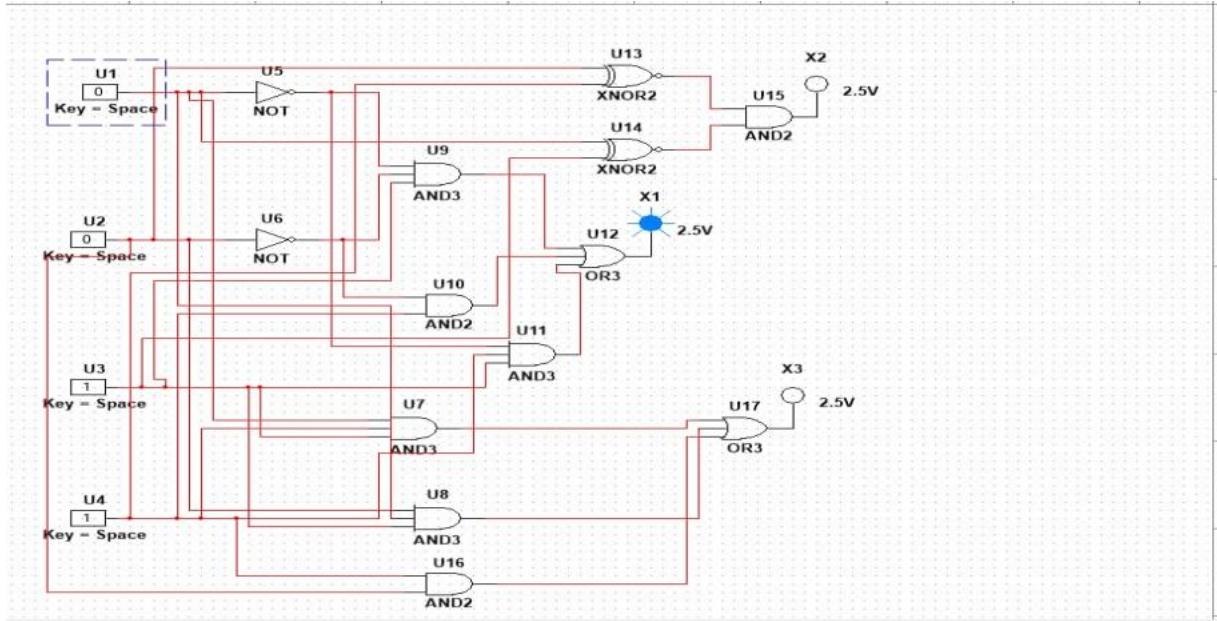
$$A < B = A'A.B' + A'B + A.B'B'$$

$$A = B = (A.B') (A'.B)$$

$$A > B = A.B.B' + A.A'.B' + AB$$

Inputs				Outputs		
A		B		G(A>B)	E(A=B)	L(A<B)
A1	A0	B1	B0			
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0





Lab Number #09

Verifying Latches (S-R Latch & D Latch)

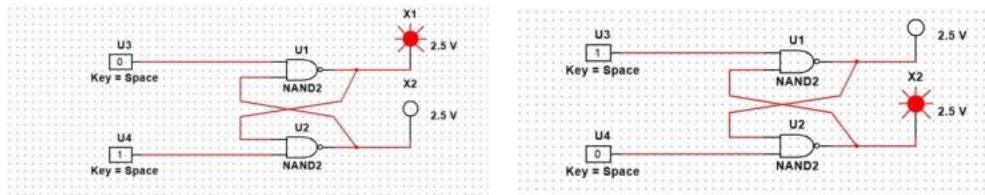
A latch is a basic digital memory circuit that stores one bit of data. Unlike combinational logic circuits, latches have memory and can store information based on the input signals.

S-R Latch (Set-Reset Latch):

SR latch using NAND

Truth Table

S	R	Q	Q'
0	0	Not Used	Not Used
0	1	1	0
1	0	0	1
1	1	No change	No change



SR latch using NOR

S	R	Q _n
0	0	Q(n-1)
0	1	1
1	0	0
1	1	Not Used

