EE122 Computer Architecture & Logic Design

- **TOPICS:** REGISTERS AND COUNTERS

WEEK: 10

PROGRAM: BE COMPUTER SOFTWARE ENGINEERING

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Today's Lecture

Identify the basic forms of data movement in shift registers

Explain how serial in/serial out, serial in/parallel out, parallel in/serial out, and parallel in/parallel out shift registers operate

Describe how a bidirectional shift register operates

Determine the sequence of a Johnson counter

Set up a ring counter to produce a specified sequence

Construct a ring counter from a shift register

Use a shift register as a time-delay device

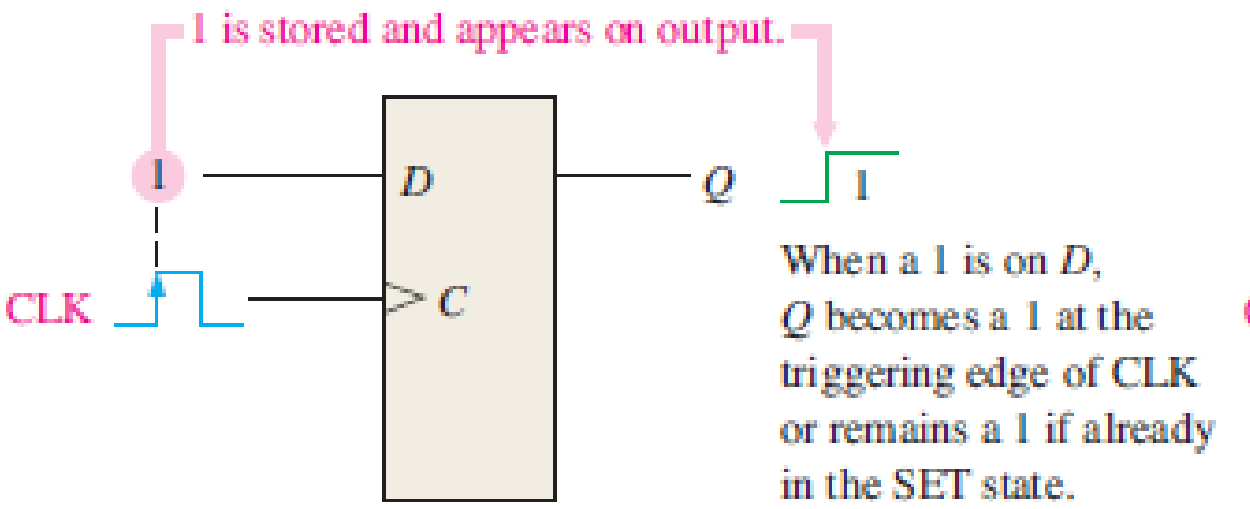
Use a shift register to implement a serial-to-parallel data converter

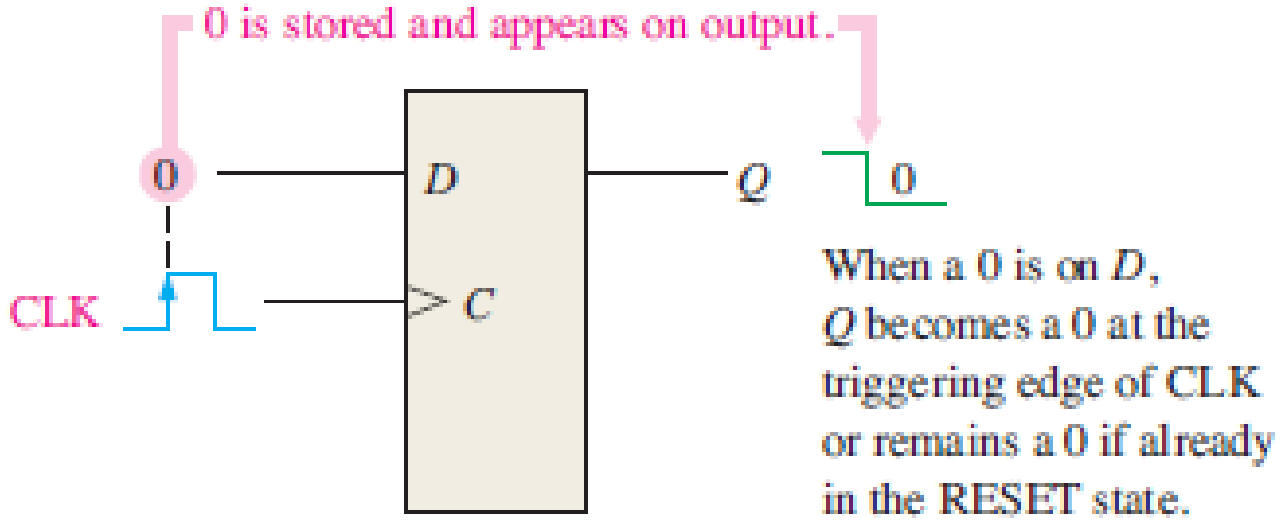
Shift Registers – Introduction

- A type of sequential logic circuit
- Storage of digital data
- Shift registers consist of arrangements of flip-flops and are important in applications involving the storage and transfer of data in a digital system.
- A register has no specified sequence of states, except in certain very specialized applications.
- A register, in general, is used solely for storing and shifting data (1s and 0s) entered into it from an external source and typically possesses no characteristic internal sequence of states.

Shift Register Operations

A register can consist of one or more flip-flops used to store and shift data.

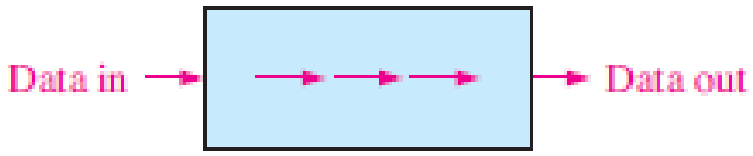




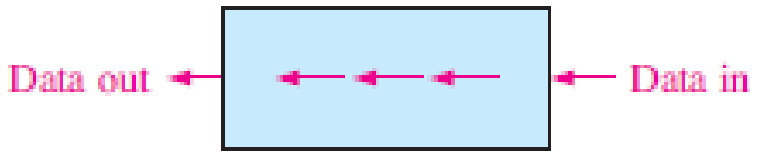
The *storage capacity* of a register is the total number of bits (1s and 0s) of digital data it can retain. Each **stage** (flip-flop) in a shift register represents one bit of storage capacity; therefore, the number of stages in a register determines its storage capacity.

The flip-flop as a storage element.

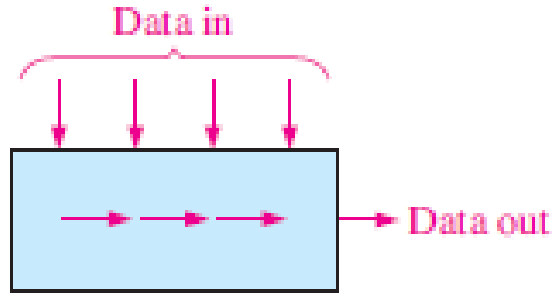
shift capability – Data movement in Registers



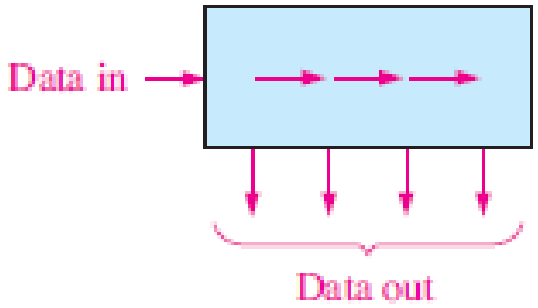
(a) Serial in/shift right/serial out



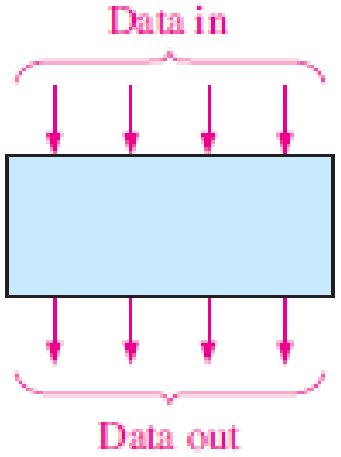
(b) Serial in/shift left/serial out



(c) Parallel in/serial out



(d) Serial in/parallel out



(e) Parallel in/parallel out

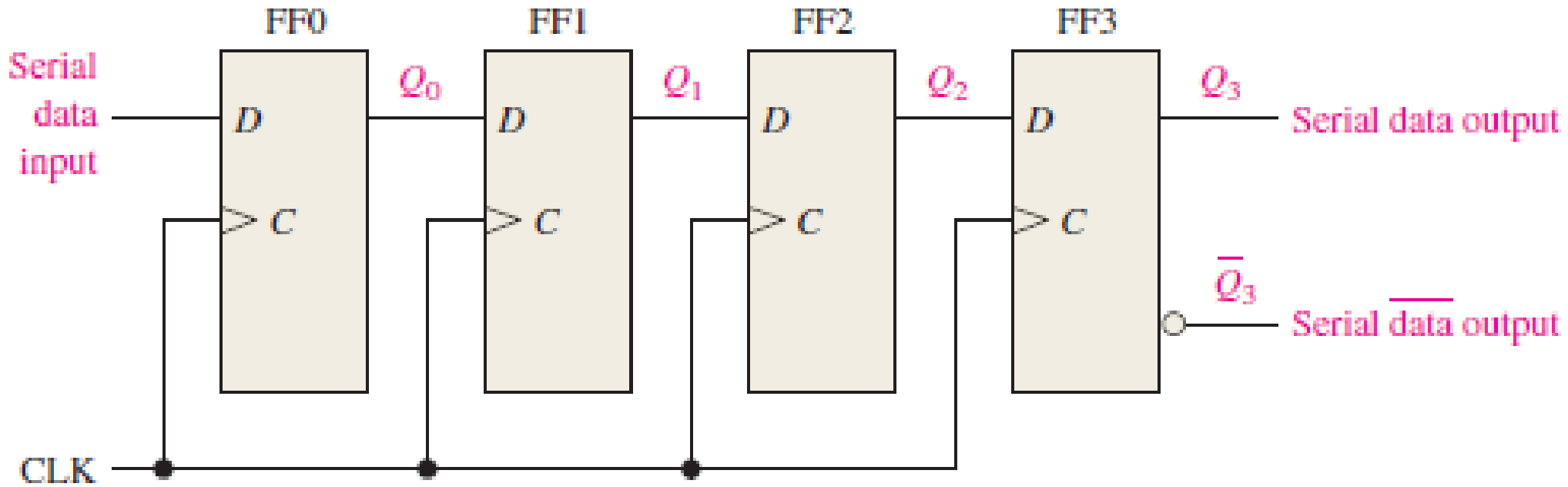
(f) Rotate right

(g) Rotate left

Types of Shift Register Data I/Os

1. Serial In/Serial Out Shift Registers
2. Serial in/parallel out Shift Registers
3. Parallel in/serial out Shift Registers
4. Parallel in/ Parallel out Shift Registers

Serial In/Serial Out Shift Registers



Serial in/serial out shift register.

With four stages, this register can store up to four bits of data.

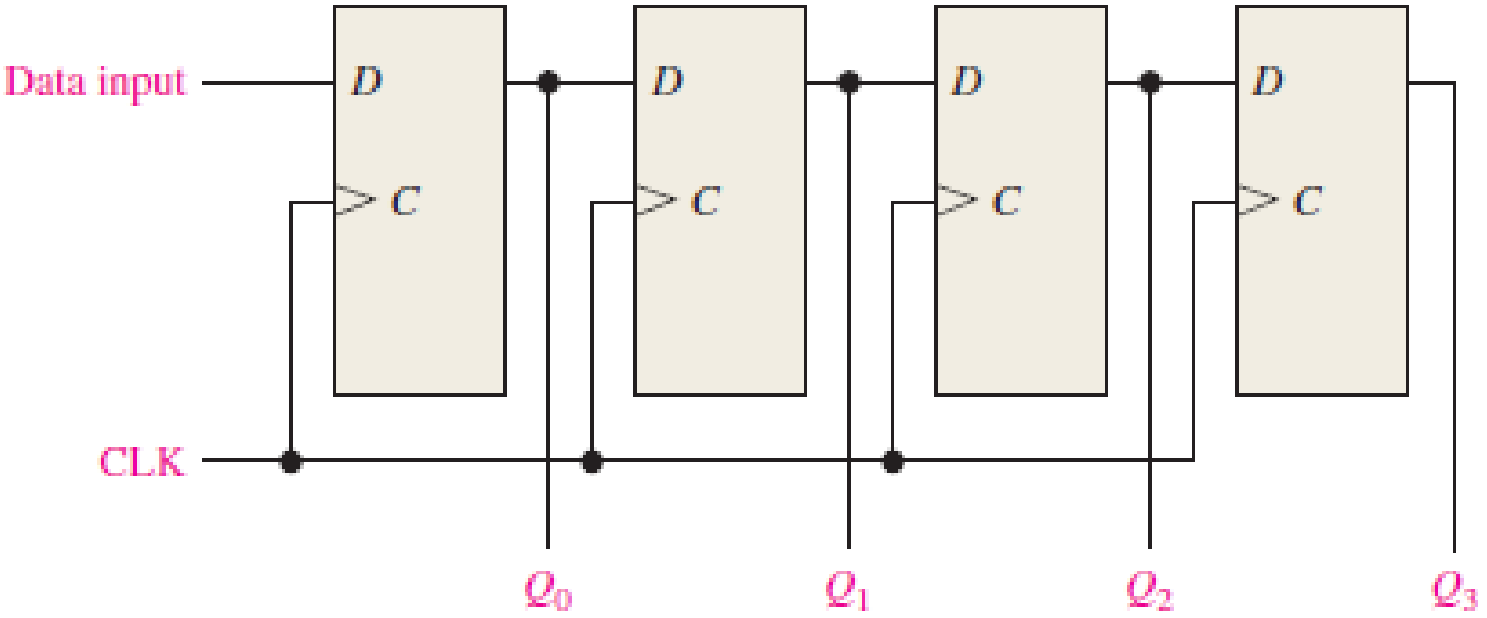
Shifting a 4-bit code into the shift register in Figure
Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

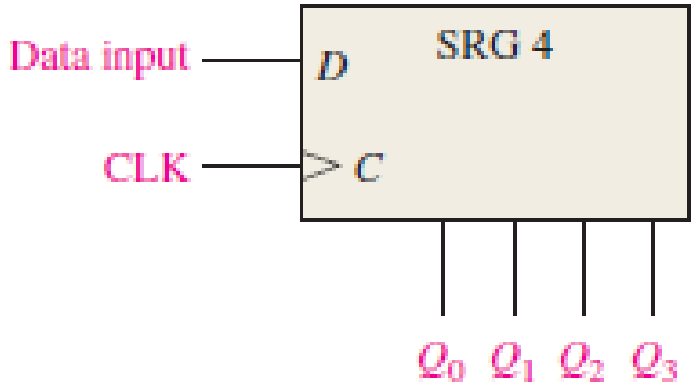
Shifting a 4-bit code out of the shift register in Figure
Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	1	0	1	0
5	0	1	0	1
6	0	0	1	0
7	0	0	0	1
8	0	0	0	0

Serial In/Parallel Out Shift Registers



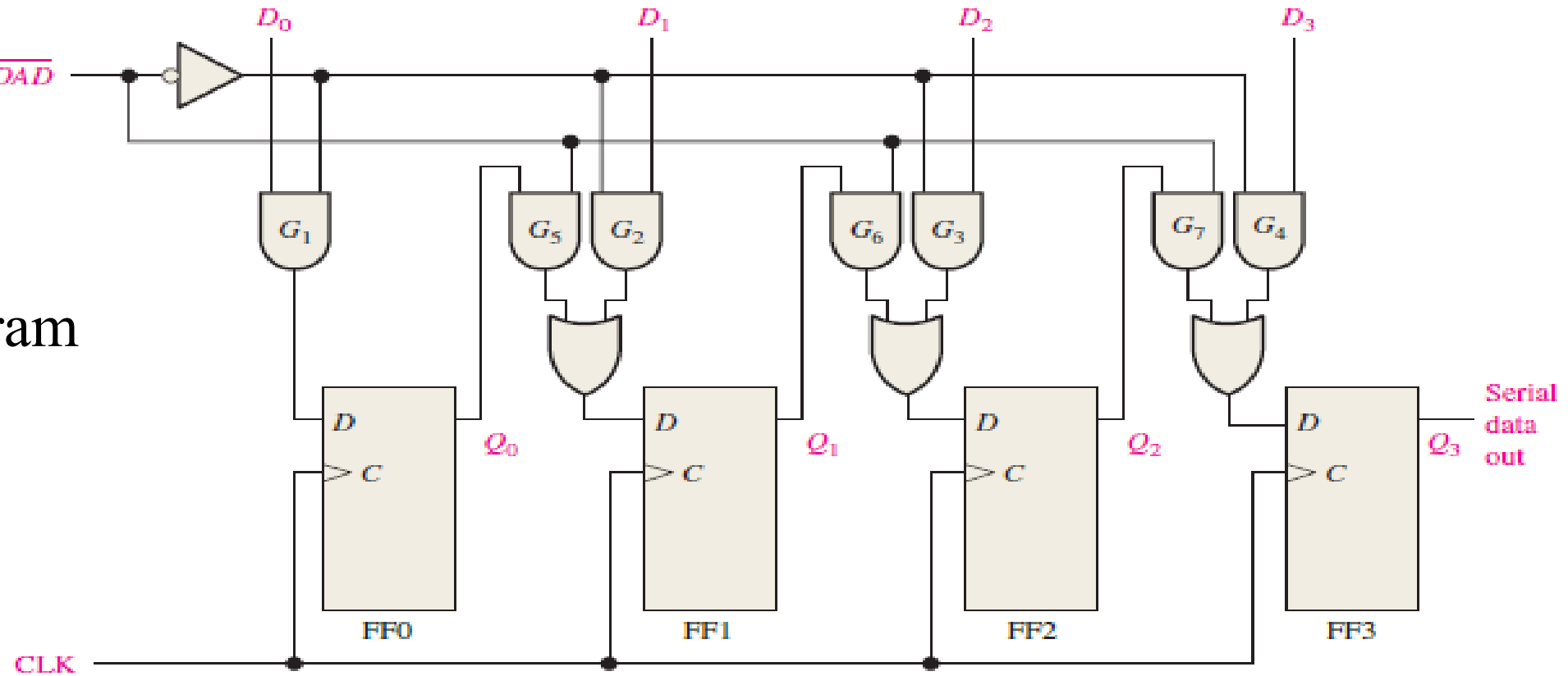
(a)



(b)

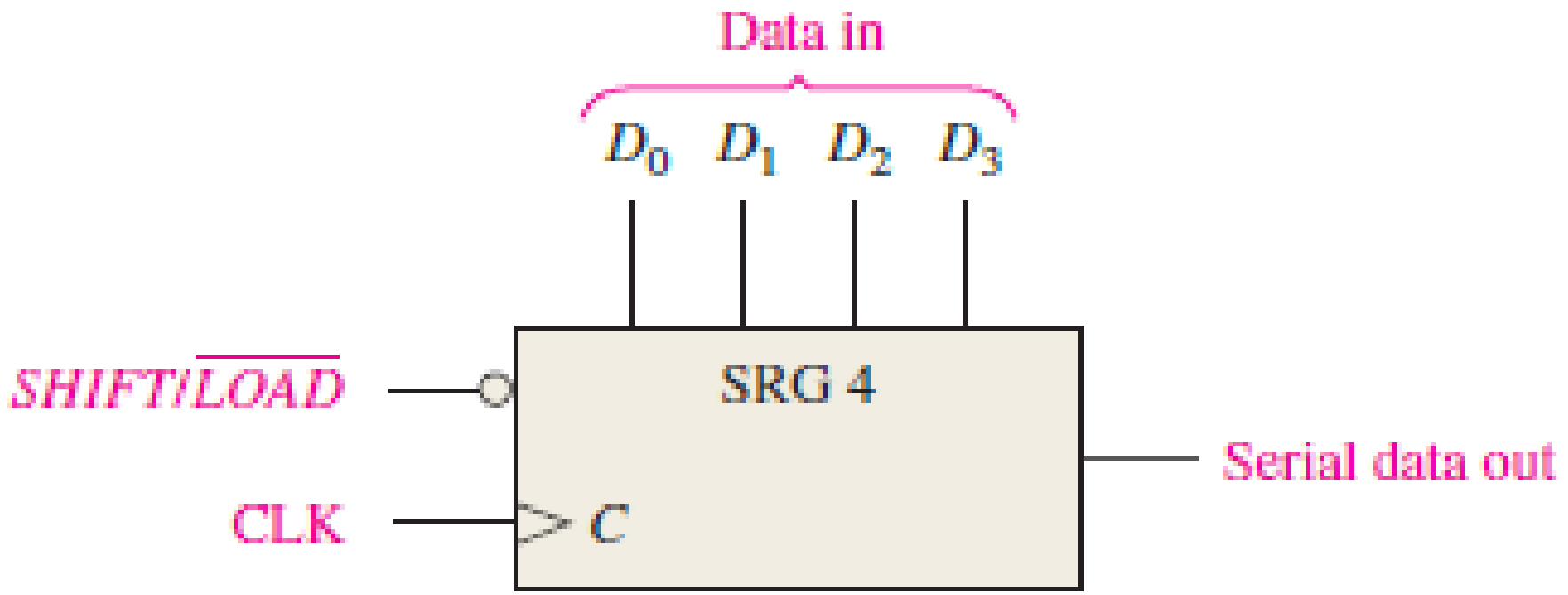
Parallel In/Serial Out Shift Registers

Logic diagram

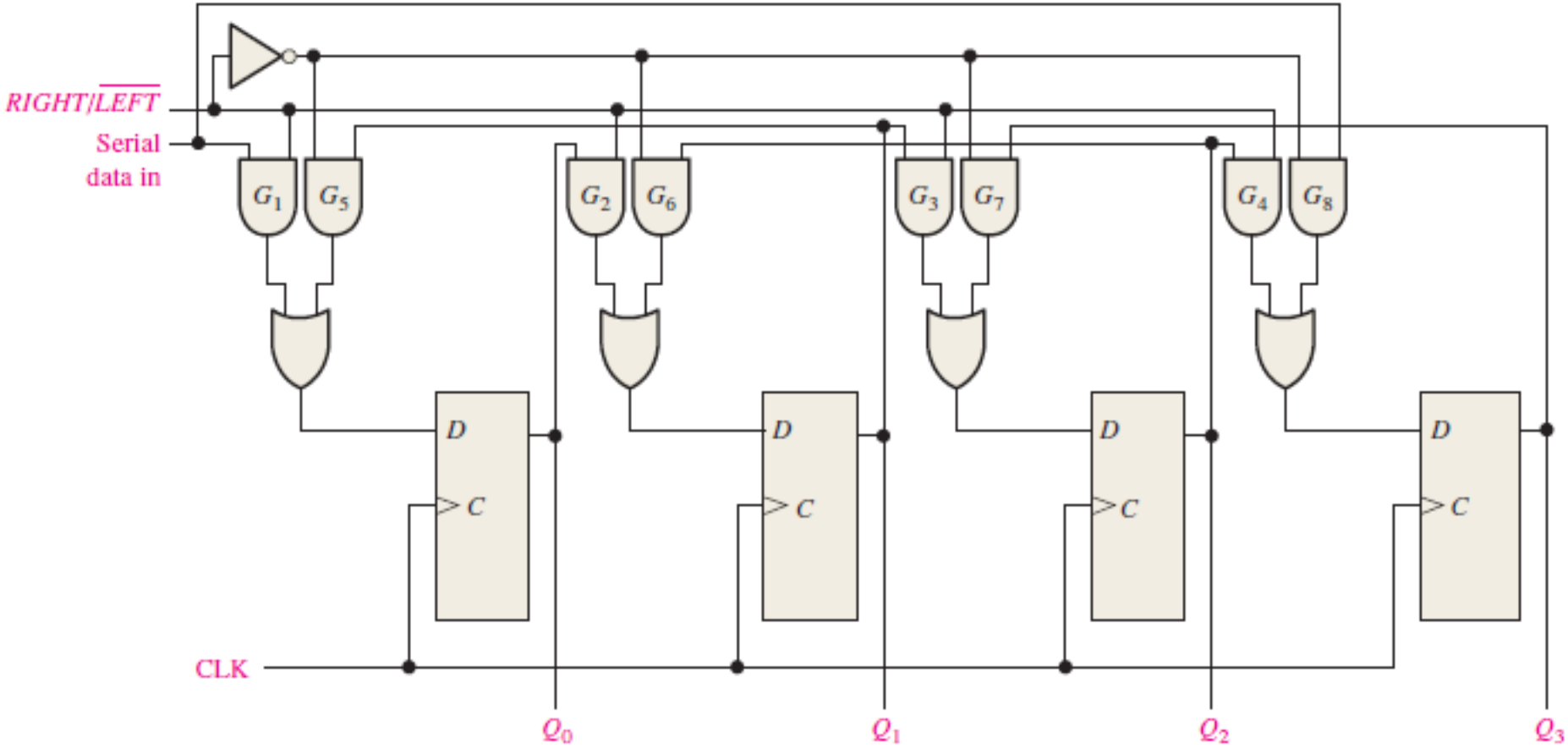


When *SHIFT/LOAD** is LOW, gates *G*1 through *G*4 are enabled, allowing each data bit to be applied to the *D* input of its respective flip-flop. When a clock pulse is applied, the flip-flops with *D* = 1 will set and those with *D* = 0 will reset, thereby storing all four bits simultaneously

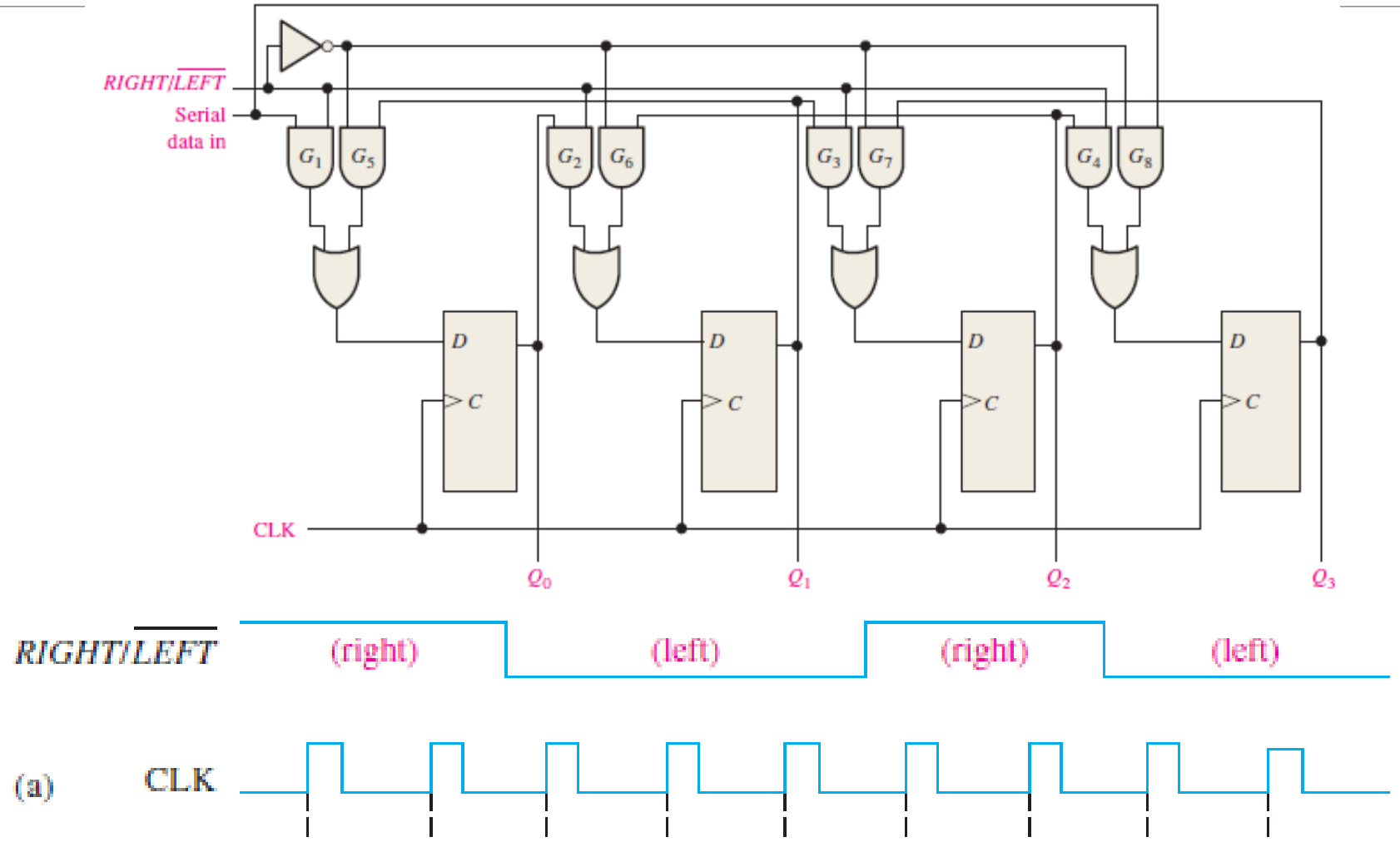
Parallel In/Serial Out Shift Registers- Logic symbol



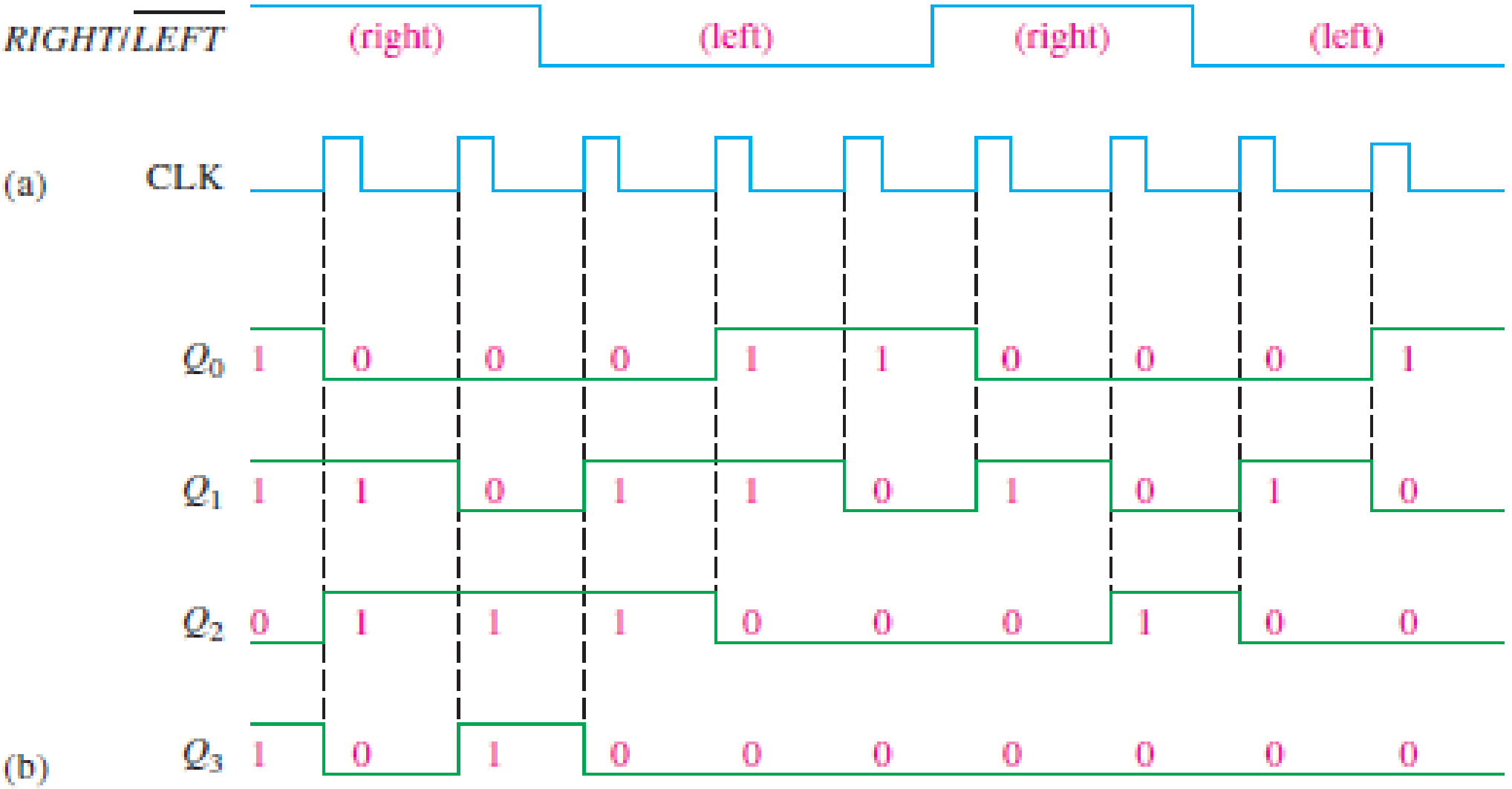
Bidirectional Shift Registers



Example: Determine the state of the shift register of in the Figure (previous slide) after each clock pulse for the given *RIGHT*/*LEFT** control input waveform shown. Assume that *Q*0 = 1, *Q*1 = 1, *Q*2 = 0, and *Q*3 = 1 and that the serial data-input line is LOW.



Solution


RIGHT/LEFT
(right)
(left)
(right)
(left)
(a)
CLK
Q_0 1 0 0 0 1 1 0 0 0 1
Q_1 1 1 0 1 1 0 1 0 1 0
Q_2 0 1 1 1 0 0 0 1 0 0
(b)
Q_3 1 0 1 0 0 0 0 0 0 0

Shift Register Counters

- Discuss how a shift register counter differs from a basic shift register
- Explain the operation of a Johnson counter
- Specify a Johnson sequence for any number of bits
- Explain the operation of a ring counter and determine the sequence of any specific ring counter

The Johnson Counter

Table a)

Four-bit Johnson sequence.

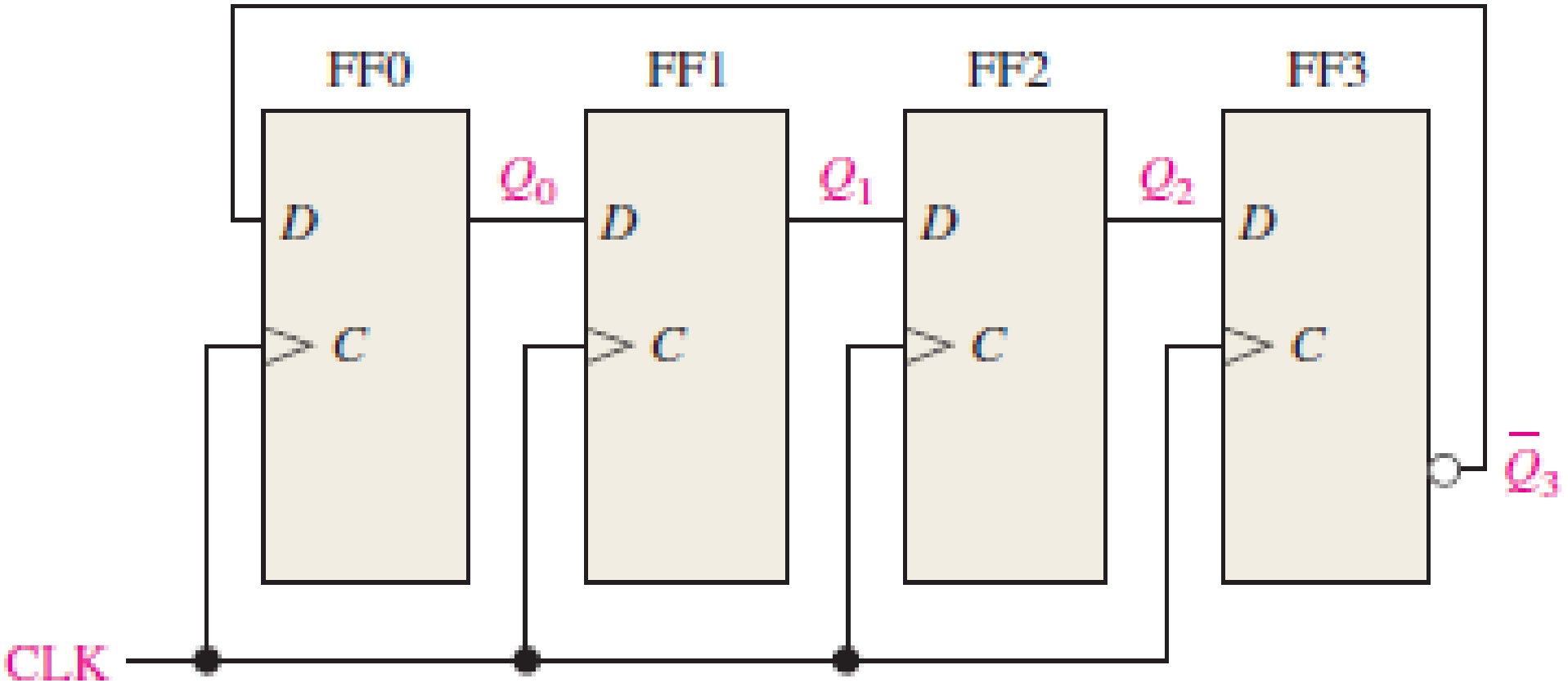
Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Table b)

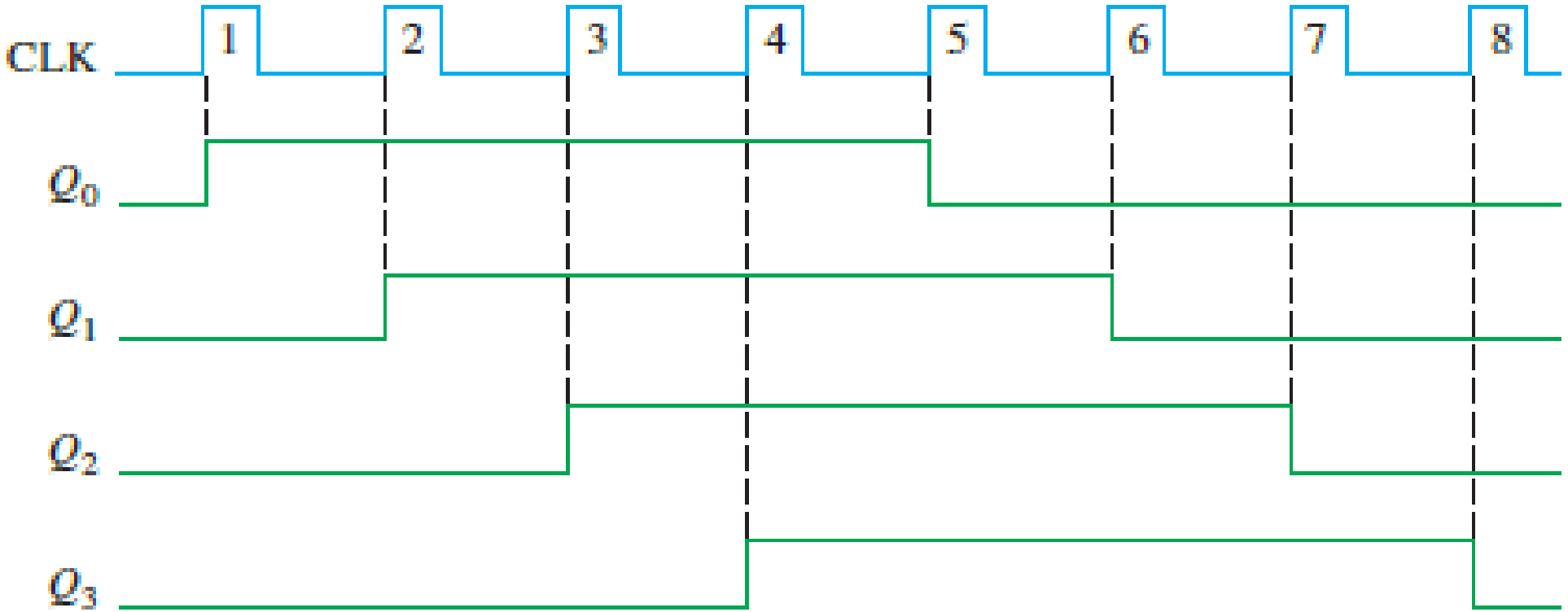
Five-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

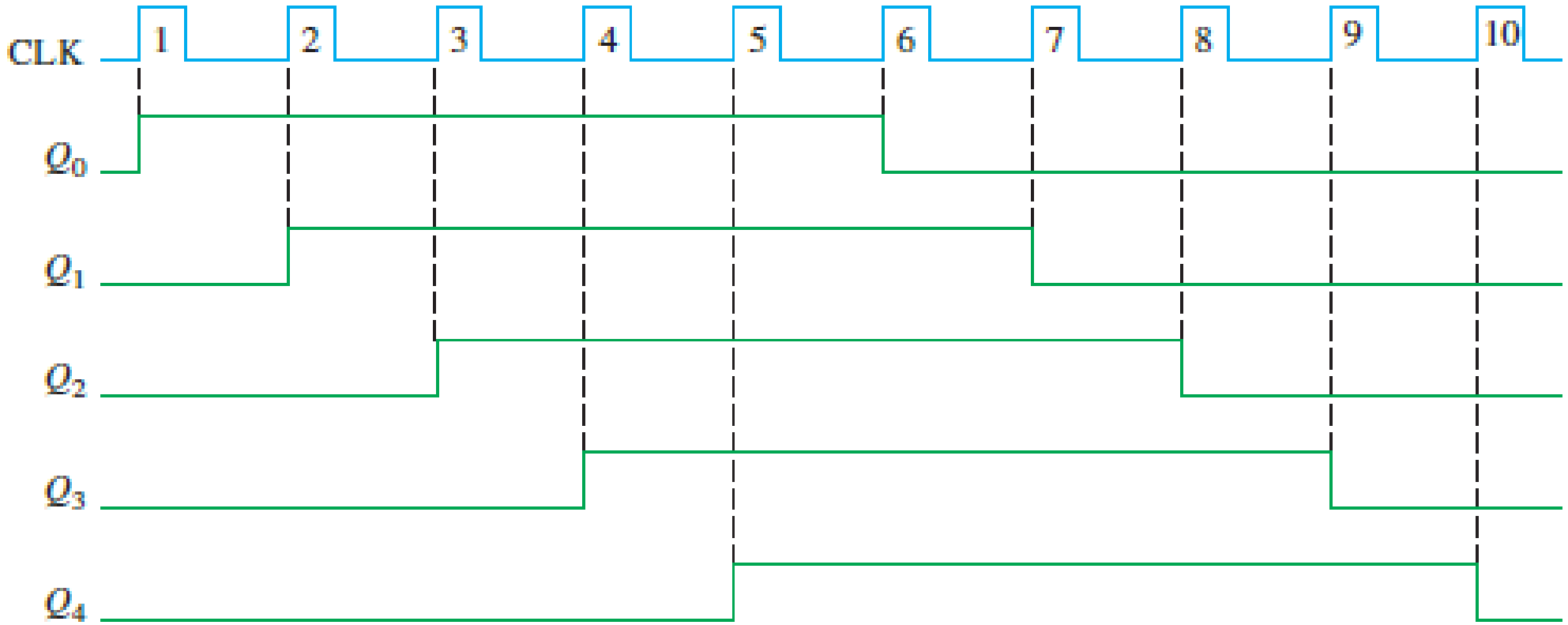
Implementation of 4-bit Johnson Counter



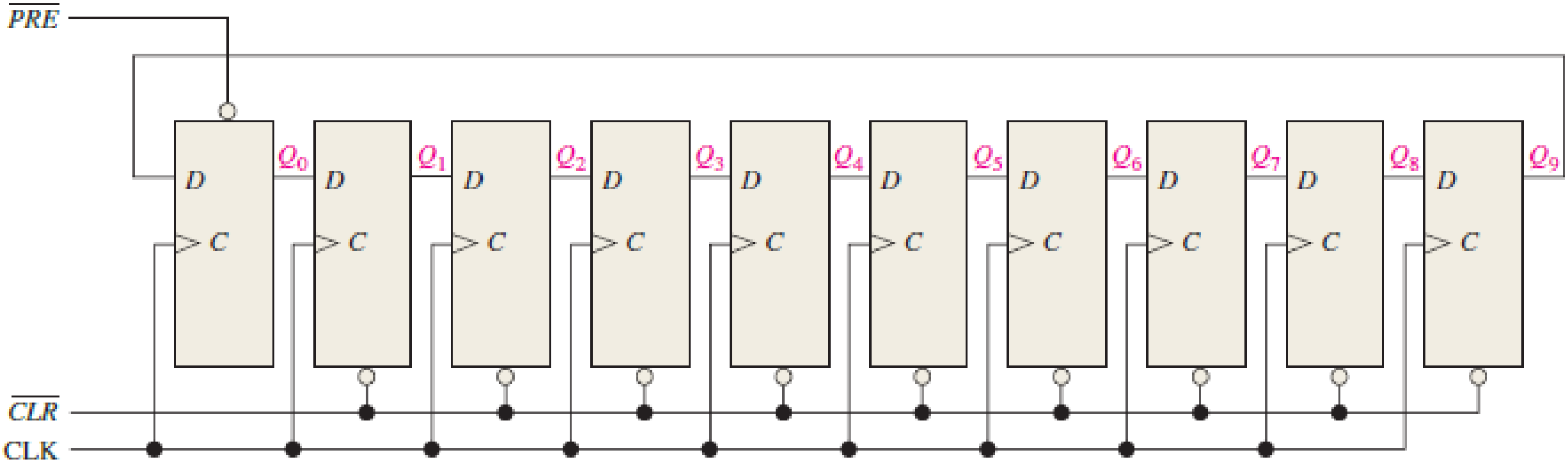
Timing sequence for a 4-bit Johnson counter



Timing sequence for a 5-bit Johnson counter



The Ring Counter

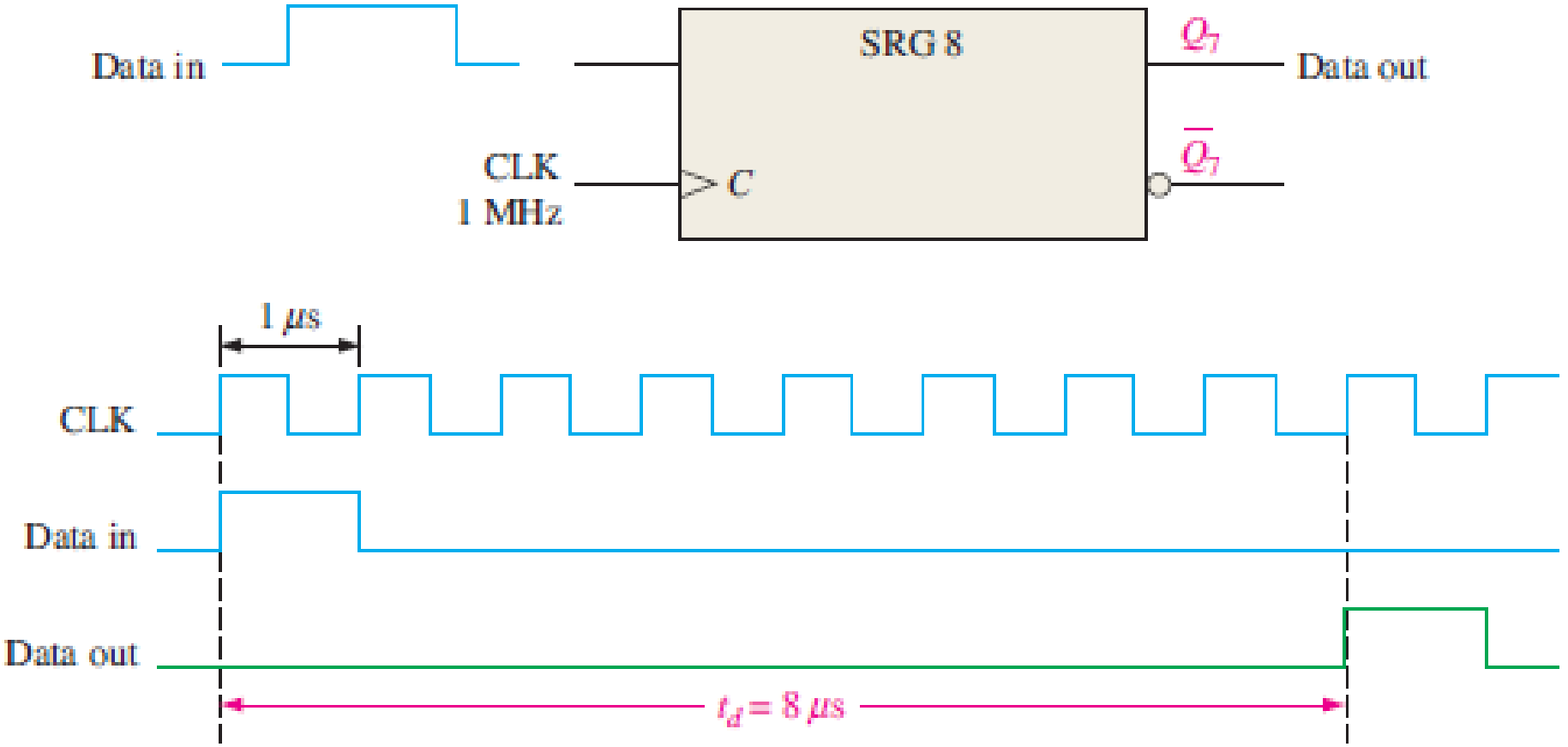


A 10-bit ring counter

Ten-bit ring counter sequence.

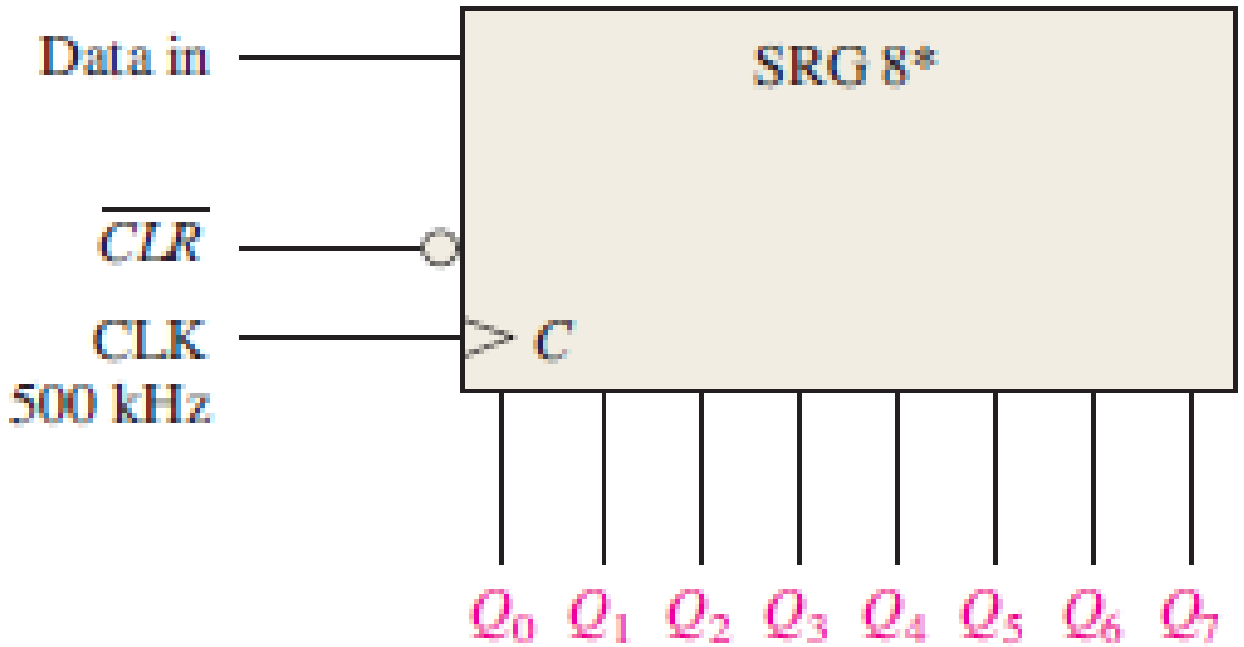
Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

Shift Register Applications -Time Delay

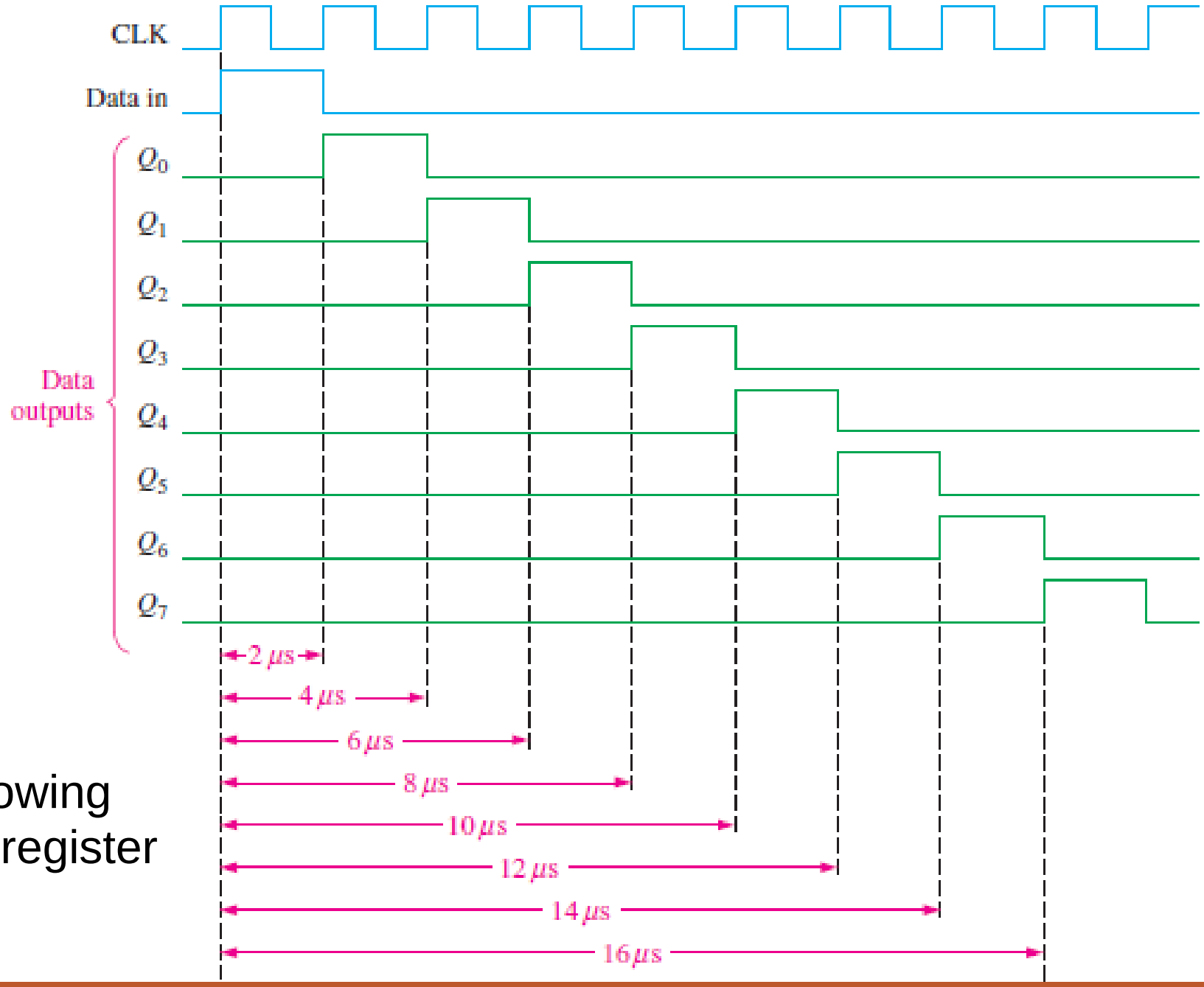


The shift register as a time-delay device

Example: Determine the amount of time delay between the serial input and each output in Figure below. Show a timing diagram to illustrate.

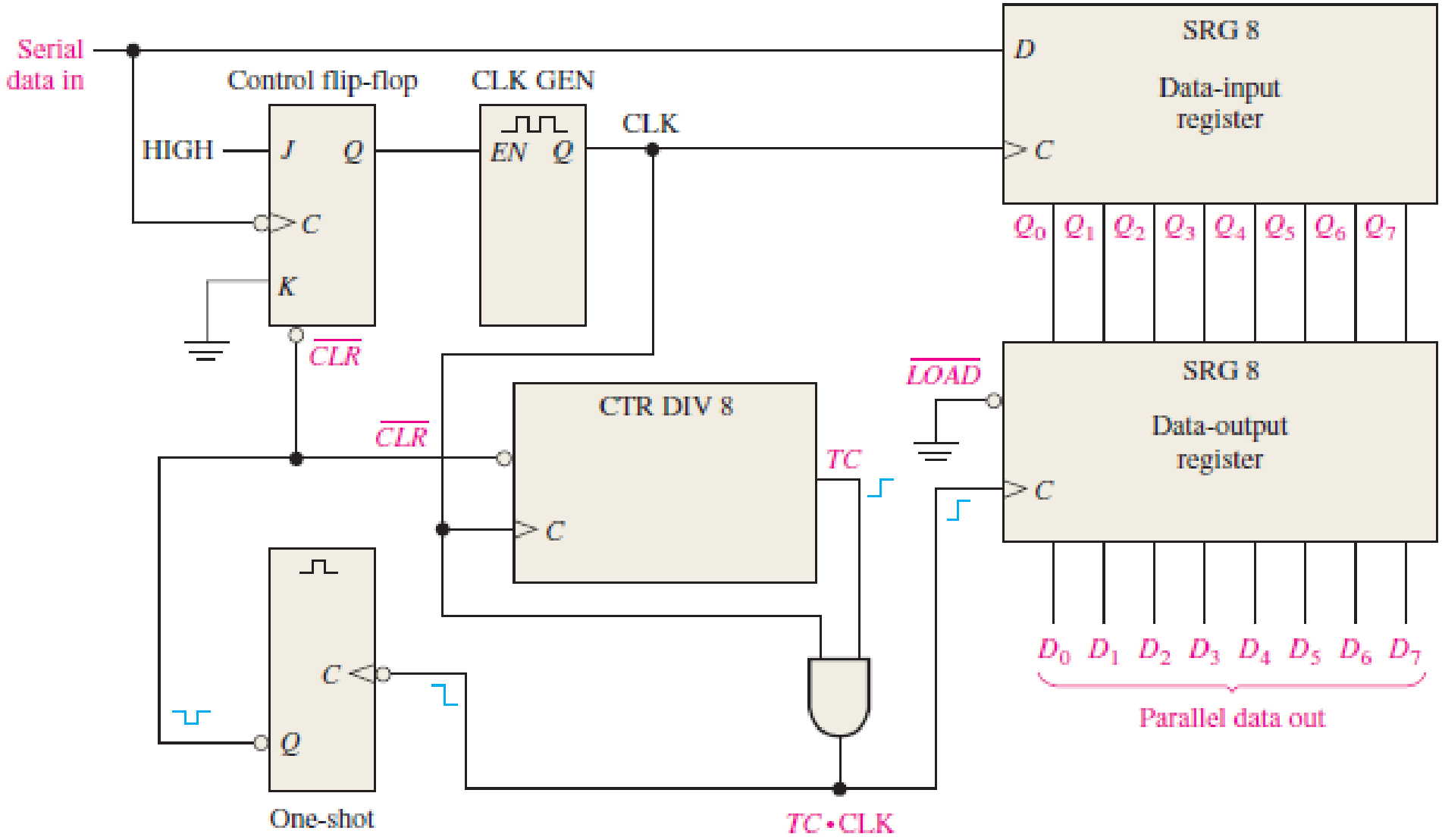


* Data shifts from Q_0 toward Q_7.



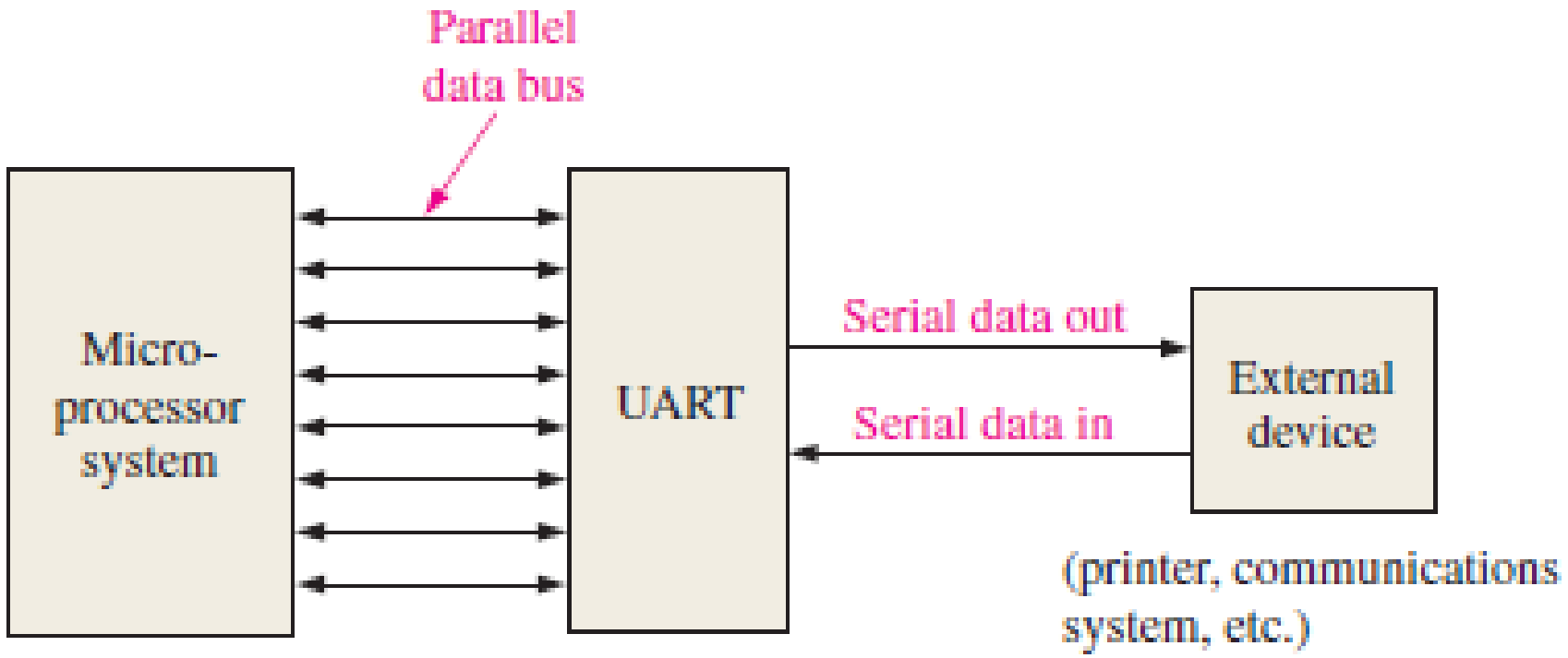
Timing diagram showing time delays for the register

Serial-to-Parallel Data Converter

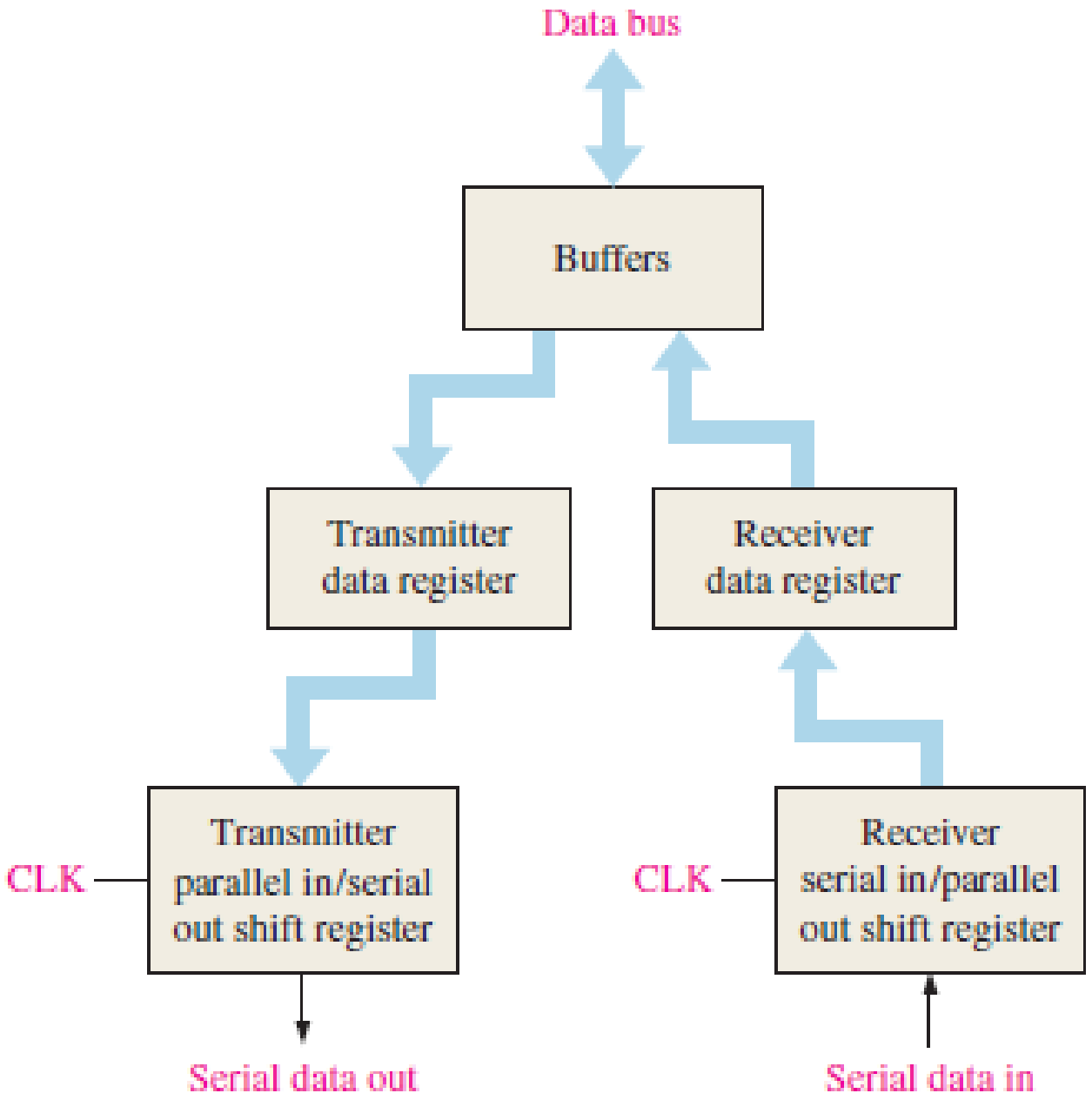


Serial-to-Parallel Data Converter- Serial data format

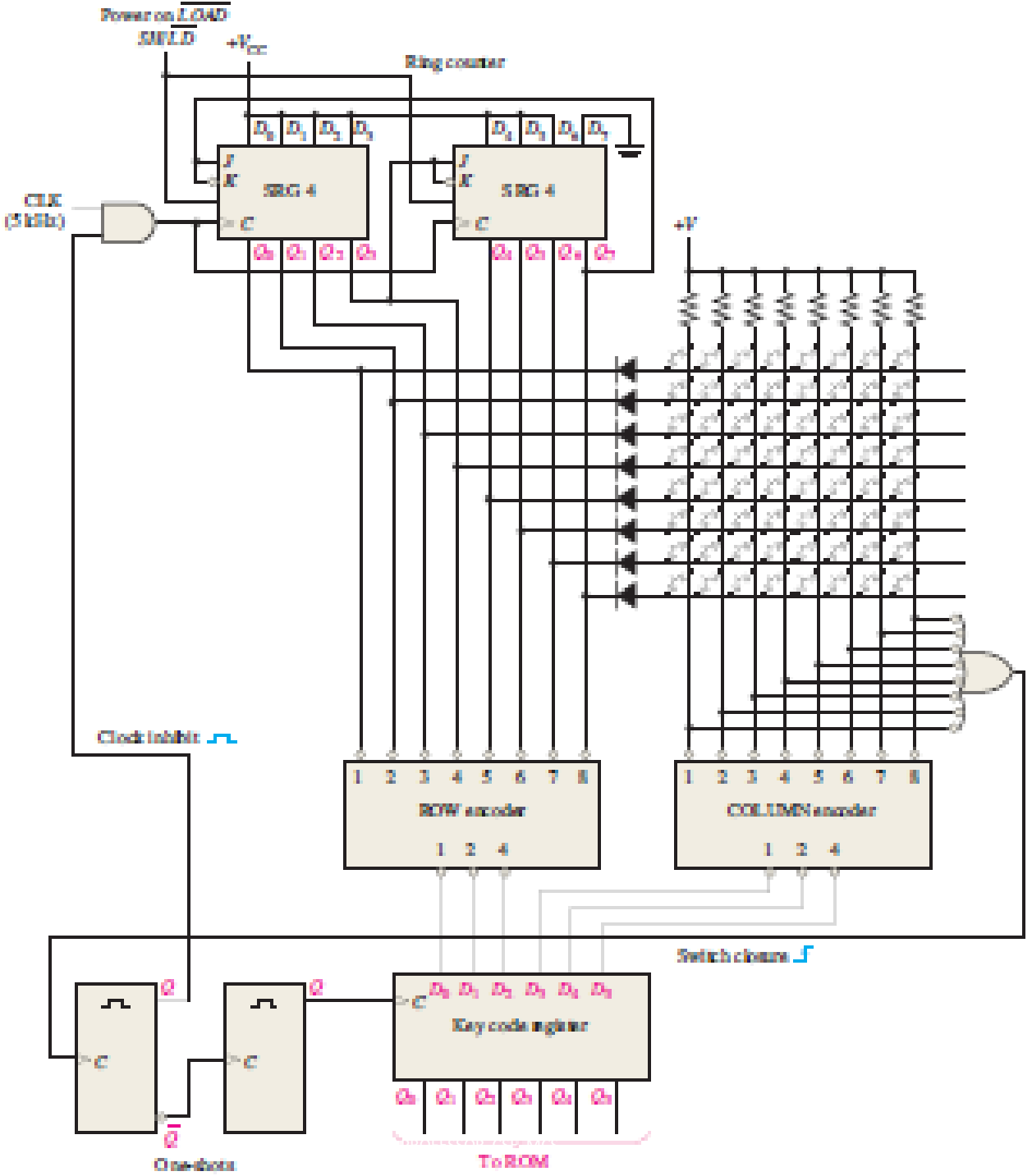
Serial-to-Parallel Data Converter- Universal Asynchronous Receiver Transmitter (UART)



Basic UART block diagram



Serial-to-Parallel Data Converter- Keyboard Encoder



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