Digital Logic Design
(EL-1005)
LABORATORY MANUAL
Spring-2024

LAB 03
Universal Logic Gates

_____ _____ ___

STUDENT NAME ROLL NO SEC

_____

INSTRUCTOR SIGNATURE & DATE

MARKS AWARDED: /10

_____

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), KARACHI

Date: 5th Feb 2024

Prepared By: Muhammad Nouman Hanif

Lab Session 03: Universal Logic Gates

OBJECTIVES:

The objectives of this lab are:

- To study the realization of basic gates using universal gates (NAND gate & NOR gate)
- To learn technology mapping (NAND-NAND & NOR-NOR implementation) and its significance in order to obtain cost effective circuit for implementation

APPARATUS:

- Logic Works
- Logic trainer

COMPONENTS:

ICs 74LS02 (NOR), 74LS00 (NAND)

Introduction:

The design of a combinational circuit starts from the specification of the problem and culminates in a logic diagram or net-list that describes a logic diagram. The procedure involves the specification, formulation, optimization, & technology mapping.

Technology mapping is actually transformation of logic diagram or net-list to a new diagram using the available implementation technology. Typically, NAND and NOR gates are more desirable to use in technology mapping due to the following reasons:

1. NAND and NOR gates are said to be universal gates where universal gate is a gate which can implement any Boolean function without needing any other type of gate.
2. Using universal gate in technology mapping may further reduce cost of optimized logic diagram.
3. Universal gates are easier to fabricate with electronic components.

A convenient way to implement a Boolean function with NAND gates only (NAND-NAND implementation) is to begin with the optimized logic diagram of the circuit consisting of AND, OR and NOT gates. The function is converted to pure NAND logic by replacing each gate in logic diagram with its representation using NAND gates only as shown in figure 5-1. After that, all inverter pairs are cancelled. The same conversion procedure is applied to implement a Boolean function with NOR gates only (NOR-NOR implementation).

Universal Logic Gates:

A. **NAND Gate:**

"It is a device whose output is 1 if at least one or all of the inputs are low (0)"

Symbol:

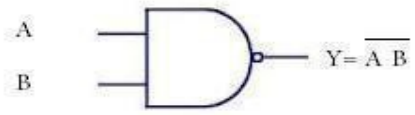


Figure 2 NAND Gate Symbol

Function Table:

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

Table: 1 NAND Gate Truth Table

H= Logic High, L= Logic Low

Connection Diagram:

74LS00 IC contains four 2-input NAND gates. The connection diagram for this IC are shown below:

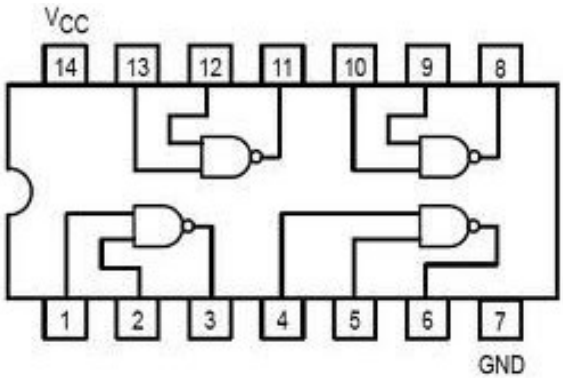


Figure 2 NAND Gate Connection diagram

B. **NOR Gate:**

"It is a device whose output is 1 if all the given inputs are low (0)".

Symbol:

Figure 3 NOR Gate Symbol

Function Table:

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

Table: 2 NOR Gate Truth Table

H= Logic High, L= Logic Low

Connection Diagram:

74LS02 IC contains four 2-input NOR gates. The function table and connection diagram for this IC are shown below:

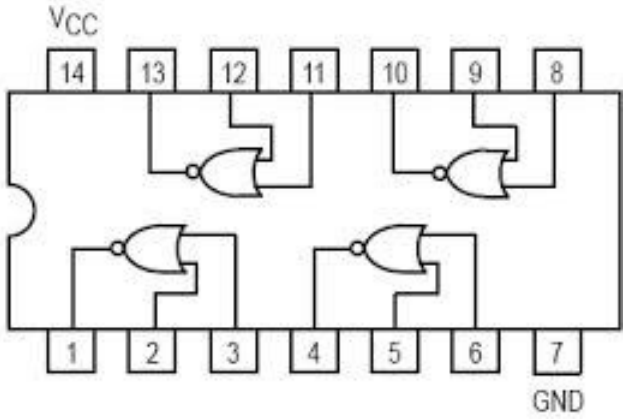


Figure 4 NOR Gate Connection diagram

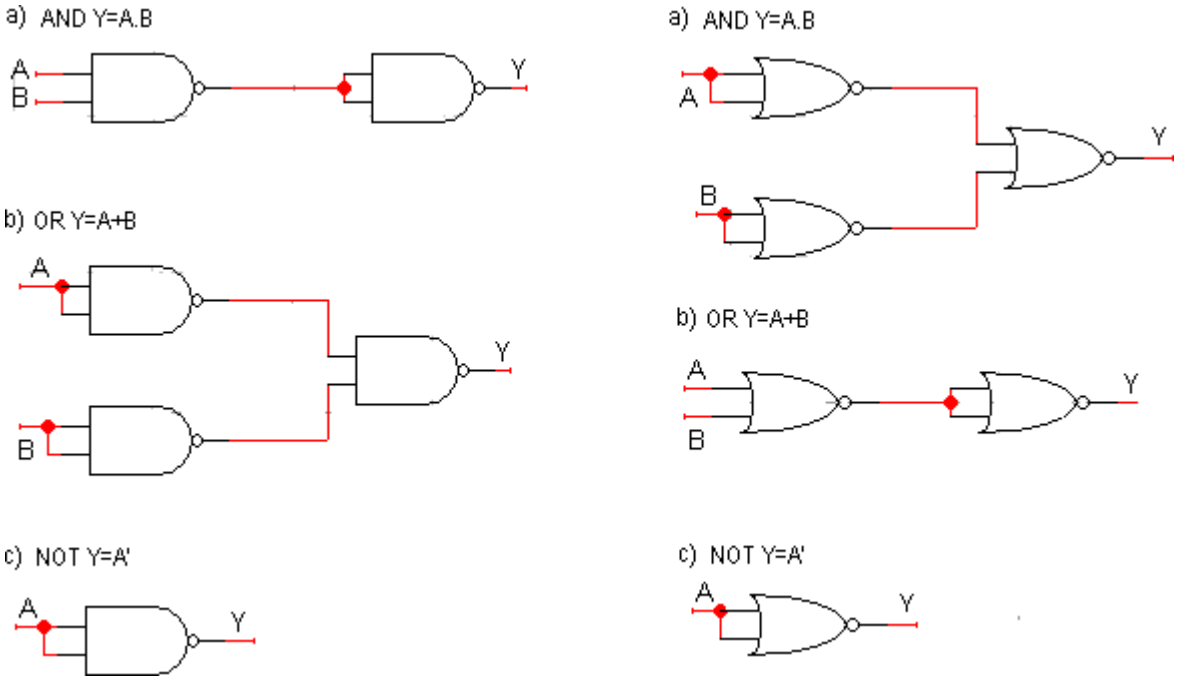


Figure 5 NAND-NAND and NOR-NOR representation of basic logic gates

Lab Tasks

Lab Task#1:

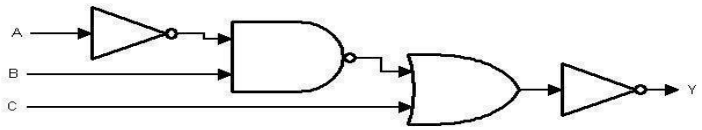
a) Design OR Logic Gate on Logic Works using NAND Gates only.

b) Design AND Logic Gate on Logic Works using NAND Gates only.

c) Design AND Logic Gate on Logic Works using NOR Gates only.

Lab Task#2:

Write the Boolean expression for the logic circuits in the Figure. Also implement the given circuits on Logic Works and draw Truth table:



Lab Task#3:

For the Boolean function $F1 = [\,\overline{(A + B\bar{C})(D + \bar{A}\bar{C})}\,] + CD$ do the following:

a) Draw logic circuit diagram on logic works and draw its truth table.

b) Draw logic circuit diagram on logic works and draw its truth table using only Universal Gates.
(Optional Bonus Lab Task#3 Part (b): 0.5%)

Lab Task#4:

Implement the following scenario/ Logic on Logic Works

In a manufacturing process, there are two tanks storing liquid chemicals. Each tank has a sensor that activates when the chemical level decreases to 25% of its capacity. These sensors output 5V when the tanks are more than one-quarter full, and 0V when the level drops to one-quarter full. The objective is to use a single green LED on an indicator panel to illuminate when both tanks reach the one-quarter full mark. Show how a NAND gate can be used to implement this function.

Lab Task#5:

Implement the following scenario/ Logic on Logic Works

For the process described in Lab Task#4 it has been decided to have a red LED display come on when at least one of the tanks falls to the quarter-full level rather than have the green LED display indicate when both are above one quarter. Design circuit on logic works that shows how this requirement can be implemented.