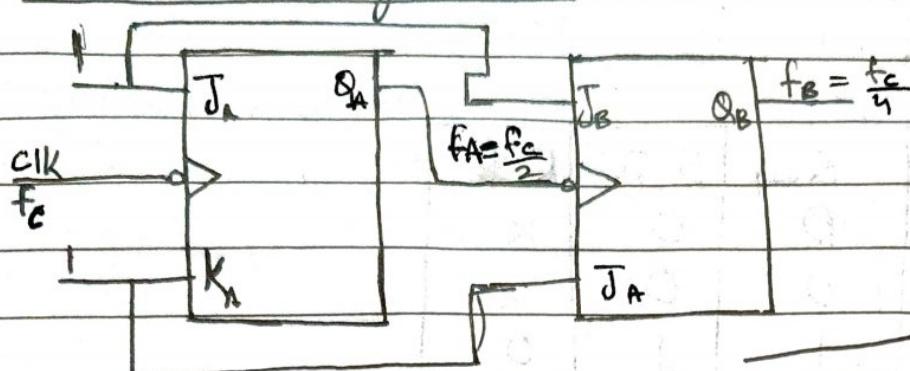
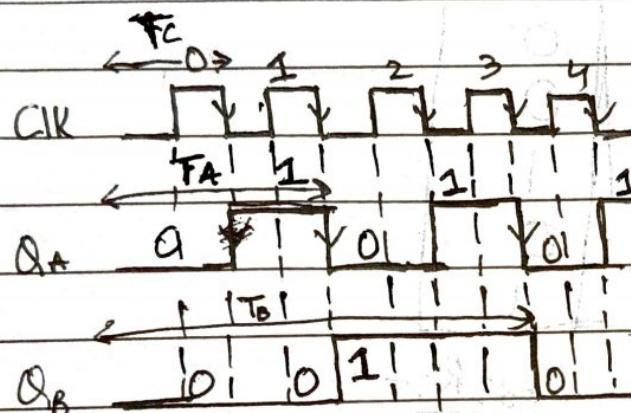


CountersFF as divider by 2 circuit:-

This is

0-3 Counter.



$$T_A = 2T_C$$

$$\frac{1}{f_A} = \frac{2}{f_C}$$

$$f_A = \frac{f_C}{2}$$

$$T_B = 2T_A$$

$$\frac{1}{f_B} = \frac{2}{f_A}$$

$$f_B = \frac{f_A}{2} = \frac{f_C}{4}$$

If we are having n number of F.F where $J=1, K=1$ and they are negative edge triggered, then the output frequency :-

$$\text{output frequency} = \frac{\text{Input frequency}}{2^n}$$

How does this work as a counter

Clk	Q_0	Q_1
0	0	0
1	0	1
2	1	0
3	1	1

why is 4 not considered :-

at 4 ~~the~~, $Q_0=0$, $Q_1=0$, which means it has reset.

Q) for counting from 0-15, 4 ff are required, why?

ans):- $0-15 = 16$ values

$$2^4 = 16$$

$n = 4$, 4 number of flip flops.

$Q_D Q_C Q_B Q_A$

$$0 \text{ } 0 \text{ } 0 \text{ } 0 = 0$$

$$\cdot \text{ } \cdot \text{ } \cdot \text{ } \cdot$$

$$\cdot \text{ } \cdot \text{ } \cdot \text{ } \cdot$$

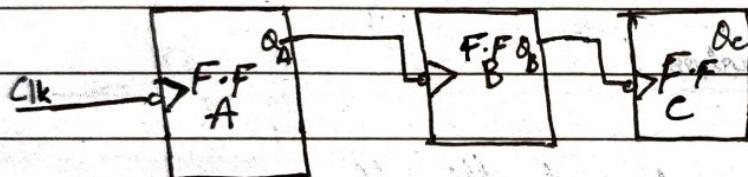
$$1 \text{ } 1 \text{ } 1 \text{ } 1 = 15$$

Types of Counters.Counters

Ripple / Asynchronous Counters

~~Synchronous~~ Synchronous CountersRipple :-

The external clock signal is applied to the first F.F. Then the output of the preceding flip flop is connected to the CLK of the next flip flop.



and so on

depending on number of flip flops.

Synchronous :-

There is no connection b/w output of first flip flop and clock of next flip flop.

Ripple

① Flip flops are connected in such a way that O/P of preceding F.F is the CLK of next F.F.

② F.F are not clocked simultaneously.

③ Circuit is simple for more number of states.

④ Speed is slow as clock is propagated through number of stages.

Synchronous

There is no connection b/w O/P of previous F.F & on next flip flop.

F.F are clocked simultaneously.

It becomes complicated as ~~the~~ number of states increases.

Speed is high as clock is given at the same time.

Asynchronous / Synchronous

Up counters

-1, 2, 3, ...

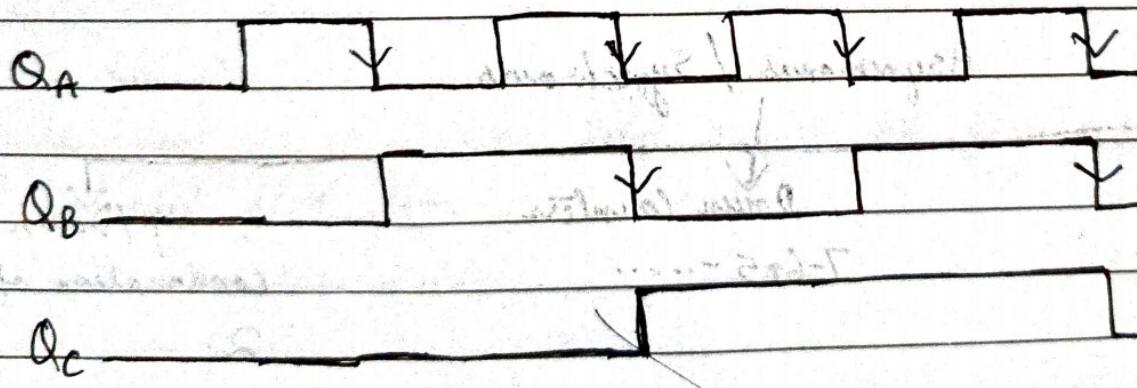
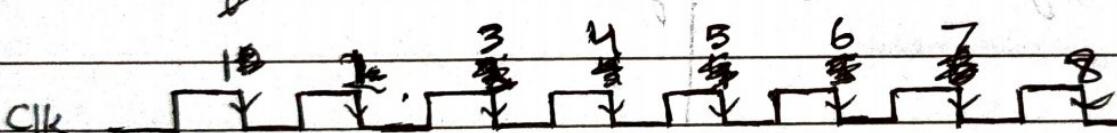
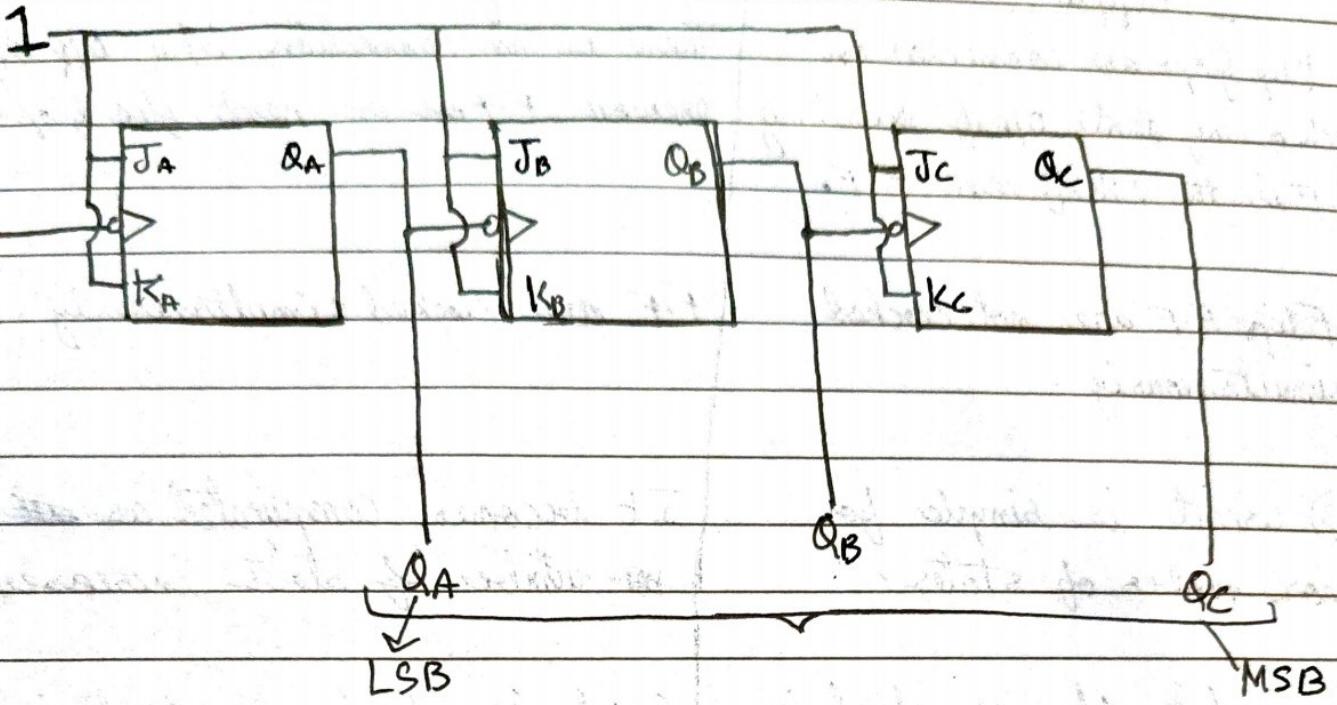
Down counters

7, 6, 5, ...

Up/Down Counters
combination of other

2.

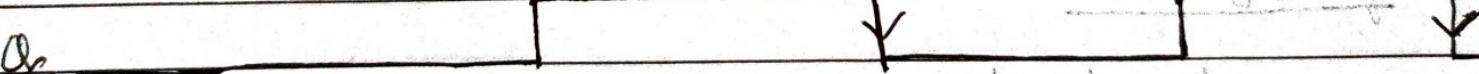
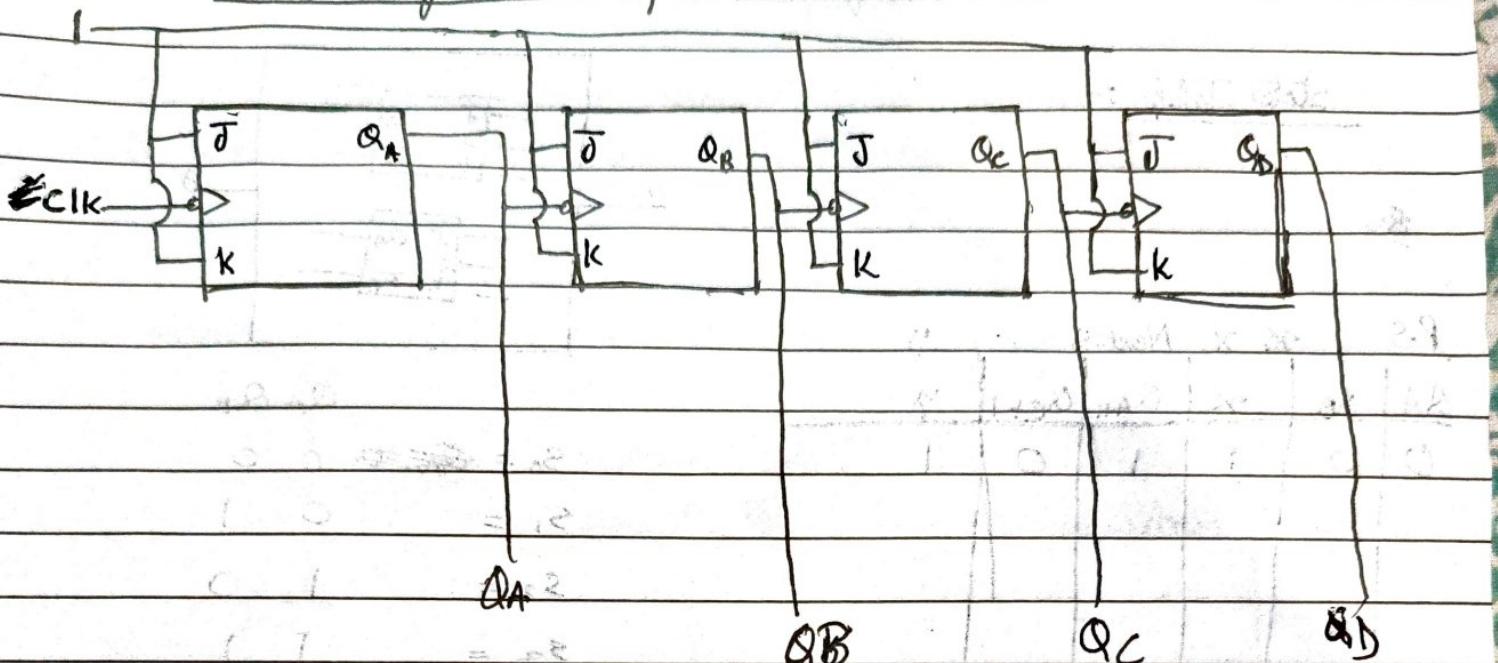
3 Bit Up synchronous Up Counter



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4 bit Asynchronous Up Counter



$B \rightarrow D$

X1

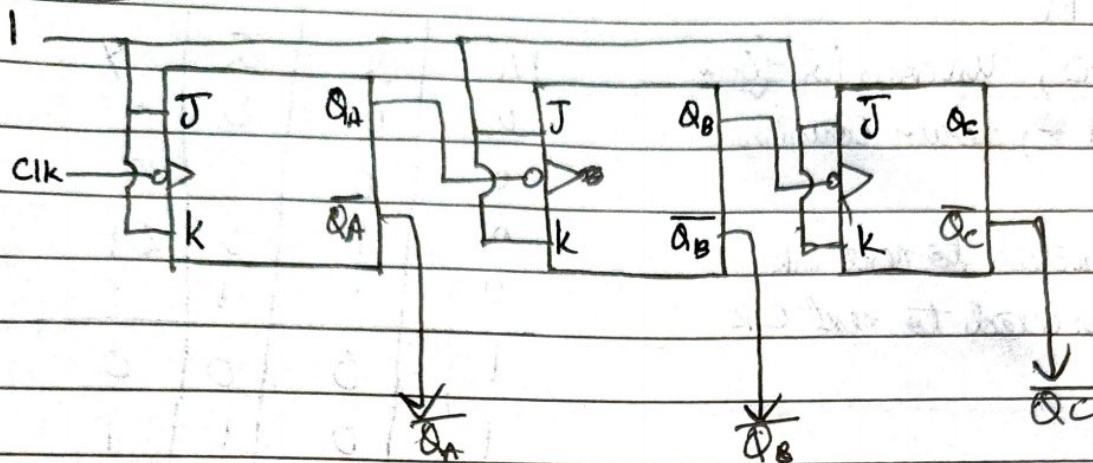
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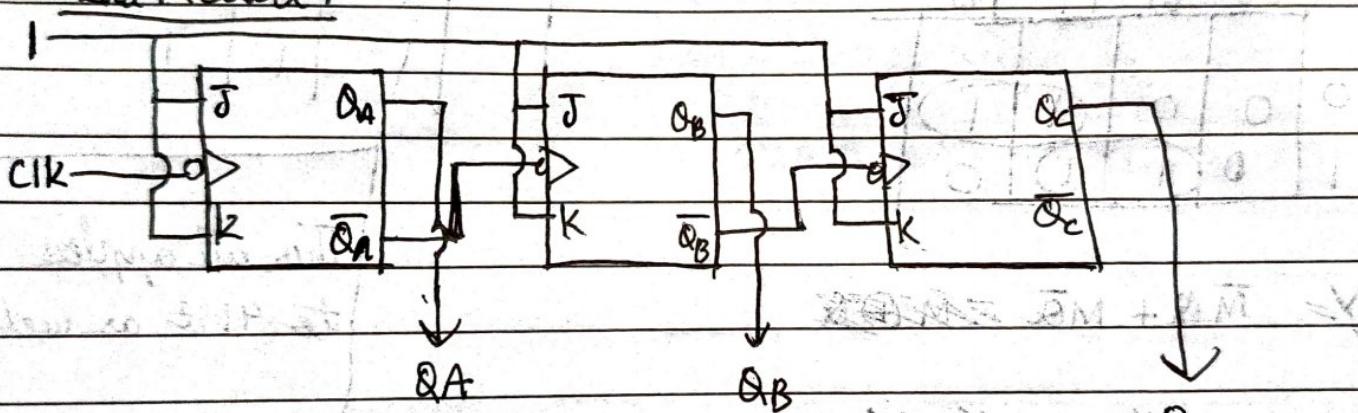
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3/4 bit Asynchronous down counter

3 bit



2nd Method:-



* The same thing from above can be done for 4bit counters.

3 bit and 4 bit updown asynchronous counters

mode = M

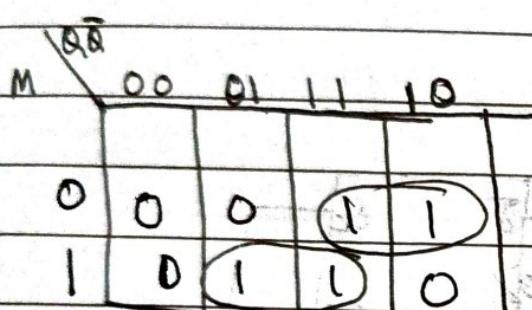
when $M=0$, up counter

$M=1$, down counter

$M=0$, Q connected to next CLK

$M=1$, \bar{Q} connected to next CLK

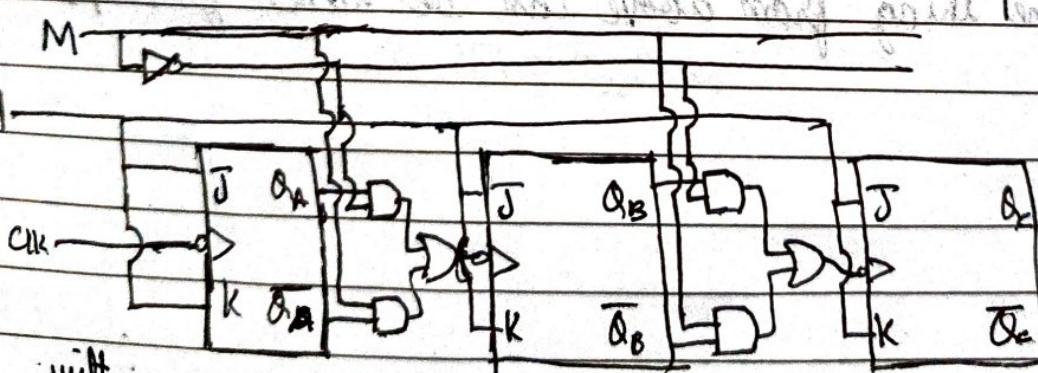
M	Q	\bar{Q}	Y
0	0	1	0
0	0	1	0
0	1	0	1
0	1	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	0



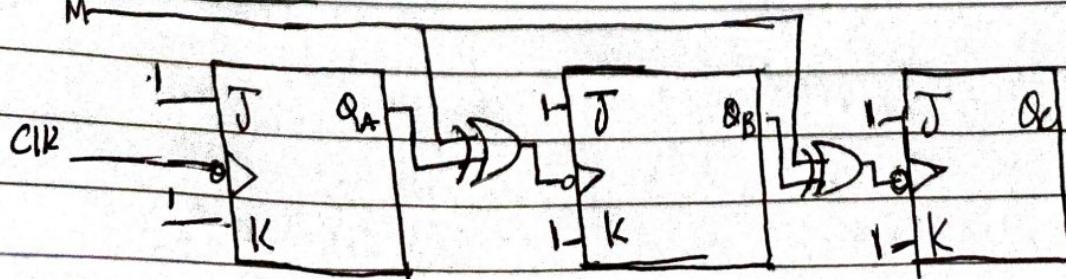
$$Y = \overline{M}Q + M\bar{Q}$$

This all applies
to 4bit as well.

Y is the combinational circuit used.



with XOR Gate



Modulus of counter and counting up to a particular value.

~~Mod~~ MOD-4 counter means , 2 bit counter

Mod -8 counter means , 3 bit counter

~~n~~ n bit counter = ~~Mod~~ MOD- 2^n counter

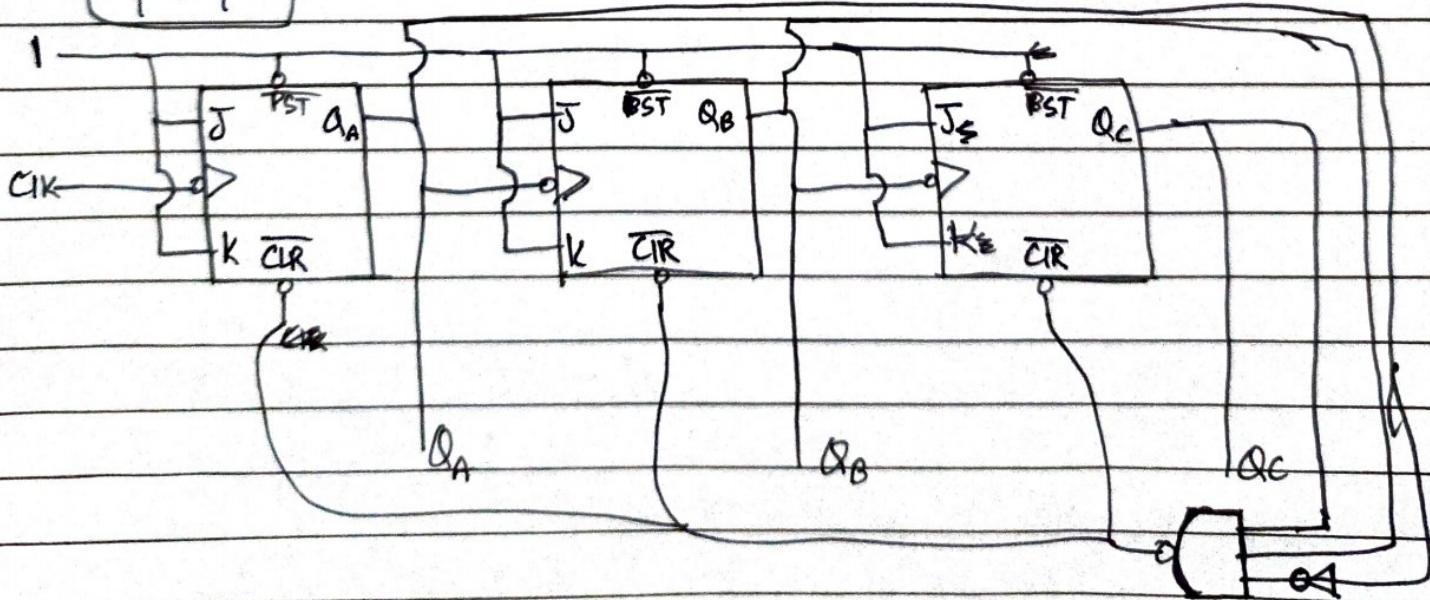
Counting up to a particular value

count up to 5 (0 - 5) ~~3~~ / Mod-6 counter.

000
001
010
011
100
101

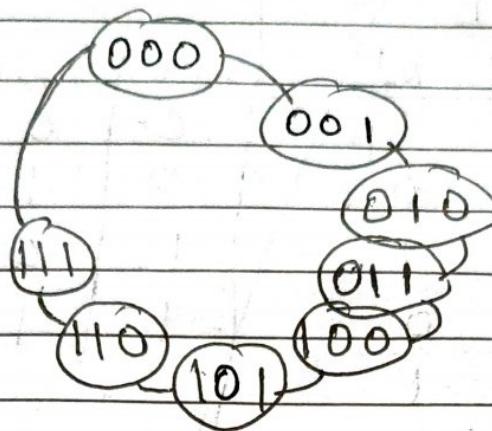
Mod-6 Counter

Explanation :- The output values must reset when 6 (110) is reached. as such as soon as 110 occurs, The CLR gets low signal and activates . setting everything to 0.



Synchronous Steps to Design Counters

① State Diagram



② The state Table

Current State			Next State		
Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

③ The chosen flip flop ~~transition table~~ excitation table

D flip flop:-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

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Step 4

 ~~$D_0 = D_0$~~ K-Map

$D_1 = \bar{Q}_2 Q_0$	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D_2	D_1	D_0
$D_0 = D_0$	0	0	0	0	0	1	0	0	1
$D_0 = D_0$	0	0	1	0	1	0	0	1	0
$D_0 = D_0$	0	1	0	0	1	1	0	1	1
$D_0 = D_0$	0	1	1	1	0	0	1	0	0
$D_0 = D_0$	1	0	0	1	0	1	1	0	1
$D_0 = D_0$	1	0	1	1	1	0	1	1	0
$D_0 = D_0$	1	1	0	1	1	1	1	1	1
$D_0 = D_0$	1	1	1	0	0	0	0	0	0

 D_2

$Q_1 Q_0$		P_1				
Q_2	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10
0	0 0 0 0	0 0 0 0	1 0 0 0	1 0 0 0	0 0 0 0	0 0 0 0
1	0 1 0 1	1 0 0 1	0 1 0 1	0 1 0 1	0 0 0 0	0 0 0 0

 P_1

$Q_1 Q_0$		D_2				
Q_2	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10
0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
1	0 1 0 1	1 0 0 1	0 1 0 1	0 1 0 1	0 0 0 0	0 0 0 0

$$D_2 = Q_2 \bar{Q}_1 + Q_2 \bar{Q}_0 + \bar{Q}_2 Q_1 Q_0$$

$$\begin{aligned} D_1 &= \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0 \\ &= Q_1 \oplus Q_0 \end{aligned}$$

 D_2

$Q_1 Q_0$		D_1				
Q_2	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10	00 01 11 10
0	1 1 0 0	0 0 1 1	0 0 1 1	0 0 1 1	0 0 1 1	0 0 1 1
1	1 0 1 0	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1	0 1 0 1

$$D_0 = \bar{Q}_0$$

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3-Bit Up/Down Synchronous Counter (T-Flip flop)

T-T (T-Flip flop)

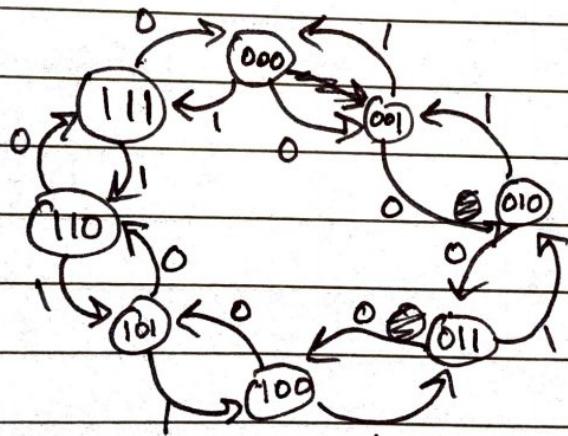
Transition Table (T-Flip flop)

CIR	T	Q_{n+1}
0	X	Q_n
1	0	Q_n
1	1	\bar{Q}_n

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

$$T = Q_{n+1} \oplus Q_n$$

State diagram



* assuming $M=0$ (up counting)
 $M=1$ (down counting)

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M	Q_C	Q_B	Q_A	Q_C^+	Q_B^+	Q_A^+	T_C	T_B	T_A
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1

 $T_C =$

$M Q_C$	00	01	11	10
00	0	0	(0)	0
01	0	0	(1)	0
10	(1)	0	0	0
11	(0)	0	0	0

 $T_B =$

$M Q_A$	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

 $T_A =$

$M Q_C$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

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$$T_C = \overline{M} Q_B Q_A + M \overline{Q}_B \overline{Q}_A$$

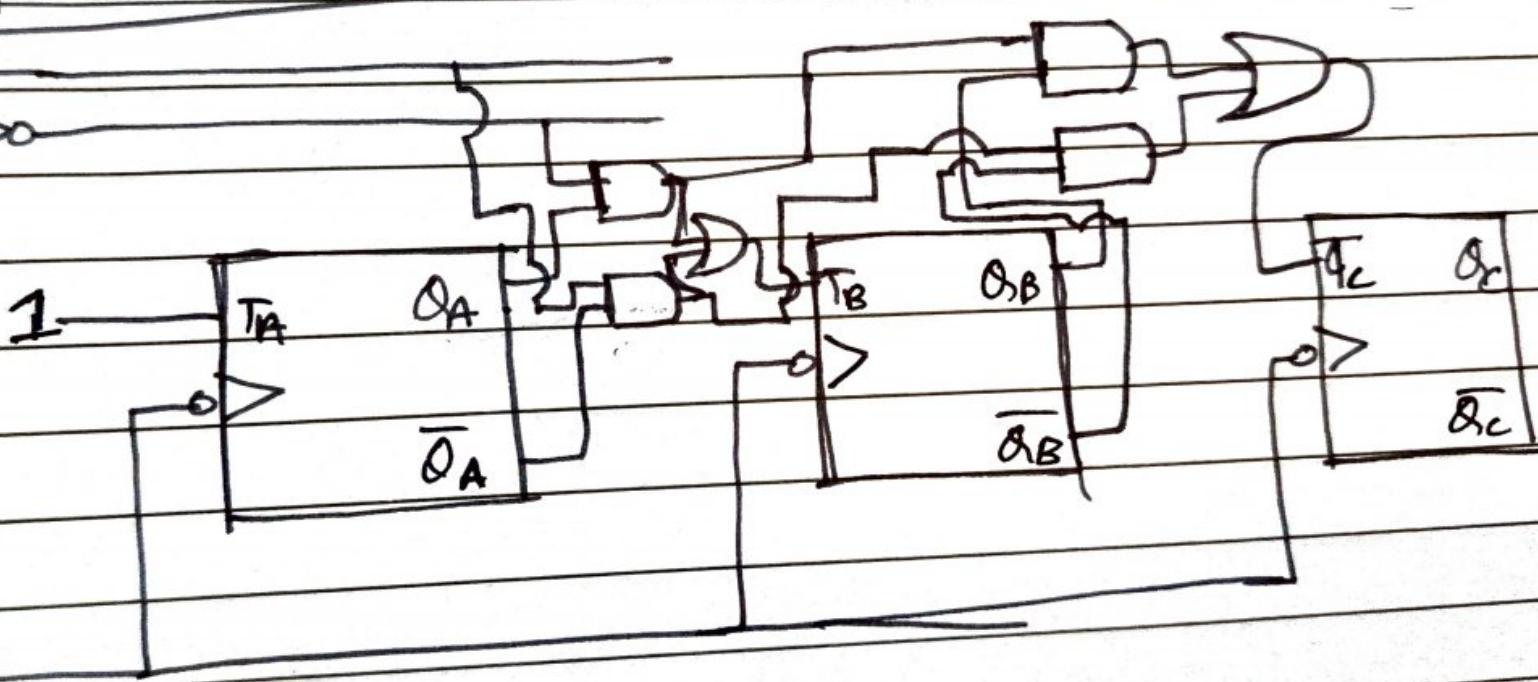
$$T_B = \overline{M} Q_A + M \overline{Q}_A$$

$$T_A = 1$$

M



1



Clk

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Important points for counter

and

- ① Negative edge Triggered ~~and~~ Q is next clock . Then it is up counter.
- ② Negative edge Triggered and \bar{Q} is next clock . Then it is down counter.
- ③ Positive edge Triggered and Q is next clock . Then it is down counter.
- ④ Negative edge Triggered and \bar{Q} is next clock . Then it is up counter.