Digital Logic Design
(EL-1005)
LABORATORY MANUAL
Spring-2024

LAB 07
Binary Multiplier Hardware Implementations

STUDENT NAME	ROLL NO	SEC

INSTRUCTOR SIGNATURE& DATE

MARKS AWARDED: /10

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Binary Multiplier Hardware Implementations

OBJECTIVES:

After completing this lab, you would be able to know

- To study the basic operation and design of multiplier Circuits
- To learn how to implement 2x2 bit multiplier circuit.
- To learn how to implement 3x3 bit multiplier circuit.

APPARATUS:

- Logic Trainer, Logic Works

COMPONENTS:

ICs 74LS00 (NAND), 74LS02 (NOR), 74LS04 (NOT), 74LS08 (AND), 74LS32 (OR), 74LS86 (XOR), 74LS266 (XNOR)

Introduction:

A multiplier is a combinational logic circuit that we use to multiply binary digits. Just like the adder and the subtractor, a multiplier is an arithmetic combinational logic circuit. It is also known as a **binary multiplier or a digital multiplier**.

Multiplication in binary Number system is like its decimal counterpart. Two numbers A and B can be multiplied by partial products: for each digit in B, the product of that digit in A is calculated and written on a new line, shifted leftward so that its rightmost digit lines up with the digit in B that was used. The sum of all these partial products gives the final result. Since there are only two digits in binary, there are only two possible outcomes of each partial multiplication:

- If the digit in B is 0, the partial product is also 0.
- If the digit in B is 1, the partial product is equal to A.

How does binary multiplication work and how to design a 2-bit multiplier?

Binary multiplication works just like normal multiplication. There are four main rules that are quite simple to understand:

0 x 0 = 0

0 x 1 = 0

1 x 0 = 0

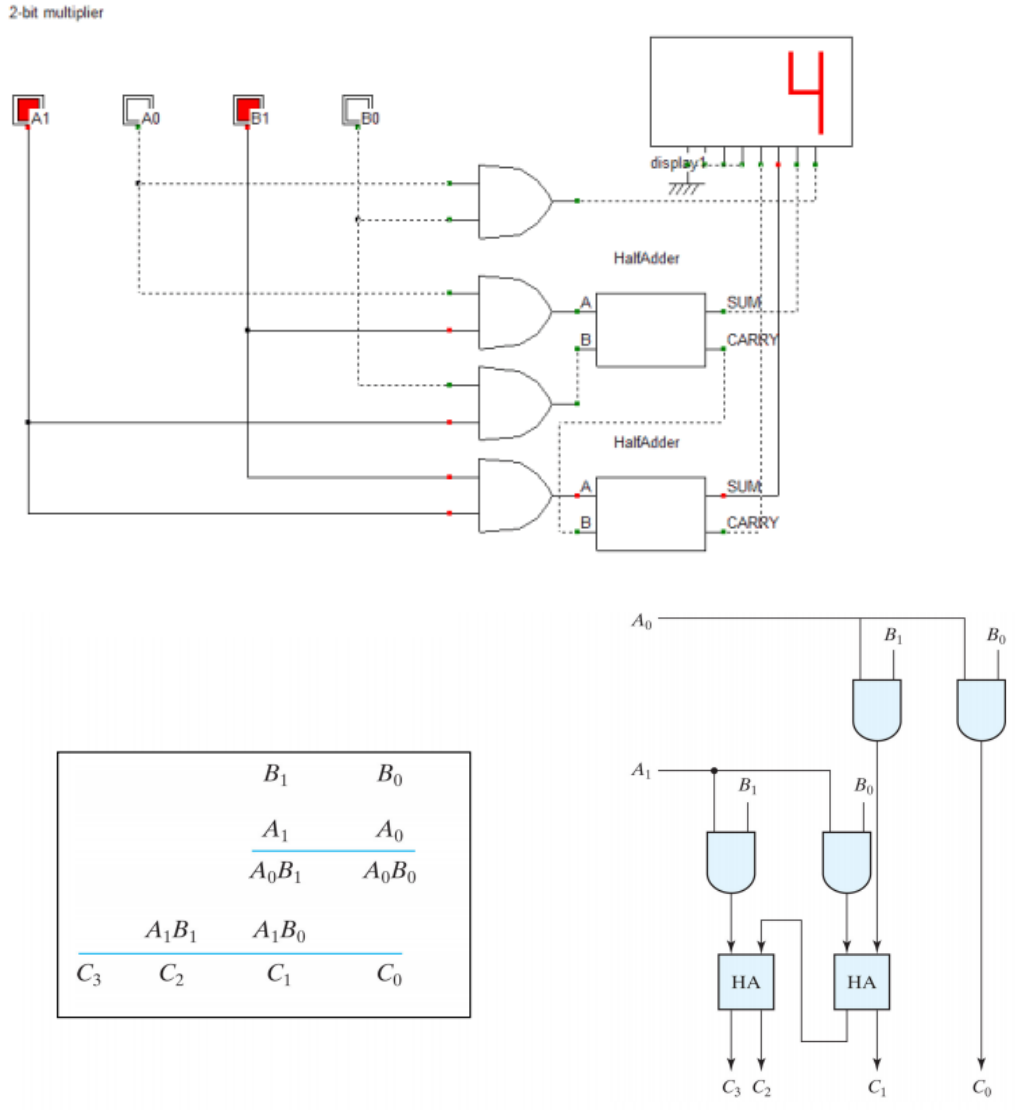
1 x 1 = 1

Suppose you have two binary digits A1A0 and B1B0, here's how that multiplication would take place.

		A1	A0
		B1	B0
		A1B0	A0B0
A1B1		A0B1	X
A1B1+C		A0B1+A1B0	A0B0

As the number of bits increases, we keep shifting each successive partial product to the left by 1 bit. In the end, we add the digits while keeping in mind the carry that might generate.

Based on the above equation, we can see that we need four AND gates and two half adders to design the combinational circuit for the multiplier. The AND gates will perform the multiplication, and the half adders will add the partial product terms. Hence the circuit obtained is as follows.



2-bit Binary Multiplier