Name: EE-272L Digital Systems Design

Reg. No.. Marks Obtained: _____

Lab Manual

DSD Lab Manual Evaluation Rubrics

Assessment	Total Marks	Marks Obtained	0-30%	30-60%	70-100%
Code Organization	3		No Proper Indentation and descriptive naming, no code organization. Zero to Some understanding but not working	Proper Indentation or descriptive naming or code organization. Mild to Complete understanding but not working	Proper Indentation and descriptive naming, code organization. Complete understanding, and proper working
Simulation	5		Simulation not done or incorrect, without any understanding of waveforms	Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms	Working simulation without any errors, etc and complete understanding of waveforms
FPGA	2		Not implemented on FPGA and questions related to synthesis and implementation not answered.	Correctly Implemented on FPGA or questions related to synthesis and implementation answered.	Correctly Implemented on FPGA and questions related to synthesis and implementation answered.

Lab Task

For this lab, you are required to create a module containing two 2-bits inputs a and b such that we observe the following output on the tri-color LED.

$$F = \begin{cases} a > b & Cyan \\ a = b & Purple \\ a < b & Yellow \end{cases}$$

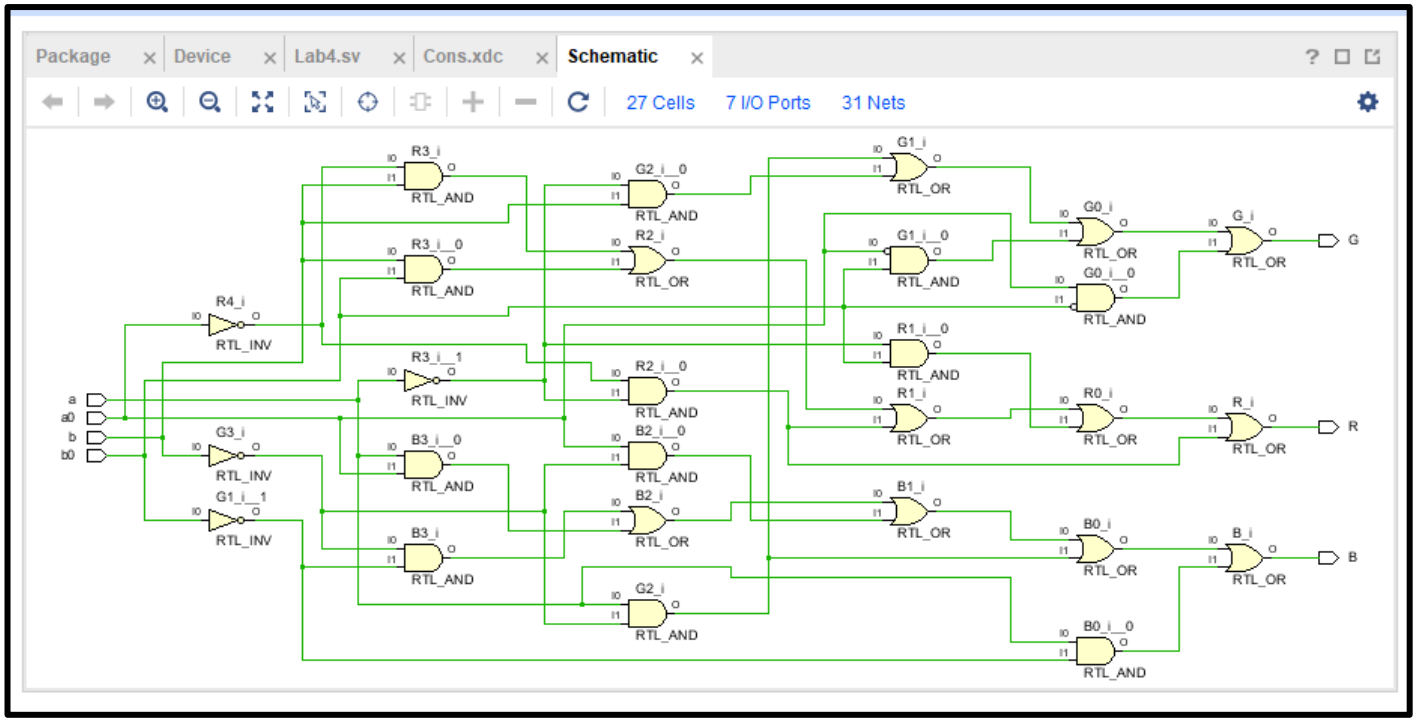
For this purpose, first develop the truth table according to the requirement and then get the minimized expression for the output using K-maps. Next, implement the design on Vivado.

Deliverables

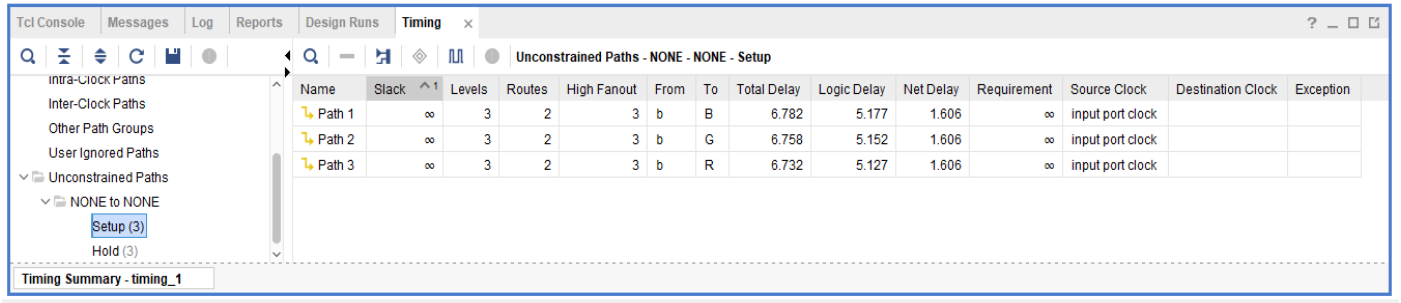
a) Truth table:

	a	a0	b	b0	R	G	B
0	0	0	0	0	1	0	1
1	0	0	0	1	1	1	0
2	0	0	1	0	1	1	0
3	0	0	1	1	1	1	0
4	0	1	0	0	0	1	1
5	0	1	0	1	1	0	1
6	0	1	1	0	1	1	0
7	0	1	1	1	1	1	0
8	1	0	0	0	0	1	1
9	1	0	0	1	0	1	1
10	1	0	1	0	1	0	1
11	1	0	1	1	1	1	0
12	1	1	0	0	0	1	1
13	1	1	0	1	0	1	1
14	1	1	1	0	0	1	1
15	1	1	1	1	1	0	1

d) Circuit diagram inferred by the Xilinx Vivado:

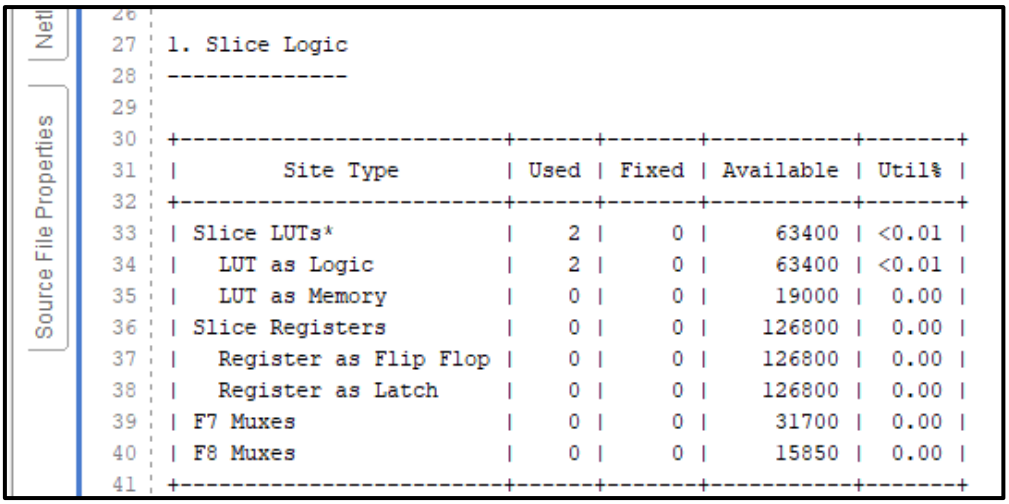


e) Maximum Combinational delay:



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 1	∞	3	2	3	b	B	6.782	5.177	1.606	∞	input port clock		
Path 2	∞	3	2	3	b	G	6.758	5.152	1.606	∞	input port clock		
Path 3	∞	3	2	3	b	R	6.732	5.127	1.606	∞	input port clock		

f) Utilization Report:



1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	2	0	63400	<0.01
LUT as Logic	2	0	63400	<0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

System Verilog code: