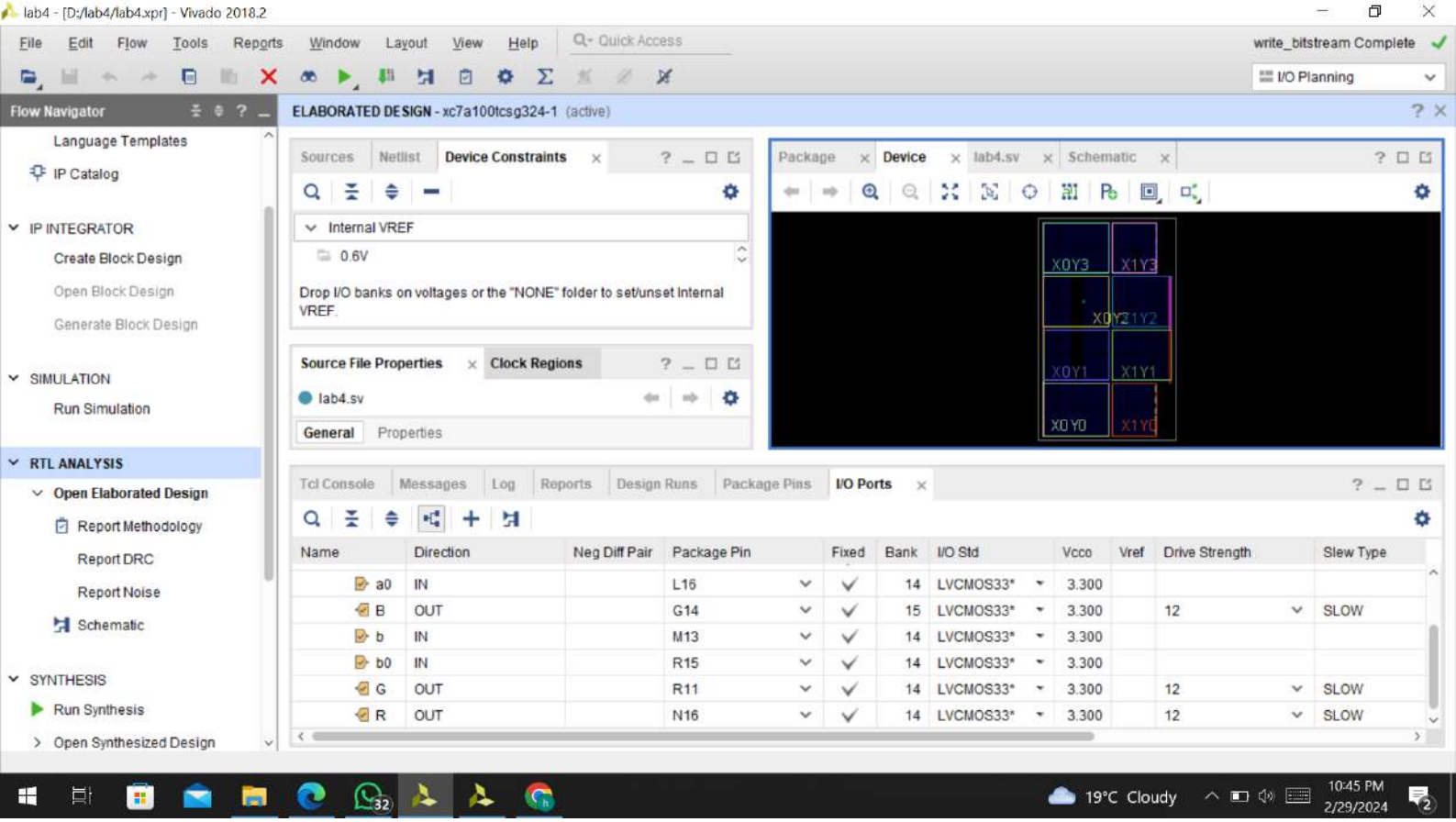
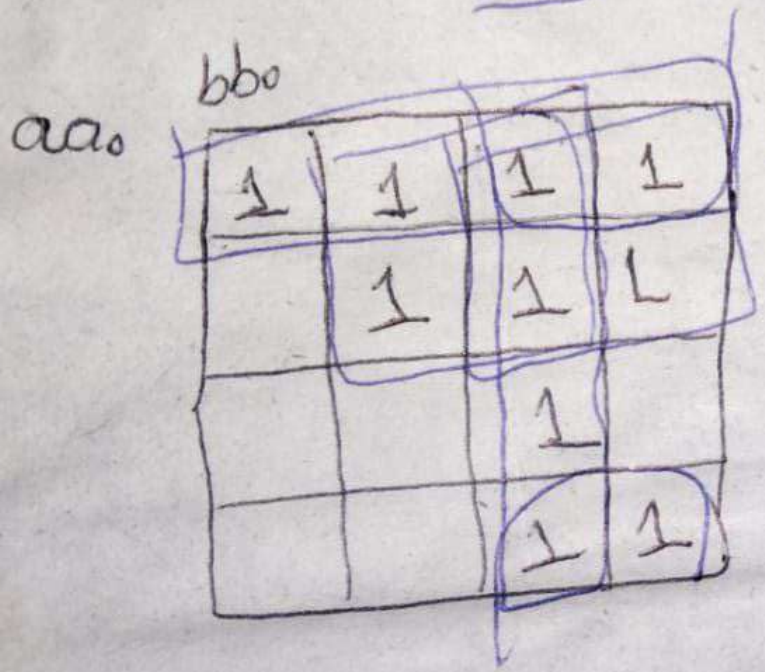
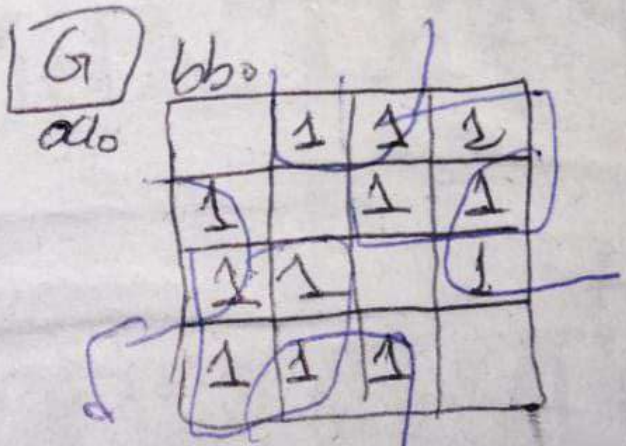

lab4 - [D:/lab4/lab4.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
I/O Planning
Flow Navigator
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
ELABORATED DESIGN - xc7a100tcsg324-1 (active)
Sources Netlist Device Constraints
Internal VREF
0.6V
Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.
Source File Properties Clock Regions
lab4.sv
General Properties
Package Device lab4.sv Schematic
X0Y3 X1Y3
X0Y2 X1Y2
X0Y1 X1Y1
X0Y0 X1Y0
Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports
Name Direction Neg Diff Pair Package Pin Fixed Bank I/O Std Vcco Vref Drive Strength Slew Type
a0 IN L16 14 LVCMOS33* 3.300
B OUT G14 15 LVCMOS33* 3.300 12 SLOW
b IN M13 14 LVCMOS33* 3.300
b0 IN R15 14 LVCMOS33* 3.300
G OUT R11 14 LVCMOS33* 3.300 12 SLOW
R OUT N16 14 LVCMOS33* 3.300 12 SLOW
19°C Cloudy
10:45 PM
2/29/2024

R



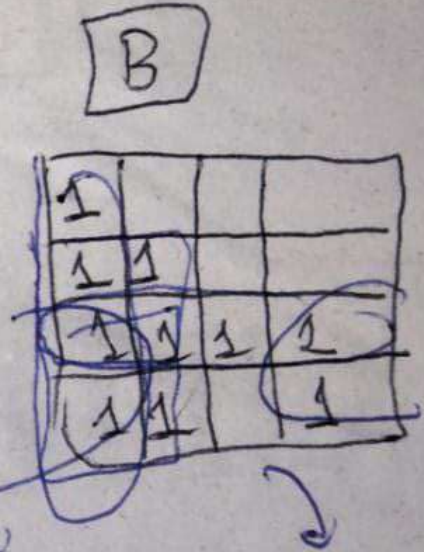
$\rightarrow \bar{a}_0 b + b b_0 + \bar{a}_0 \bar{a} + \bar{a} \cdot b_0 + \bar{b_0} \cdot a$

G



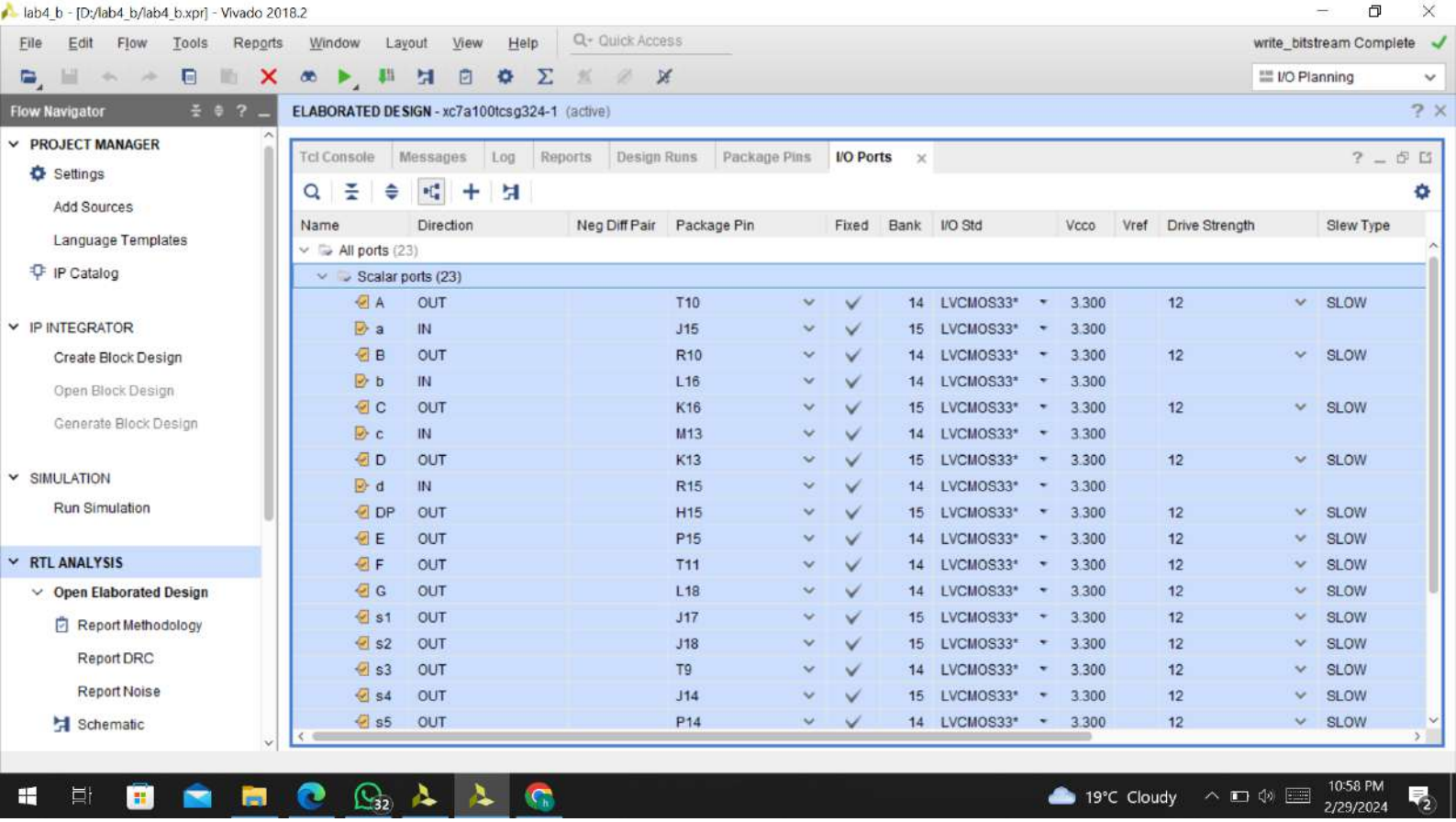
$a\bar{b} + \bar{a}b + \bar{a}_0 b_0 + a_0 \bar{b_0}$

B



$\bar{b}\bar{b_0} + aa_0 + a_0 b$

$a\bar{b} + a\bar{b_0}$


lab4_b - [D:/lab4_b/lab4_b.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
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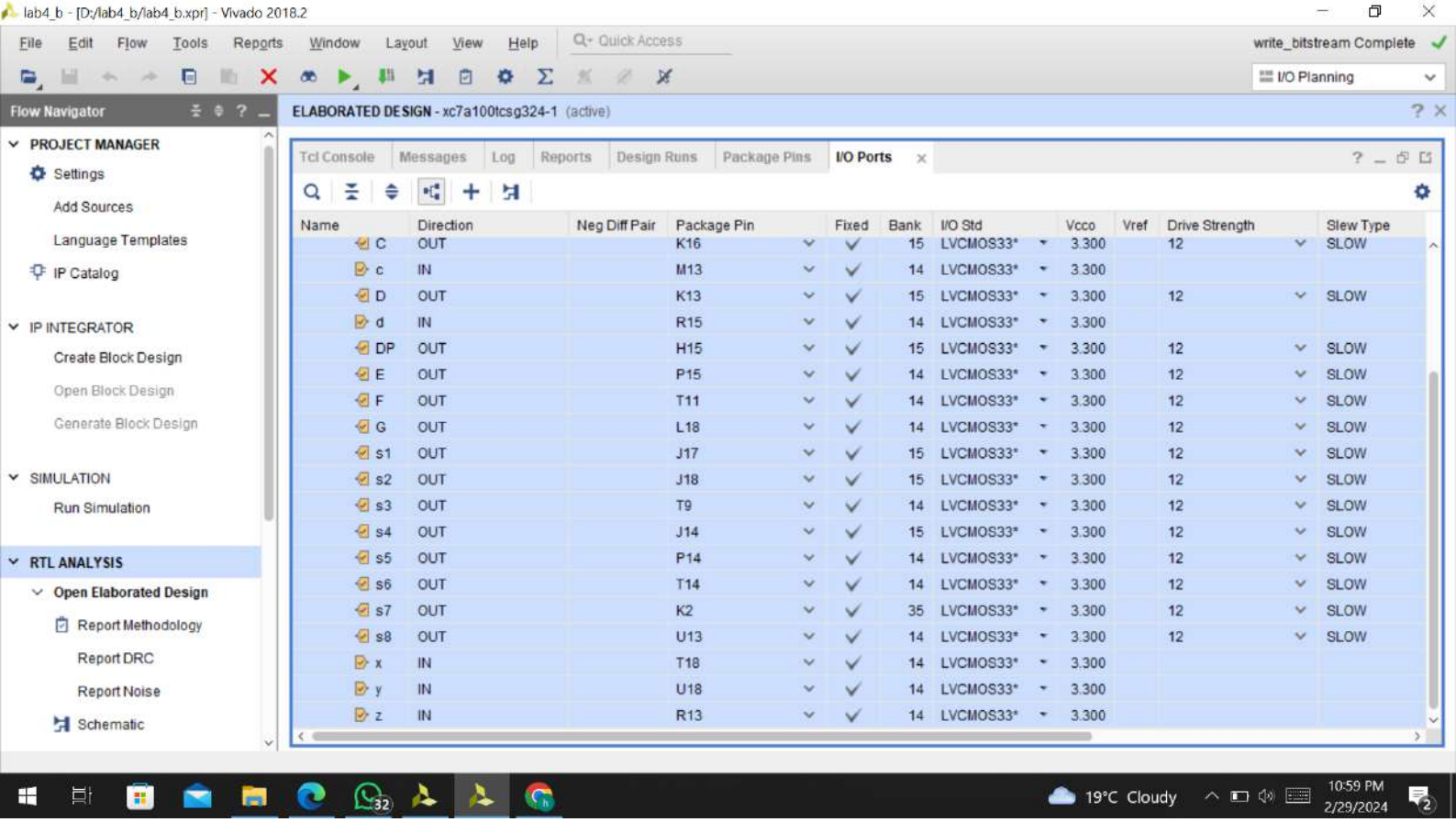
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a100tcsg324-1 (active)
Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports
Name Direction Neg Diff Pair Package Pin Fixed Bank I/O Std Vcco Vref Drive Strength Slew Type
All ports (23)
Scalar ports (23)
A OUT T10 14 LVCMOS33* 3.300 12 SLOW
a IN J15 15 LVCMOS33* 3.300
B OUT R10 14 LVCMOS33* 3.300 12 SLOW
b IN L16 14 LVCMOS33* 3.300
C OUT K16 15 LVCMOS33* 3.300 12 SLOW
c IN M13 14 LVCMOS33* 3.300
D OUT K13 15 LVCMOS33* 3.300 12 SLOW
d IN R15 14 LVCMOS33* 3.300
DP OUT H15 15 LVCMOS33* 3.300 12 SLOW
E OUT P15 14 LVCMOS33* 3.300 12 SLOW
F OUT T11 14 LVCMOS33* 3.300 12 SLOW
G OUT L18 14 LVCMOS33* 3.300 12 SLOW
s1 OUT J17 15 LVCMOS33* 3.300 12 SLOW
s2 OUT J18 15 LVCMOS33* 3.300 12 SLOW
s3 OUT T9 14 LVCMOS33* 3.300 12 SLOW
s4 OUT J14 15 LVCMOS33* 3.300 12 SLOW
s5 OUT P14 14 LVCMOS33* 3.300 12 SLOW
19°C Cloudy
10:58 PM
2/29/2024


lab4_b - [D:/lab4_b/lab4_b.xpr] - Vivado 2018.2
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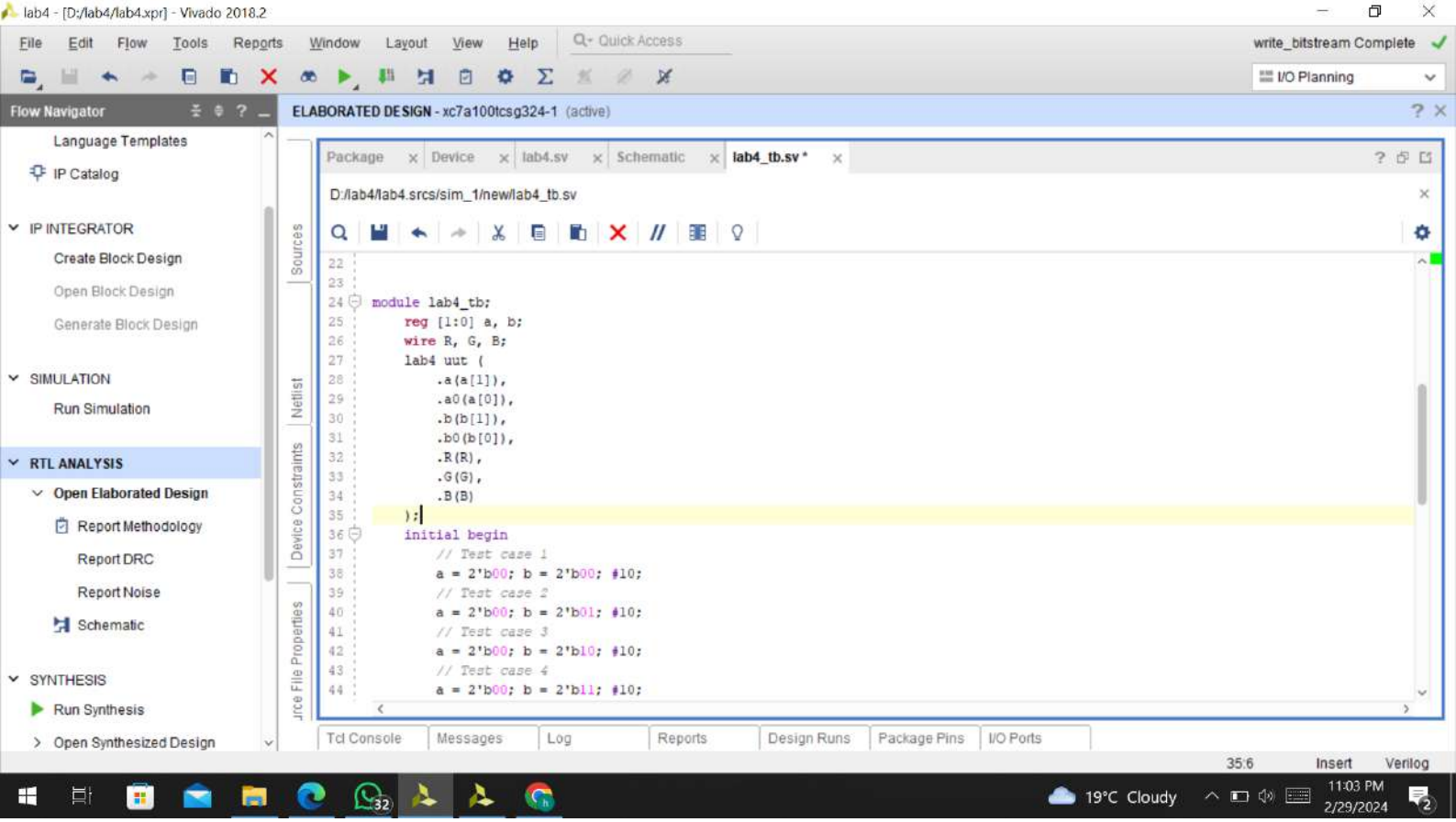
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a100tcsg324-1 (active)
Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports
Name Direction Neg Diff Pair Package Pin Fixed Bank I/O Std Vcco Vref Drive Strength Slew Type
C OUT K16 15 LVCMOS33* 3.300 12 SLOW
c IN M13 14 LVCMOS33* 3.300
D OUT K13 15 LVCMOS33* 3.300 12 SLOW
d IN R15 14 LVCMOS33* 3.300
DP OUT H15 15 LVCMOS33* 3.300 12 SLOW
E OUT P15 14 LVCMOS33* 3.300 12 SLOW
F OUT T11 14 LVCMOS33* 3.300 12 SLOW
G OUT L18 14 LVCMOS33* 3.300 12 SLOW
s1 OUT J17 15 LVCMOS33* 3.300 12 SLOW
s2 OUT J18 15 LVCMOS33* 3.300 12 SLOW
s3 OUT T9 14 LVCMOS33* 3.300 12 SLOW
s4 OUT J14 15 LVCMOS33* 3.300 12 SLOW
s5 OUT P14 14 LVCMOS33* 3.300 12 SLOW
s6 OUT T14 14 LVCMOS33* 3.300 12 SLOW
s7 OUT K2 35 LVCMOS33* 3.300 12 SLOW
s8 OUT U13 14 LVCMOS33* 3.300 12 SLOW
x IN T18 14 LVCMOS33* 3.300
y IN U18 14 LVCMOS33* 3.300
z IN R13 14 LVCMOS33* 3.300
19°C Cloudy
10:59 PM
2/29/2024


lab4 - [D:/lab4/lab4.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
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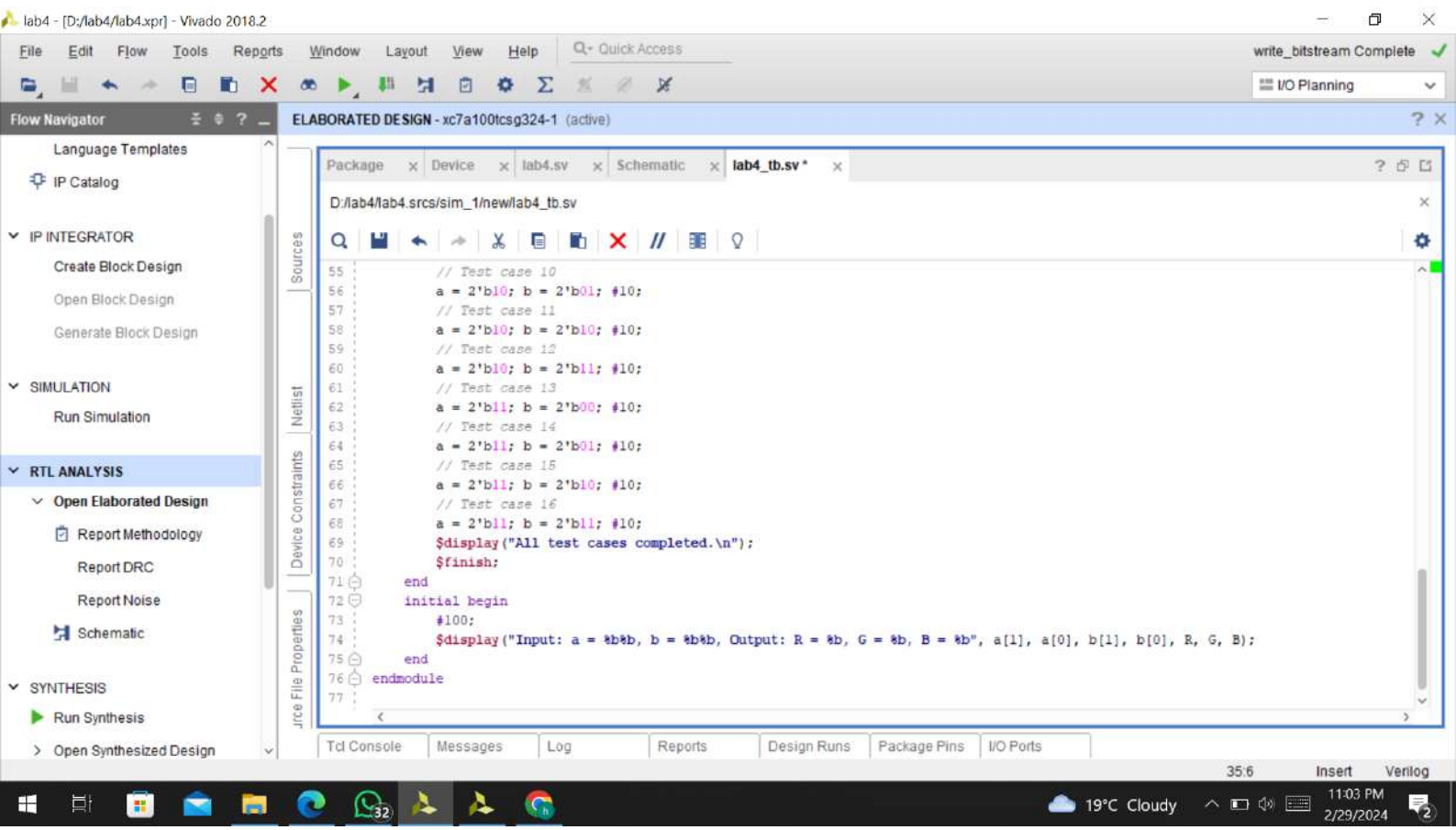
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
ELABORATED DESIGN - xc7a100tcsg324-1 (active)
Package
Device
lab4.sv
Schematic
lab4_tb.sv *
D:/lab4/lab4.srcs/sim_1/new/lab4_tb.sv
Sources
Netlist
Device Constraints
Source File Properties
22
23
24 module lab4_tb;
25 reg [1:0] a, b;
26 wire R, G, B;
27 lab4 uut (
28 .a(a[1]),
29 .a0(a[0]),
30 .b(b[1]),
31 .b0(b[0]),
32 .R(R),
33 .G(G),
34 .B(B)
35);
36 initial begin
37 // Test case 1
38 a = 2'b00; b = 2'b00; #10;
39 // Test case 2
40 a = 2'b00; b = 2'b01; #10;
41 // Test case 3
42 a = 2'b00; b = 2'b10; #10;
43 // Test case 4
44 a = 2'b00; b = 2'b11; #10;
Tcl Console
Messages
Log
Reports
Design Runs
Package Pins
I/O Ports
35:6
Insert
Verilog
19°C Cloudy
11:03 PM
2/29/2024


lab4 - [D:/lab4/lab4.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
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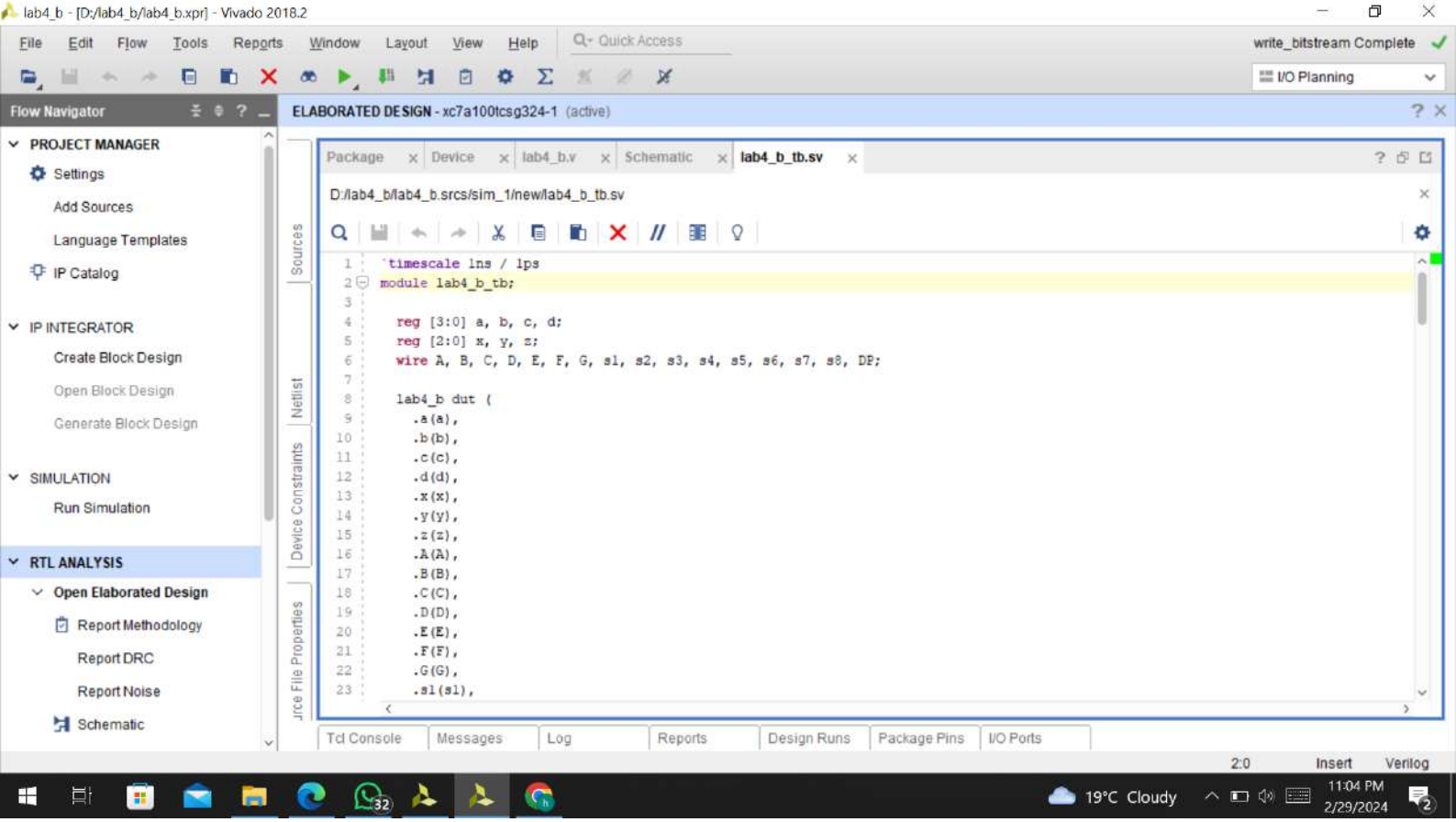
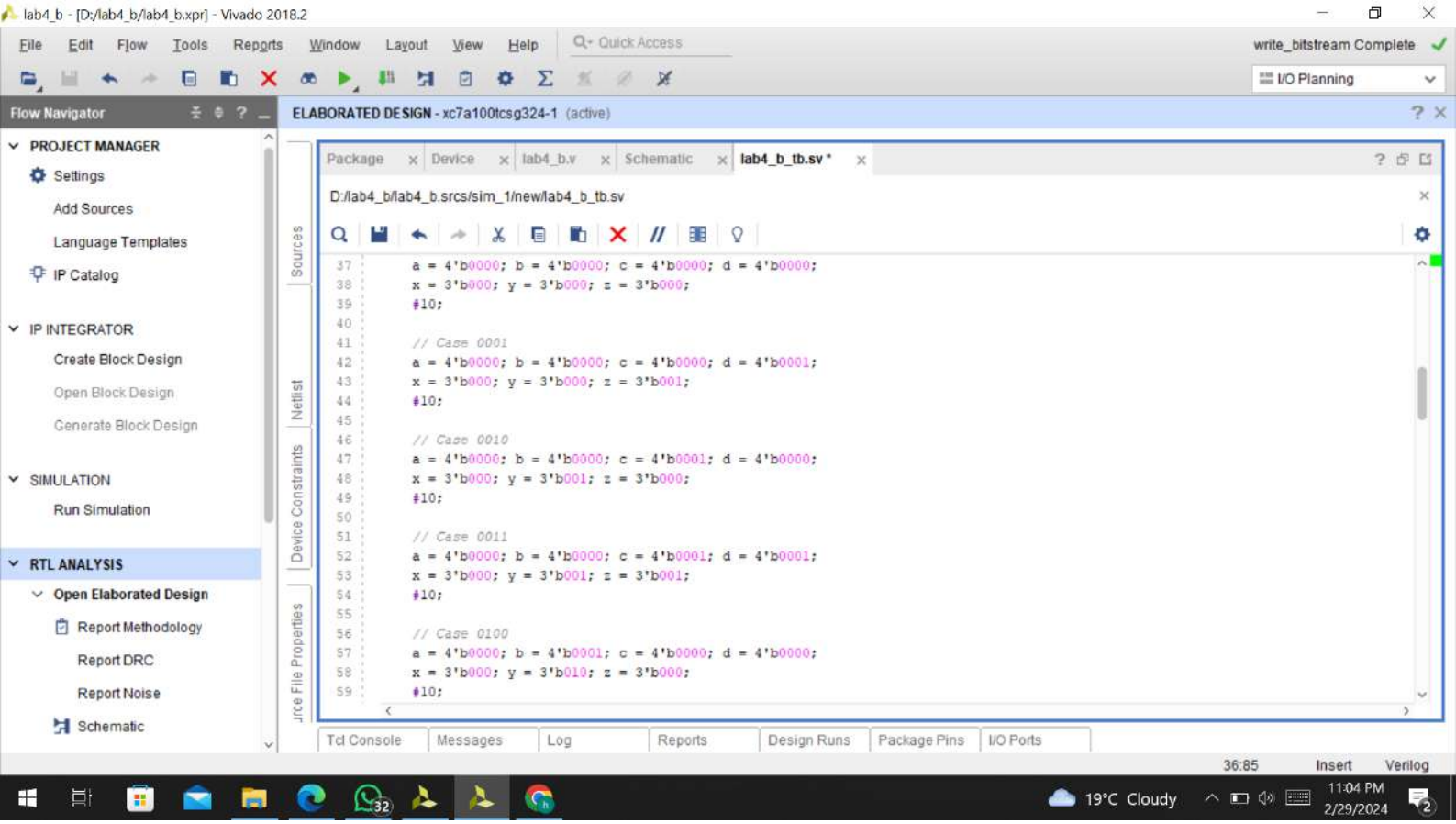
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
ELABORATED DESIGN - xc7a100tcsg324-1 (active)
Package
Device
lab4.sv
Schematic
lab4_tb.sv *
D:/lab4/lab4.srcs/sim_1/new/lab4_tb.sv
Sources
Netlist
Device Constraints
Source File Properties
55 // Test case 10
56 a = 2'b10; b = 2'b01; #10;
57 // Test case 11
58 a = 2'b10; b = 2'b10; #10;
59 // Test case 12
60 a = 2'b10; b = 2'b11; #10;
61 // Test case 13
62 a = 2'b11; b = 2'b00; #10;
63 // Test case 14
64 a = 2'b11; b = 2'b01; #10;
65 // Test case 15
66 a = 2'b11; b = 2'b10; #10;
67 // Test case 16
68 a = 2'b11; b = 2'b11; #10;
69 $display("All test cases completed.\n");
70 $finish;
71 end
72 initial begin
73 #100;
74 $display("Input: a = %b%b, b = %b%b, Output: R = %b, G = %b, B = %b", a[1], a[0], b[1], b[0], R, G, B);
75 end
76 endmodule
77
Tcl Console
Messages
Log
Reports
Design Runs
Package Pins
I/O Ports
35:6
Insert
Verilog
19°C Cloudy
11:03 PM
2/29/2024




```
1  `timescale 1ns / 1ps
2  module lab4_b_tb;
3
4    reg [3:0] a, b, c, d;
5    reg [2:0] x, y, z;
6    wire A, B, C, D, E, F, G, s1, s2, s3, s4, s5, s6, s7, s8, DP;
7
8    lab4_b dut (
9      .a(a),
10     .b(b),
11     .c(c),
12     .d(d),
13     .x(x),
14     .y(y),
15     .z(z),
16     .A(A),
17     .B(B),
18     .C(C),
19     .D(D),
20     .E(E),
21     .F(F),
22     .G(G),
23     .s1(s1),
```


lab4_b - [D:/lab4_b/lab4_b.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
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I/O Planning
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IP INTEGRATOR
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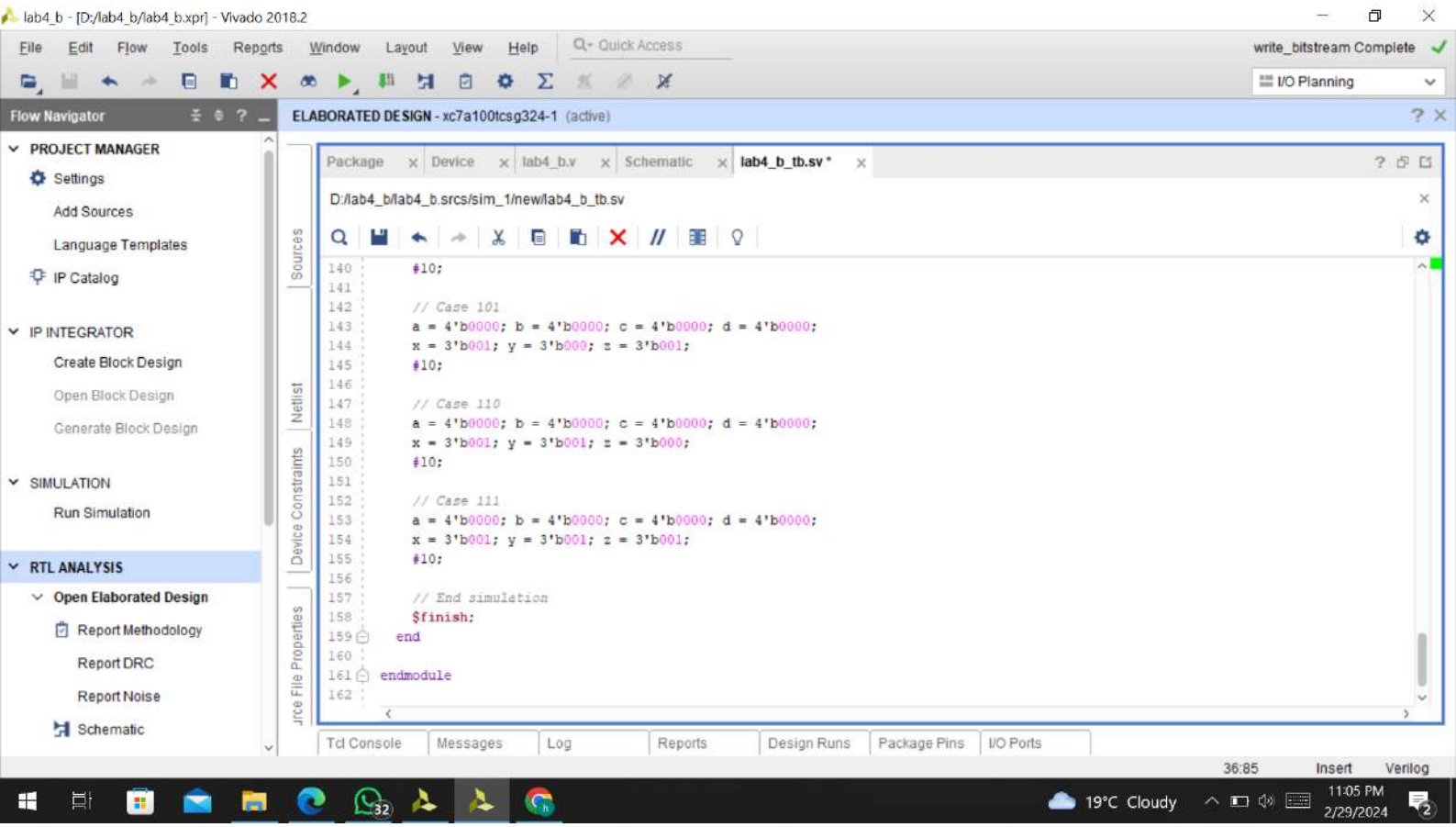
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a100tcsg324-1 (active)
Package
Device
lab4_b.v
Schematic
lab4_b_tb.sv *
D:/lab4_b/lab4_b.srcs/sim_1/new/lab4_b_tb.sv
Sources
Netlist
Device Constraints
Source File Properties
a = 4'b0000; b = 4'b0000; c = 4'b0000; d = 4'b0000;
x = 3'b000; y = 3'b000; z = 3'b000;
#10;
// Case 0001
a = 4'b0000; b = 4'b0000; c = 4'b0000; d = 4'b0001;
x = 3'b000; y = 3'b000; z = 3'b001;
#10;
// Case 0010
a = 4'b0000; b = 4'b0000; c = 4'b0001; d = 4'b0000;
x = 3'b000; y = 3'b001; z = 3'b000;
#10;
// Case 0011
a = 4'b0000; b = 4'b0000; c = 4'b0001; d = 4'b0001;
x = 3'b000; y = 3'b001; z = 3'b001;
#10;
// Case 0100
a = 4'b0000; b = 4'b0001; c = 4'b0000; d = 4'b0000;
x = 3'b000; y = 3'b010; z = 3'b000;
#10;
Tcl Console
Messages
Log
Reports
Design Runs
Package Pins
I/O Ports
36:85
Insert
Verilog
19°C Cloudy
11:04 PM
2/29/2024


lab4_b - [D:/lab4_b/lab4_b.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
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I/O Planning
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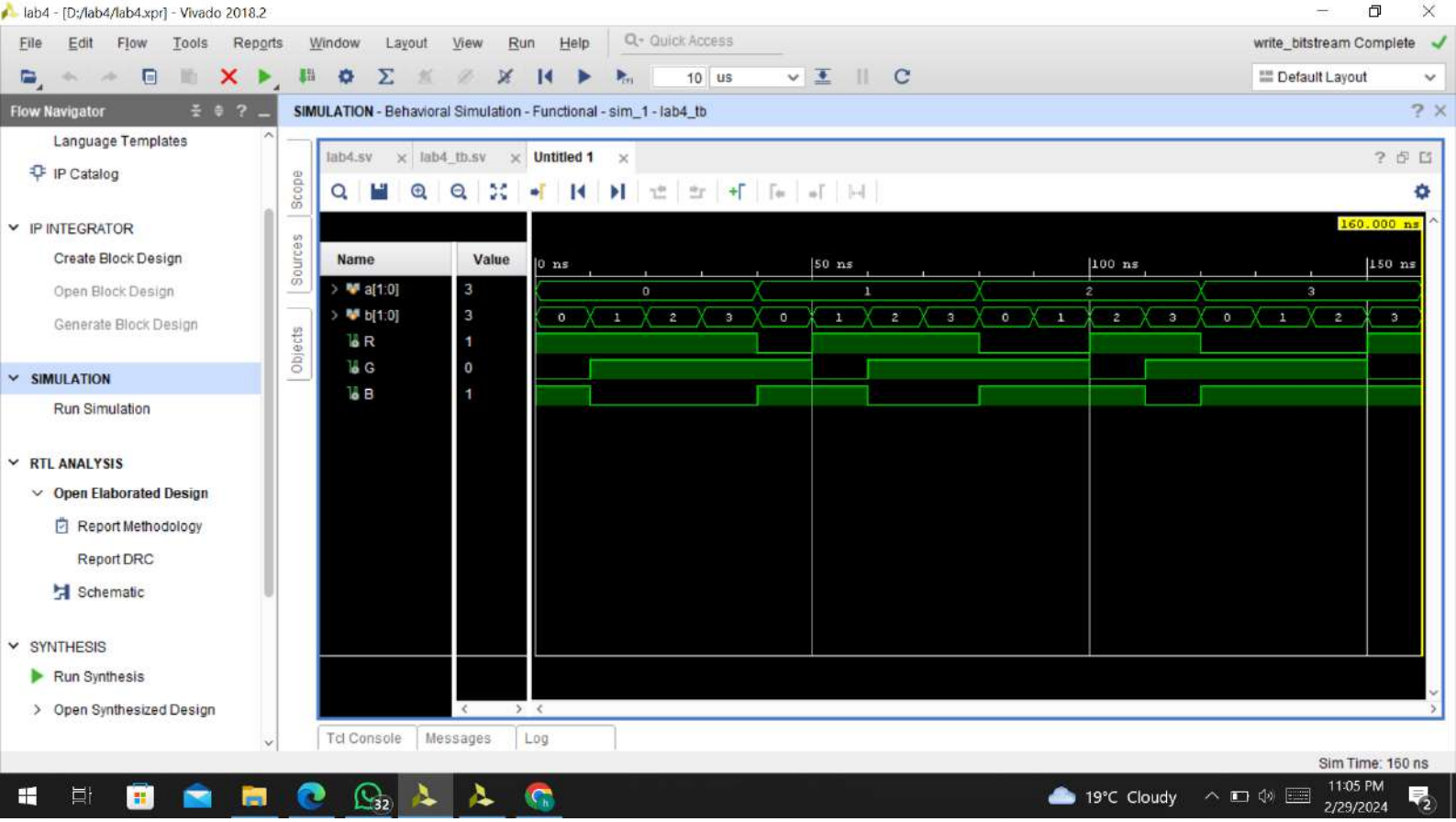
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a100tcsg324-1 (active)
Package
Device
lab4_b.v
Schematic
lab4_b_tb.sv *
D:/lab4_b/lab4_b.srcs/sim_1/new/lab4_b_tb.sv
#10;
// Case 101
a = 4'b0000; b = 4'b0000; c = 4'b0000; d = 4'b0000;
x = 3'b001; y = 3'b000; z = 3'b001;
#10;
// Case 110
a = 4'b0000; b = 4'b0000; c = 4'b0000; d = 4'b0000;
x = 3'b001; y = 3'b001; z = 3'b000;
#10;
// Case 111
a = 4'b0000; b = 4'b0000; c = 4'b0000; d = 4'b0000;
x = 3'b001; y = 3'b001; z = 3'b001;
#10;
// End simulation
$finish;
end
endmodule
Sources
Netlist
Device Constraints
Tcl Console
Messages
Log
Reports
Design Runs
Package Pins
I/O Ports
36:85
Insert
Verilog
19°C Cloudy
11:05 PM
2/29/2024


lab4 - [D:/lab4/lab4.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Run Help
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SIMULATION - Behavioral Simulation - Functional - sim_1 - lab4_tb
Language Templates
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IP INTEGRATOR
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Open Block Design
Generate Block Design
SIMULATION
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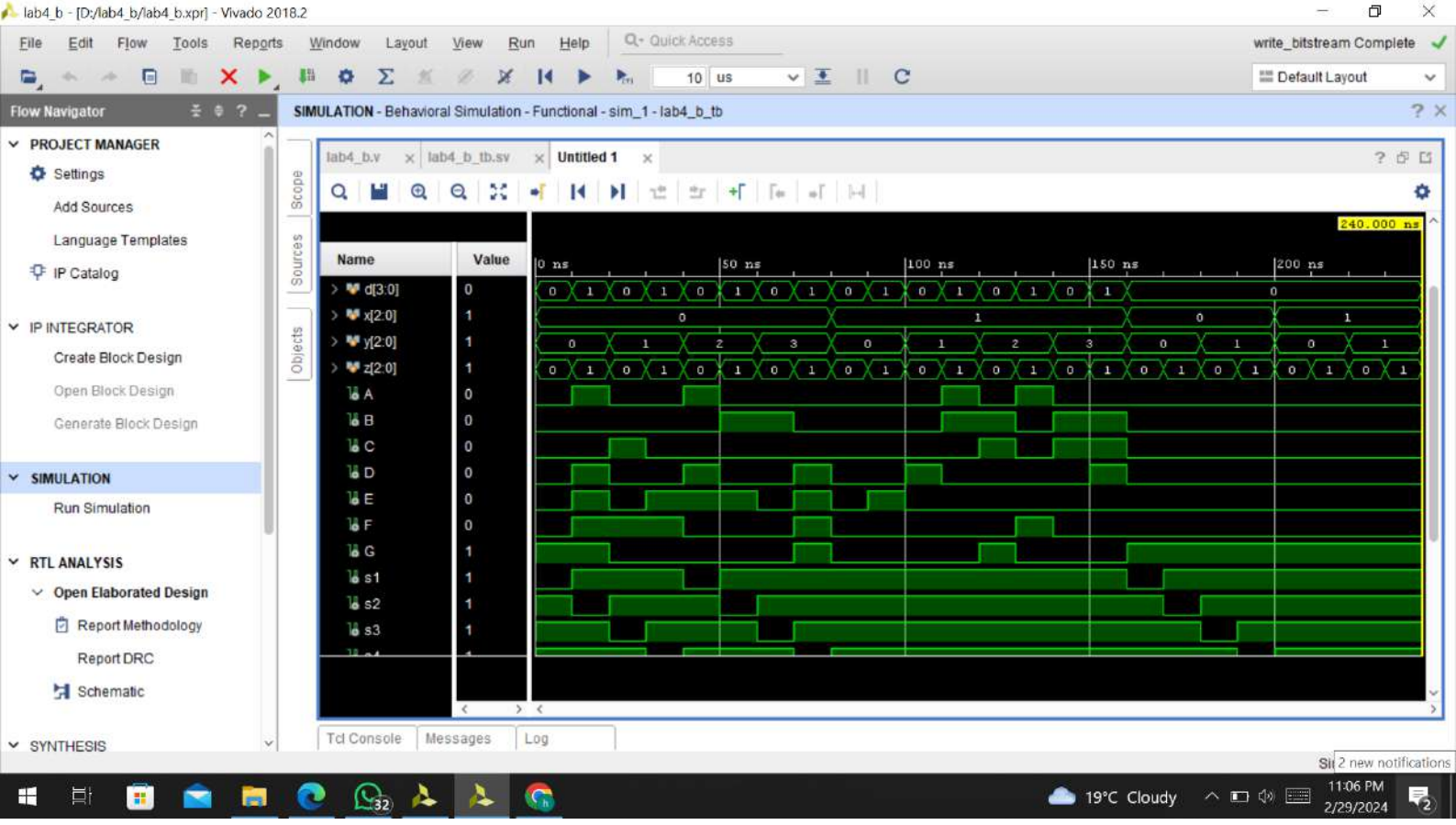
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
lab4.sv
lab4_tb.sv
Untitled 1
Scope
Sources
Objects
Name
Value
a[1:0]
b[1:0]
R
G
B
160.000 ns
0 ns
50 ns
100 ns
150 ns
Tcl Console
Messages
Log
Sim Time: 160 ns
19°C Cloudy
11:05 PM
2/29/2024


lab4_b - [D:/lab4_b/lab4_b.xpr] - Vivado 2018.2
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Schematic
SYNTHESIS
SIMULATION - Behavioral Simulation - Functional - sim_1 - lab4_b_tb
lab4_b.v
lab4_b_tb.sv
Untitled 1
Scope
Sources
Objects
Name
Value
d[3:0]
x[2:0]
y[2:0]
z[2:0]
A
B
C
D
E
F
G
s1
s2
s3
240.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
Tcl Console
Messages
Log
2 new notifications
19°C Cloudy
11:06 PM
2/29/2024