

Name:

EE-272L Digital Systems Design

Reg. No.:

Marks Obtained: _____

Lab Manual

DSD Lab Manual Evaluation Rubrics
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Assessment	Total Marks	Marks Obtained	0-30%	30-60%	70-100%
Code Organization	3		No Proper Indentation and descriptive naming, no code organization. Zero to Some understanding but not working	Proper Indentation or descriptive naming or code organization. Mild to Complete understanding but not working	Proper Indentation and descriptive naming, code organization. Complete understanding, and proper working
Simulation	5		Simulation not done or incorrect, without any understanding of waveforms	Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms	Working simulation without any errors, etc and complete understanding of waveforms
FPGA	2		Not implemented on FPGA and questions related to synthesis and implementation not answered.	Correctly Implemented on FPGA or questions related to synthesis and implementation answered.	Correctly Implemented on FPGA and questions related to synthesis and implementation answered.

Combinational Circuit Design using K-Maps

Task:

You are required to build a circuit to display different characters (0 to F) on one of the eight seven-segment displays.

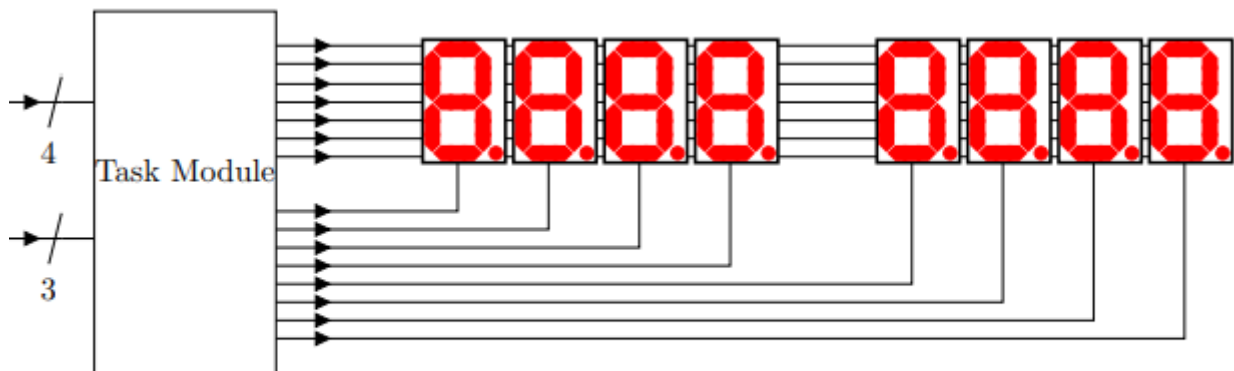


Fig. 4.3: Lab Task Modular Diagram.

Deliverables

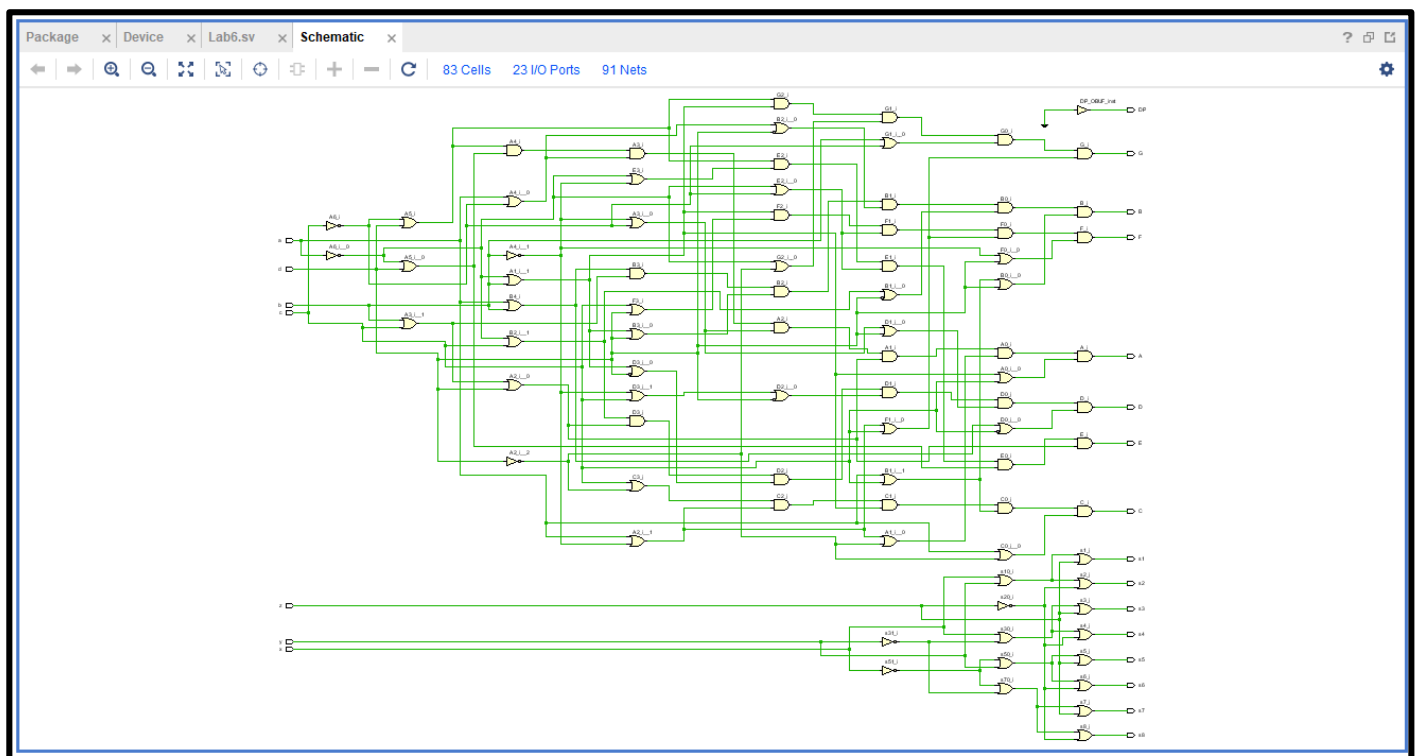
- Truth table (Cathodes):

	a	B	c	d	A	B	C	D	E	F	G
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	0	1	0	0
A	1	0	1	0	0	0	0	1	0	0	0
B	1	0	1	1	1	1	0	0	0	0	0
C	1	1	0	0	0	1	1	0	0	0	1
D	1	1	0	1	1	0	0	0	0	1	0
E	1	1	1	0	0	1	1	0	0	0	0
F	1	1	1	1	0	1	1	1	0	0	0

- Truth table (Anodes):

	x	y	z	s1	s2	s3	s4	s5	s6	s7	s8
0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
2	0	1	0	1	1	0	1	1	1	1	1
3	0	1	1	1	1	1	0	1	1	1	1
4	1	0	0	1	1	1	1	0	1	1	1
5	1	0	1	1	1	1	1	1	0	1	1
6	1	1	0	1	1	1	1	1	1	0	1
7	1	1	1	1	1	1	1	1	1	1	0

- Circuit diagram inferred by the Xilinx Vivado:



- Maximum combinational delay in Synthesis:

SYNTHESIZED DESIGN - xc7a100tcs9324-1 (active)													
Unconstrained Paths - NONE - NONE - Setup													
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 1	∞	3	2	8	y	s3	6.827	5.222	1.606	∞	input port clock		
Path 2	∞	3	2	8	y	s8	6.806	5.201	1.606	∞	input port clock		
Path 3	∞	3	2	8	y	s4	6.803	5.197	1.606	∞	input port clock		
Path 4	∞	3	2	7	c	F	6.800	5.194	1.606	∞	input port clock		
Path 5	∞	3	2	7	c	B	6.796	5.191	1.606	∞	input port clock		
Path 6	∞	3	2	7	c	A	6.792	5.186	1.606	∞	input port clock		
Path 7	∞	3	2	7	c	D	6.791	5.185	1.606	∞	input port clock		
Path 8	∞	3	2	8	y	s6	6.779	5.173	1.606	∞	input port clock		
Path 9	∞	3	2	8	y	s5	6.777	5.171	1.606	∞	input port clock		
Path 10	∞	3	2	8	x	s7	6.766	5.160	1.606	∞	input port clock		

- Maximum combinational delay in Implementation:

IMPLEMENTED DESIGN - xc7a100tcs9324-1 (active)

Tcl Console Messages Log Reports Design Runs DRC Power Timing x

Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 1	∞	3	2	8	z	s7	12.309	5.369	6.940	∞	input port clock		
Path 2	∞	3	2	8	z	s4	9.974	5.404	4.570	∞	input port clock		
Path 3	∞	3	2	7	a	A	9.969	5.407	4.562	∞	input port clock		
Path 4	∞	3	2	7	a	B	9.901	5.157	4.744	∞	input port clock		
Path 5	∞	3	2	8	z	s3	9.760	5.192	4.568	∞	input port clock		
Path 6	∞	3	2	7	b	F	9.658	5.400	4.257	∞	input port clock		
Path 7	∞	3	2	8	z	s8	9.624	5.368	4.256	∞	input port clock		
Path 8	∞	3	2	7	a	D	9.623	5.382	4.241	∞	input port clock		
Path 9	∞	3	2	8	z	s1	9.572	5.390	4.182	∞	input port clock		
Path 10	∞	3	2	8	z	s6	9.334	5.170	4.164	∞	input port clock		

General Information
Timer Settings
Design Timing Summary
Check Timing (0)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
NONE to NONE
Setup (10)
Hold (10)

- Resource Utilization Summary:

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	8	0	63400	0.01
LUT as Logic	8	0	63400	0.01
LUT as Memory	0	0	19000	0.00
Slice Registers	0	0	126800	0.00
Register as Flip Flop	0	0	126800	0.00
Register as Latch	0	0	126800	0.00
F7 Muxes	0	0	31700	0.00
F8 Muxes	0	0	15850	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	23	0	210	10.95
Bonded IPADs	0	0	2	0.00
PHY_CONTROL	0	0	6	0.00
PHASER_REF	0	0	6	0.00
OUT_FIFO	0	0	24	0.00
IN_FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	24	0.00
PHASER_IN/PHASER_IN_PHY	0	0	24	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

- System Verilog code:

```
D:\Notepad++\Projects\Lab6.sv - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
Lab.sv Lab_tb.sv Lab6.sv Lab6_tb.sv
1 module Lab6(a,b,c,d,x,y,z,DP,A,B,C,D,E,F,G,s1,s2,s3,s4,s5,s6,s7,s8);
2 input logic a,b,c,d,x,y,z;
3 output logic A,B,C,D,E,F,G,s1,s2,s3,s4,s5,s6,s7,s8,DP;
4 assign DP = 0;
5 assign A = (~c|d) & (~a|d) & (a|~c) & (~b|~c) & (c|d) & (a|~b|~d) & (~a|b|c);
6 assign B = (a|b) & (b|c) & (~a|b|d) & (a|~c|~d) & (~a|c|~d) & (a|c|d);
7 assign C = (c|~d) & (a|~b) & (~a|b) & (a|c) & (a|~d);
8 assign D = (~a|c) & (b|c|d) & (~a|b|~d) & (~b|c|~d) & (~b|~c|d) & (a|b|~c);
9 assign E = (~c|d) & (~a|~b) & (~a|~c) & (~a|d) & (b|c|d);
10 assign F = (~a|b) & (c|d) & (~a|~c) & (a|~b|c) & (~b|d);
11 assign G = (~c|d) & (~a|b) & (~a|~d) & (b|~c) & (a|~b|c);
12 assign s1 = (x|y|z);
13 assign s2 = (x|y|~z);
14 assign s3 = (x|~y|z);
15 assign s4 = (x|~y|~z);
16 assign s5 = (~x|y|z);
17 assign s6 = (~x|y|~z);
18 assign s7 = (~x|~y|z);
19 assign s8 = (~x|~y|~z);
20 endmodule
```