Analysis of Sequential Circuits

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Lecture Review

- Analysis of Clocked Sequential Circuits with D Flip Flops
 - State Equation?
 - State Table?
 - Alternative State Table?
 - State Diagram?

- Analysis of Clocked Sequential Circuits
 - Circuit with T or JK flop flops

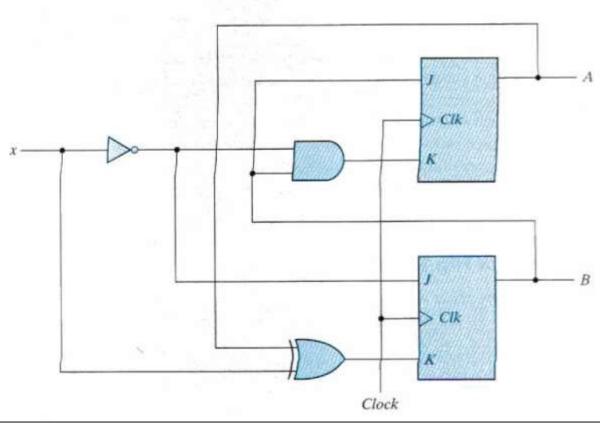
JK and T Flip Flop Analysis

- The next-state values of a sequential circuit that uses flip flops such as JK or T type can be derived using the following procedure:
 - Determine the flip flop input equations in terms of the present state and input variables
 - List the binary values of each input equation
 - Use the corresponding flip flop characteristic table to determine the next state values in the state table

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JK Analysis Example



- $J_A = \overline{B}$
- $K_A = Bx$
- $J_B = x'$
- $K_B = A'x + Ax' = A \oplus x$

JK Analysis State Table

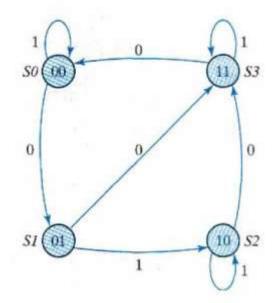
- $J_A = B$
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JK Flip Flop								
J	K	Q(t+1)						
0	0	Q(t)	No change					
0	1	0	Reset					
1	0	1	Set					
1	1	Q'(t)	Complement					

	esent tate	Input		ext ate	Output				
A	В	x	Α	В		J_A	K_{A}	J_{B}	$K_{\mathbf{B}}$
0	0	0	0	1		0	0	1	0
0	0	1	0	0		0	0	0	1
0	1	0	1	1		1	1	1	0
0	1	1	1	0		1	0	0	1
1	0	0	1	1		0	0	1	1
1	0	1	1	0		0	0	0	0
1	1	0	0	0		1	1	1	1
1	1	1	1	1		1	0	0	0

JK Analysis State Diagram

	esent tate	Input		ext ate	Output			
Α	В	x	Α	В	J_A	K_A	J_B	K _B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

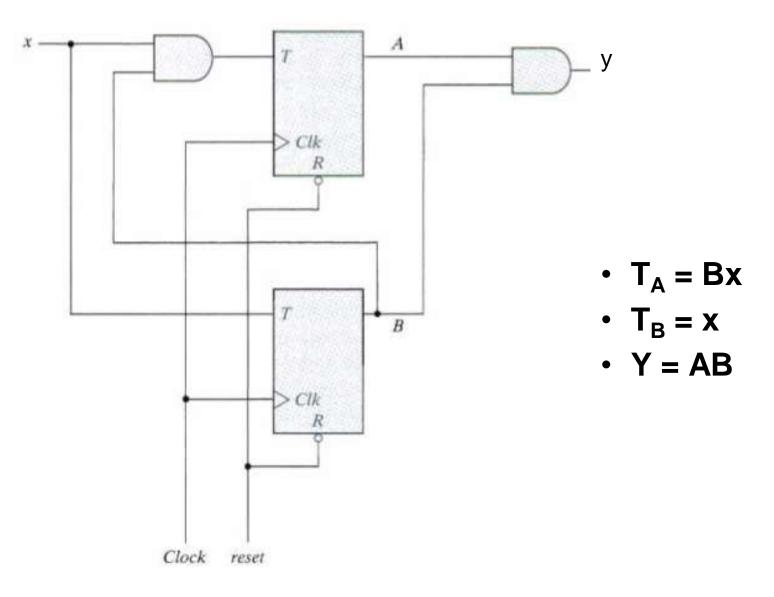


T Flip Flop Analysis

- Analysis of a sequential circuit with T flip flops follows the same procedure outlined for JK flip flops.
- The next state values in the state table can be obtained wither by using the characteristic table or the characteristic equation

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-Q(t+1) = T \oplus Q = T'Q + TQ'
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T Flip Flop Analysis Example



T Flip Flop Analysis State Table

•
$$T_A = Bx$$

• $T_B = x$

T Flip Flop								
T	Q(t+1)							
0	Q(t)	No change						
1	Q'(t)	Complement						

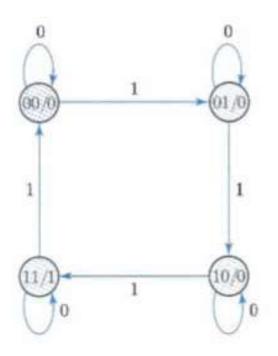
•
$$A(t + 1) = T_A \oplus A = Bx \oplus A$$

•
$$B(t + 1) = T_B \oplus B = x \oplus B$$

	esent tate	Input	Next State		Output
A	В	x	Α	В	у
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

T Flip Flop Analysis State Diagram

Present State		Input	N ext State		Output
Α	В	x	Α	В	уу
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1



End of Lecture