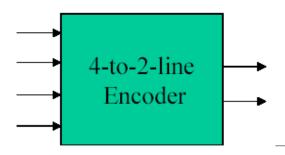
Encoder, Priority Encoder

By Engr. Rimsha

Encoders

- An encoder is a digital circuit that performs the inverse operation of a decoder.
- An encoder has 2ⁿ (or fewer) input lines and n output lines.
- The output lines generate the binary code corresponding to the input value



Truth Table: Octal to Binary Encoder

Inputs						Outputs				
D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	O	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$z=D_1+D_3+D_5+D_7$$

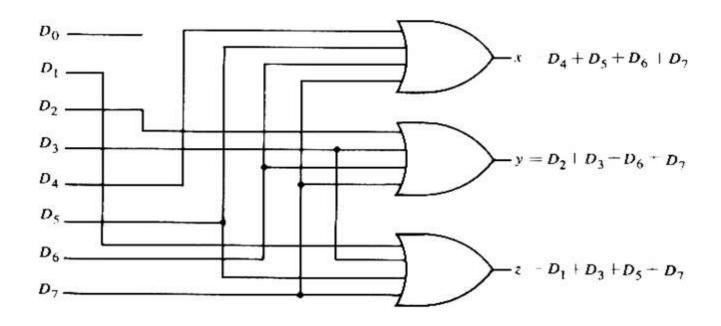
$$z=D_1+D_3+D_5+D_7$$
 $y=D_2+D_3+D_6+D_7$ $x=D_4+D_5+D_6+D_7$

$$x=D_4+D_5+D_6+D_7$$

Encoder: Example

- An example of encoder is octal-to-binary encoder
- It has eight inputs (one for each octal digits) and three outputs that generate the corresponding binary number
- It is assumed that only one input has a value of 1 at any given time
- The encoder can be implemented with OR gates whose inputs are determined directly from the truth table
- Output z is equal to 1 when the input octal digit is 1,3,5 or 7. Output y is 1 for octal digits 2,3,6 or 7 and output x is 1 for digits 4,5,6 or 7. These conditions can be expressed as by the Boolean functions as shown in the previous slide

Octal to Binary Encoder Implementation



$$z=D_1+D_3+D_5+D_7$$

$$z=D_1+D_3+D_5+D_7$$
 $y=D_2+D_3+D_6+D_7$ $x=D_4+D_5+D_6+D_7$

$$x=D_4+D_5+D_6+D_7$$

Priority Encoder

- A priority encoder is an encoder circuit that includes the priority function.
- The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence
 - D₃ has the highest priority
 - D₀ has the lowest priority
- Valid bit indicator (V) is set to 1 when one or more inputs are equal to 1. If all inputs are 0, there is no valid inputs and V is equal to 0. The other two outputs are not inspected when V equals 0 and are specified as don't care conditions

Priority Encoder: Expanded Truth Table

D_{θ}	D_I	D_2	D_3	х	у	V
0	0	0	0	X	X	0
0	0	0	1	1	1	1
0	0	1	0	1	0	1
0	0	1	1	1	1	1
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	1	0	1
0	1	1	1	1	1	1
1	0	0	0	0	0	1
1	0	0	1	1	1	1
1	0	1	0	1	0	1
1	0	1	1	1	1	1
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	0	1
1	1	1	1	1	1	1

Truth Table of a Priority Encoder

Inputs				Outputs			
D_0	D_1	D_{7}	D_3	X	У	v	
0	0	0	0	X	X	0	
I	0	0	0	0	0	1	
\boldsymbol{X}	1	0	0	0	1	1	
X	\boldsymbol{X}	1	0	1	0	1	
X	X	X	1	1	I	1	

Priority Encoder: Truth Table

	Inp	out		Output			
D ₀ _	D,	D_2	D ₃	,	X	у	V
0	0	0	0)	X	X	0
I	0	0	0	(0	0	I
X	I	0	0	()	I	I
X	X	I	0	I		0	
X	X	X	I	l l		1	I

-X: don't-care conditions in the output, used in the inputs to condense truth table, replaced by both 0 and then I

–V: valid output indication, implemented by OR function

Maps for Priority Encoder

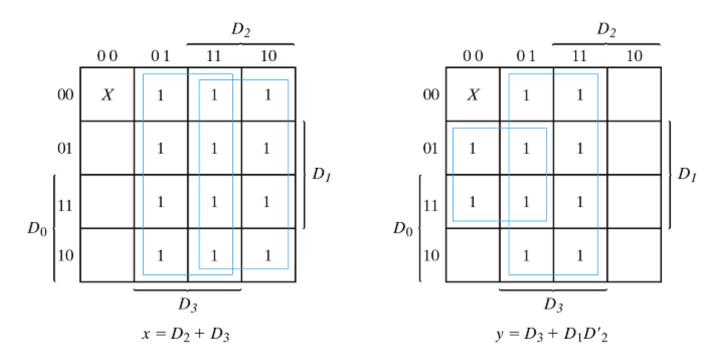
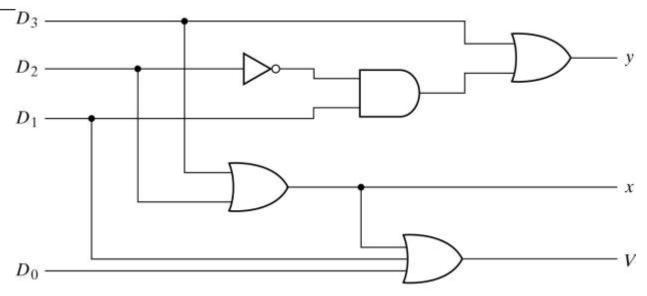


Fig. 4-22 Maps for a Priority Encoder

Priority Encoder: Logic circuit

Truth Table of a Priority Encoder

Inputs				O	Outputs		
D_0	D_1	D_2	D_3	X	У	v	
0	0	0	0	X	X	0	
I	0	0	0	0	0	1	
\boldsymbol{X}	1	0	0	0	1	1	
X	X	1	0	1	0	1	
X	X	X	1	1	1	1	



Practice Problem

 Design a Priority Encoder with Priority to Lower Subscript

End of Lecture