Computer Architecture and Logic Design

Magnitude Comparator, Decoder Circuit, Types, Its Application

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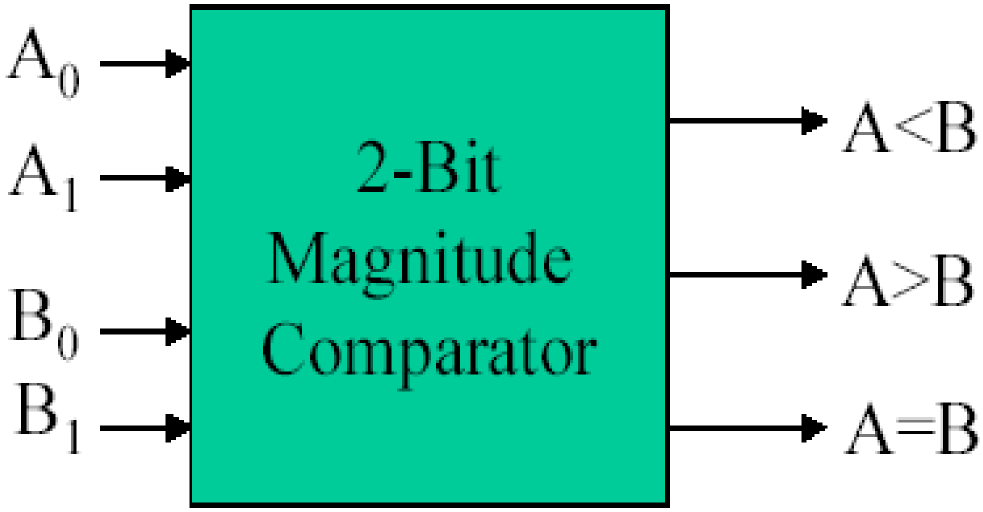
Magnitude Comparator

- The comparison of two numbers is an operation that determines if one number is greater than, less than or equal to the other number

- A magnitude comparator is a combinational circuit that compares two numbers, A and B and determines their relative magnitudes

- The outcome of the comparison is specified by three binary variables that indicates whether A>B, A=B or A<B



Magnitude Comparator

- If we follow the traditional design approach of truth table then comparing two n-bit numbers will have 2^{2n} entries in the truth table and becomes too complicated for large values of n.
- However, a comparator circuit possess a certain amount of regularity. Digital functions that possess an inherent well defined regularity can usually be designed by means of algorithmic procedure. This reduce design efforts and reduce human errors
- An algorithm is a procedure that specifies a finite set of steps, if followed, give the solution to a problem. The algorithm is direct application of the procedure a person uses to compare the relative magnitude of two numbers

Developing Algorithm

- Consider the two numbers A and B, with four digits each, the coefficients of numbers with descending significance can be written as:
  - $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$
- The two numbers are equal if all pairs of significant digits are equal:
  - A=B if $A_3=B_3$, $A_2=B_2$, $A_1=B_1$and $A_0=B_0$
- For binary (either 1 or 0) digits the equality relation of each pair of bits can be expressed logically with exclusive-NOR function to test if $A_i = B_i$ as
  - $x_i = (A_i \oplus B_i)' = (A_iB_i'+A_i'B_i)' = A_iB_i+A_i'B_i'$ for $i = 0,1,2,3$
  - $x_i = 1$ only if the pair of bits in position i are equal otherwise $x_i = 0$
- Therefore we can can check if A = B by
  - $(A=B) = x_3x_2x_1x_0$
- The symbol (A=B) is binary output variable that is equal to 1 only if all pair of digits of the two numbers are equal

Developing Algorithm

- To determine if A>B or A<B, we inspect the relative magnitudes of pairs of significant digits starting from the most significant position. If the two digits are equal, we compare the next lower significant pair of digits. This comparison continues until a pair of unequal digits is reached

- If the corresponding digit of A is 1 and that of B is 0, we conclude that A>B. If the corresponding digit of A is 0 and that of B is 1, we conclude that A<B

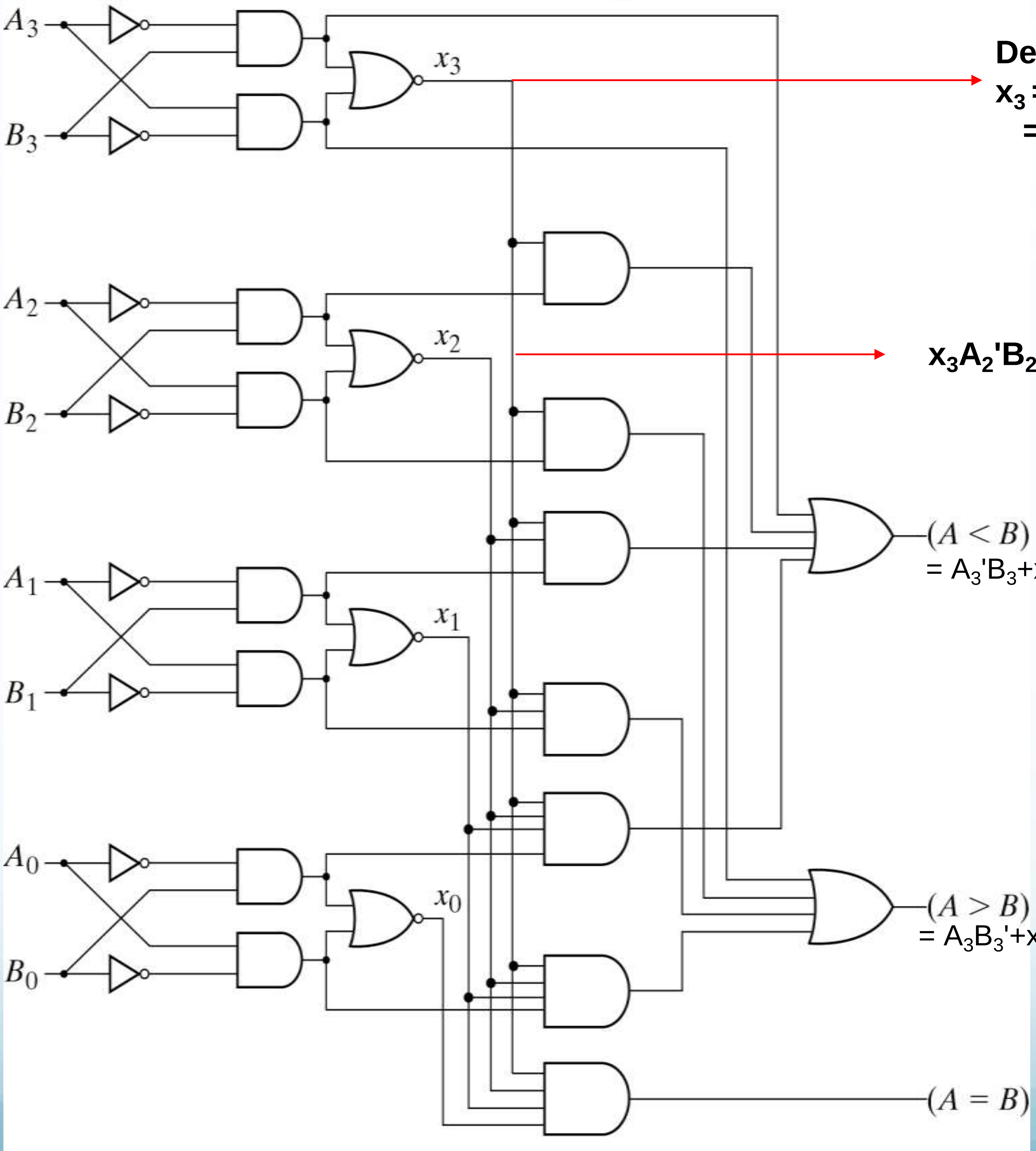
- The sequential comparison can be expressed logically by the two Boolean functions
  - $(A>B) = A_3B_3'+x_3A_2B_2'+x_3x_2A_1B_1'+x_3x_2x_1 A_0B_0'$
  - $(A<B) = A_3'B_3+x_3A_2'B_2+x_3x_2A_1'B_1+x_3x_2x_1 A_0'B_0$

- The symbols (A>B) and (A<B) are binary output variables that are equal to 1when A>B or A<B respectively

Developing Algorithm

- The gate implementation for a magnitude comparator involves a certain amount of repetition so it is simpler than it seems.
- The unequal outputs can use the same gates that are needed to generate the equal output
- The logic diagram of the 4-bit magnitude comparator is shown in fig 4 – 17
- The four x outputs are generated with exclusive-NOR circuits and applied to an AND gate to give the output binary variable (A=B)
- The other two outputs use the x variable to generate the Boolean functions
- The procedure for obtaining magnitude comparator circuits for binary numbers with more than four bits is obvious from the above steps

4-Bit Magnitude Comparator Logic Diagram



Decides if A3=B3

$$x_3 = (A_3B_3'+A_3'B_3)'$$

$$=(A_3 \oplus B_3)'$$

$x_3A_2'B_2$

$= A_3'B_3+x_3A_2'B_2+x_3x_2A_1'B_1+x_3x_2x_1\ A_0'B_0$

$= A_3B_3'+x_3A_2B_2'+x_3x_2A_1B_1'+x_3x_2x_1\ A_0B_0'$

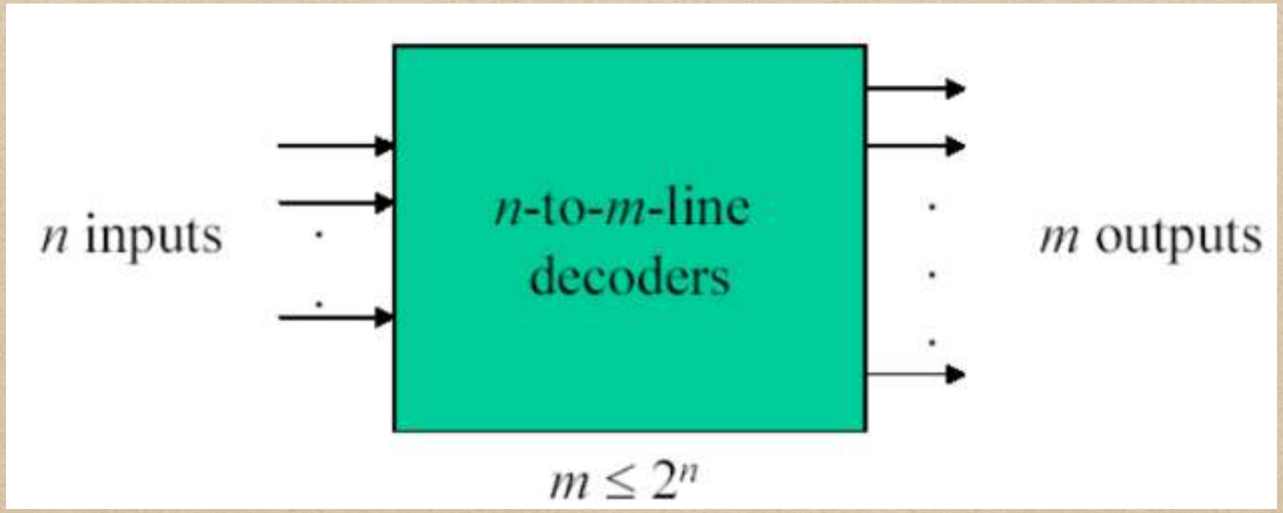
Fig. 4-17 4-Bit Magnitude Comparator

Decoder

- What is the function of a decoder?
  - It selects or de-select one of the devices

Decoder

- A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output output lines. Only one output can be active (high) at any time
- If the n-bit coded information has unused combinations, the decoder has fewer than 2n outputs



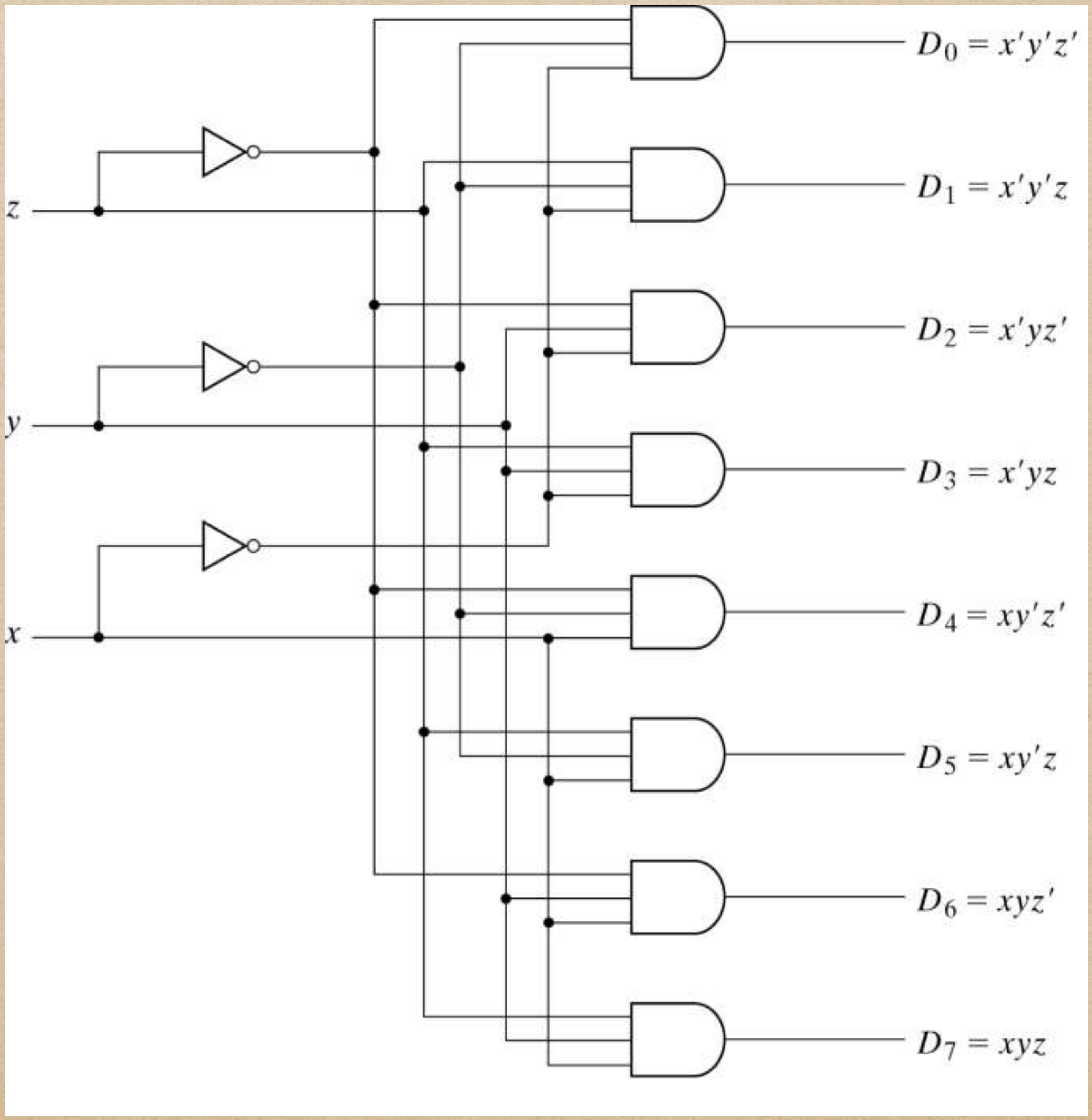
3-to-8-Line Decoder

- A 3-to-8-Line Decoder is a decoder in which three inputs are decoded into eight outputs, each representing one of the minterms of the three input variables
- Each one of the eight AND gates generates one of the minterms
- A particular application of this decoder is binary-to-octal conversion, however 3-to-8-line decoder can be used for decoding any 3-bit code to provide eight outputs, one for each element of the code

3-to-8-Line Decoder Truth Table

Inputs			Outputs							
X	Y	Z	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

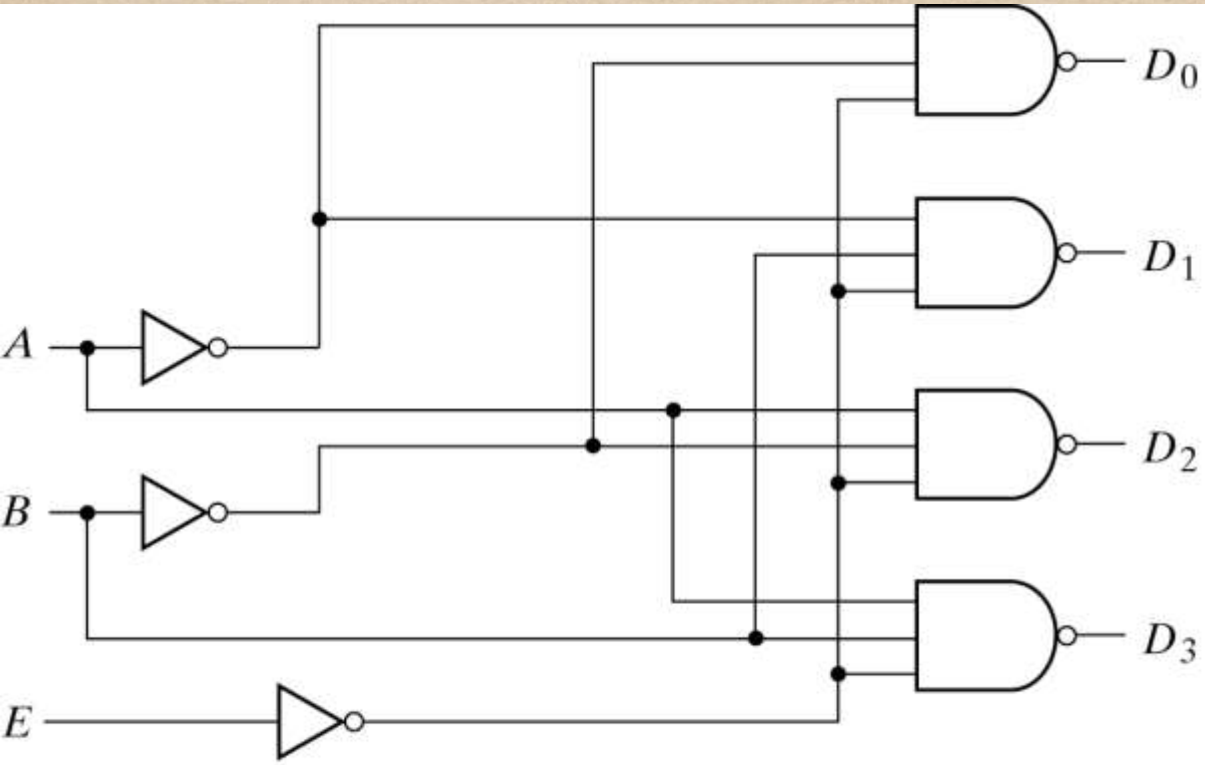
3-to-8-Line Decoder Implementation



Summary

- What is the function of a decoder?
  - It selects or de-select one of the devices

Decoders with NAND gates



(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

End of Lecture