Introduction to Sequential Logic, Latch and Flip Flop Circuits

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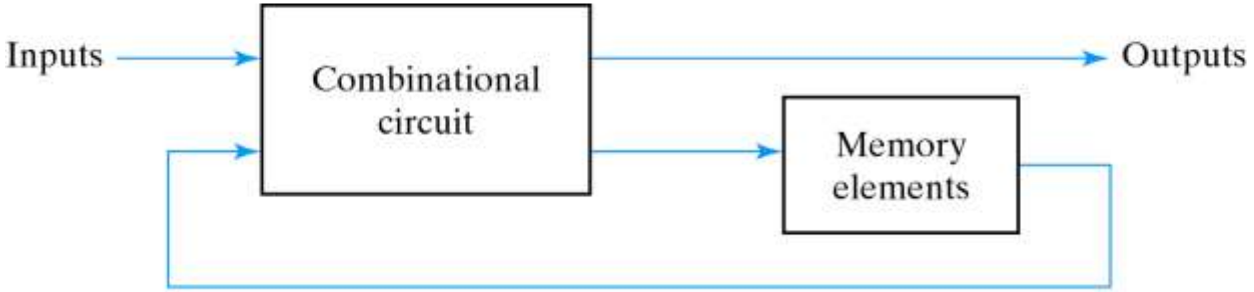
- Introduction to Sequential Logic
  - Synchoronnous Sequential Circuits
  - Asynchronous Sequential Circuits
- Latches
  - SR with NOR gates
  - SR with NAND gates

Sequential Circuits

- A sequential circuit consists of combinational circuits to which storage elements are connected to form a feedback path.
  - Storage elements store binary information.
  - Outputs of a sequential circuit are a function of the inputs and the internal state of the storage elements.
- State refers to the currently known condition of the circuit including what data is stored in the storage elements.
- A sequential circuit is specified by a time sequence of inputs, outputs, and internal states.

Sequential Circuit- Block Diagram

- **Block Diagram**



Sequential Circuit Types

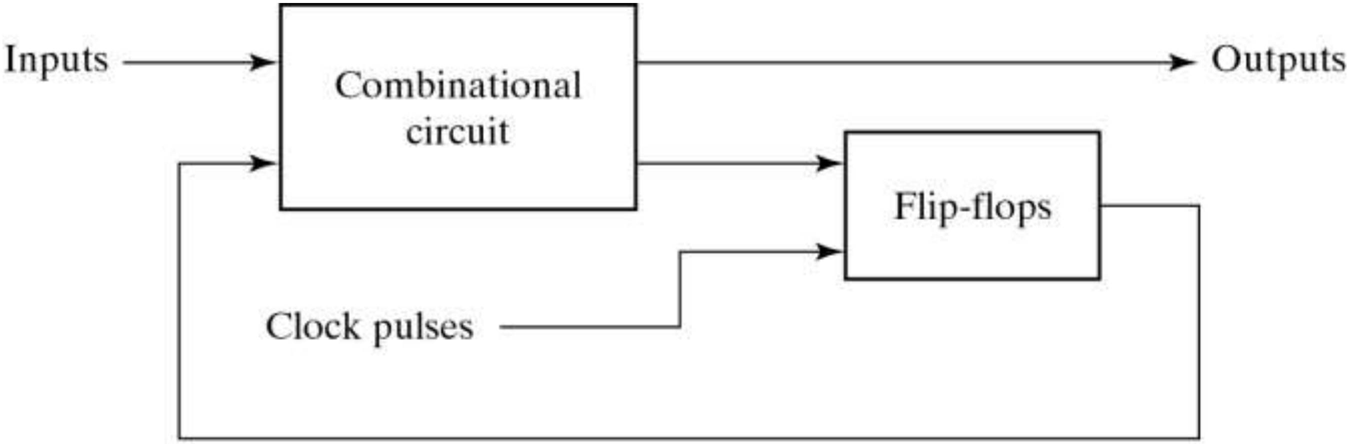
- **There are two types of sequential circuits Synchronous and Asynchronous :**
  - **A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time**
    - **» Storage elements in synchronous circuits are affected at discrete instants of time**
  - **An asynchronous sequential circuit depends on the input signals at any instant of time and the order in which the inputs change**
    - **» Storage elements in asynchronous circuits are usually time-delay devices**
    - **» The storage capability of time-delay devices is due to the time it takes for the signal to propagate through the device**
    - **» It is also regarded as combinational circuit with feedback**

Synchronous Sequential Circuit

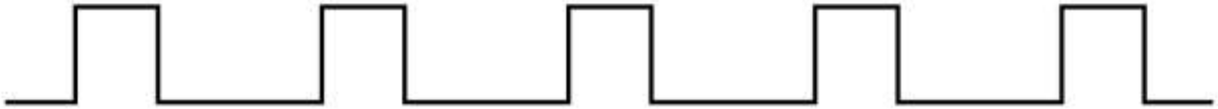
- Synchronization in synchronous sequential circuits is achieved by timing device called a clock generator
- A clock generator generate a periodic train of clock pulses
- The clock pulses are distributed throughout the system in such a way that storage elements are affected only with the arrival of each pulse
- Clock pulses are employed with other circuitry that indicates the changes to the storage elements.
- Synchronous sequential circuits that use clock pulses in the inputs of storage elements are called clocked sequential circuits.
- These are most commonly used having no instability problems
- The memory elements used in these circuits are flip-flops

Synchronous Sequential Circuit

- **Clocked Sequential Circuit**



(a) Block diagram



(b) Timing diagram of clock pulses

Flip Flop

- **The storage element used in clocked sequential circuits are called flip flops.**
  - **A flip flop is a binary storage device capable of storing one bit of information.**
  - **It has two outputs, one for the normal value and one for the complement value**
  - **Multiple flip flops can be used to store multiple bits.**
  - **Flip flops receive their inputs from a combinational circuit and a clock signal.**
  - **A Flip flop maintains a binary state indefinitely until directed by an input signal to switch states. The state of a flip flop can change only during a clock pulse.**

Latches

- A flip flop circuit can maintain a binary state indefinitely until directed by an input signal to switch states.
  - Flip flops are categorized by the number of inputs they possess and the manner in which the inputs affect the binary state.
- Latches are the most basic flip flop and they operate with signal levels.
- Latches are the building blocks for all flip flops.

SR Latch

- **The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates.**
  - **There are two inputs:**
    - **S is for set**
    - **R is for reset**
  - **There are two outputs Q and Q'**

Review

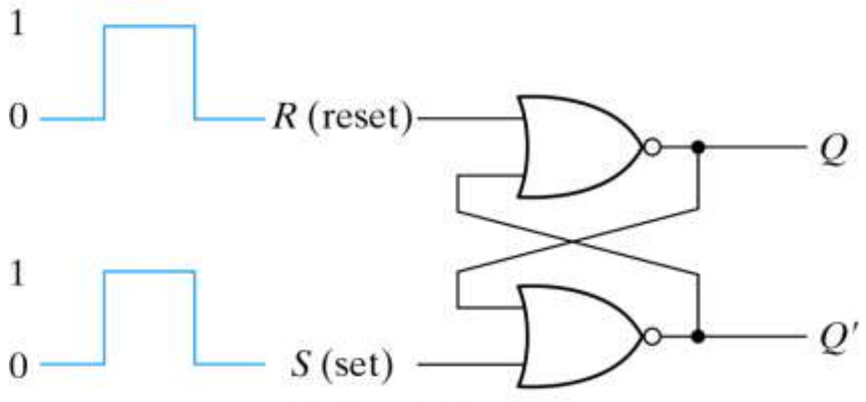
- Two type of Sequential Circuits?
  - Synchronous Sequential Circuits?
    - Behaviour is defined by at periodic time defined by clock
  - Asynchronous Sequential Circuits?
    - Changes can take place at any time instance
- Difference between Latch and Flip Flop?
  - Latch is level sensitive
  - Flip Flop is edge sensitive
  - Flip Flop is made up of latches

SR Latch

- **The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates.**
  - **There are two inputs:**
    - **S is for set**
    - **R is for reset**
  - **There are two outputs Q and Q'**

SR Latch Logic (NOR Gates)

- **The SR latch with NOR Gates has two useful states**
  - **When Q = 1 and Q’ = 0 the latch is said to be in a set state.**
  - **When Q = 0 and Q’ = 1 the latch is said to be in a reset state.**
  - **Q and Q’ are normally complement of each other. When both inputs are equal to 1 at the same time, an undefined state with both outputs equal to 0 occurs**



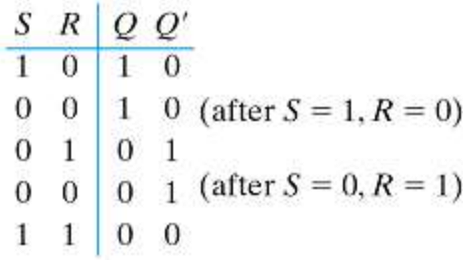
(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(b) Function table

SR Latch (NOR) Logic

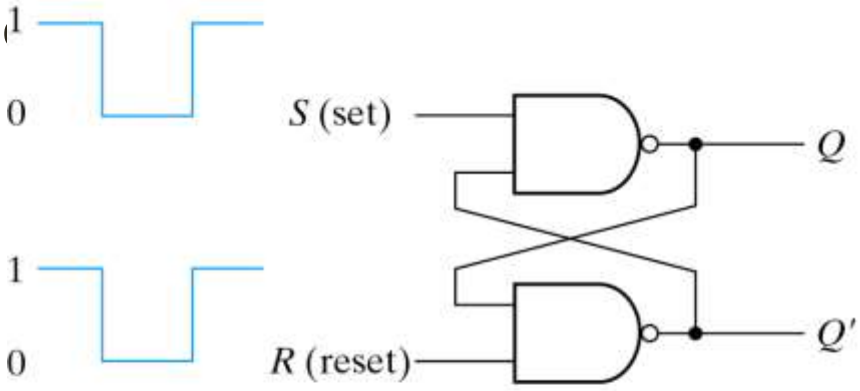
- Normally the two inputs to the SR latch (NOR) are left at 0.
- If the state needs to be changed then the application of a momentary 1 to the S input causes the latch to go to the set state.
  - The S input must go back to 0 before any other changes to avoid the occurrence of the undefined state. The circuit remains in set state.
- A momentary 1 to the R input causes the latch to go to the reset state.
  - The R input must go back to 0 before any other changes to avoid the occurrence of the undefined state. The circuit remains in reset state.
- If a 1 is applied to both S and R then the outputs both go to 0, the undefined state.



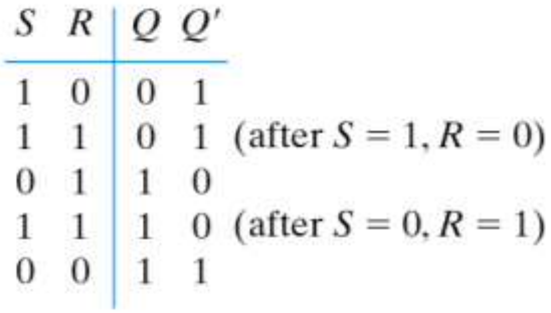
S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

SR Latch Logic (NAND Gates)

- The SR latch with NAND Gates has two useful states
  - When Q = 1 and Q’ = 0 the latch is said to be in a set state.
  - When Q = 0 and Q’ = 1 the latch is said to be in a reset state.
  - Q and Q’ are normally complement of each other. When both inputs are equal to 0 at the same time, an undefined state with both outputs equal to 1



(a) Logic diagram

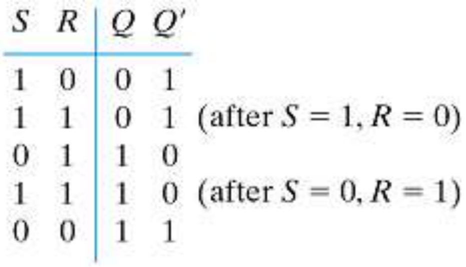


S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(b) Function table

SR Latch (NAND) Logic

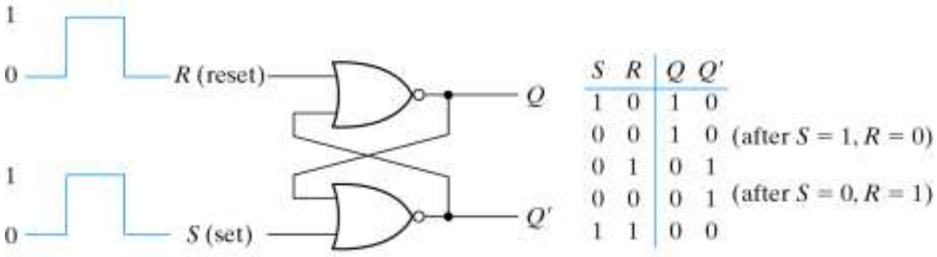
- Normally the two inputs to the SR latch (NAND) are left at 1.
- If the state needs to be changed then the application of a momentary 0 to the S input causes the latch to go to the set state.
  - The S input must go back to 1 before any other changes to avoid the occurrence of the undefined state. The circuit remains in set state.
- A momentary 0 to the R input causes the latch to go to the reset state.
  - The R input must go back to 1 before any other changes to avoid the occurrence of the undefined state. The circuit remains in reset state.
- If a 0 is applied to both S and R then the outputs both go to 1, the undefined state.



S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

NAND vs. NOR Implementations

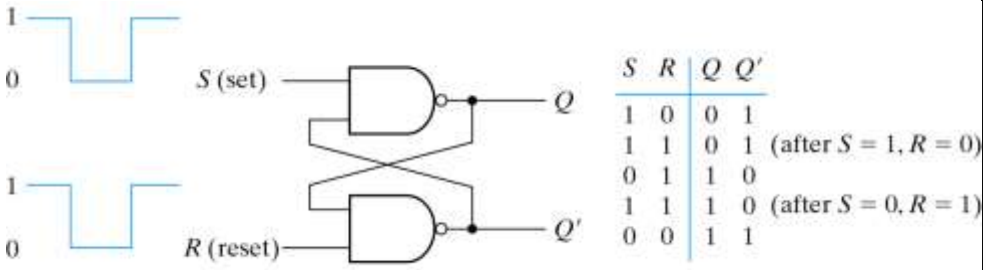
- The input signals for the NAND latch requires the complement of those values used for the NOR latch
- Because the NAND latch requires a 0 signal it is sometimes called a S’-R’ latch.



S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(a) Logic diagram (b) Function table

Fig. 5-3 *SR* Latch with NOR Gates



S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

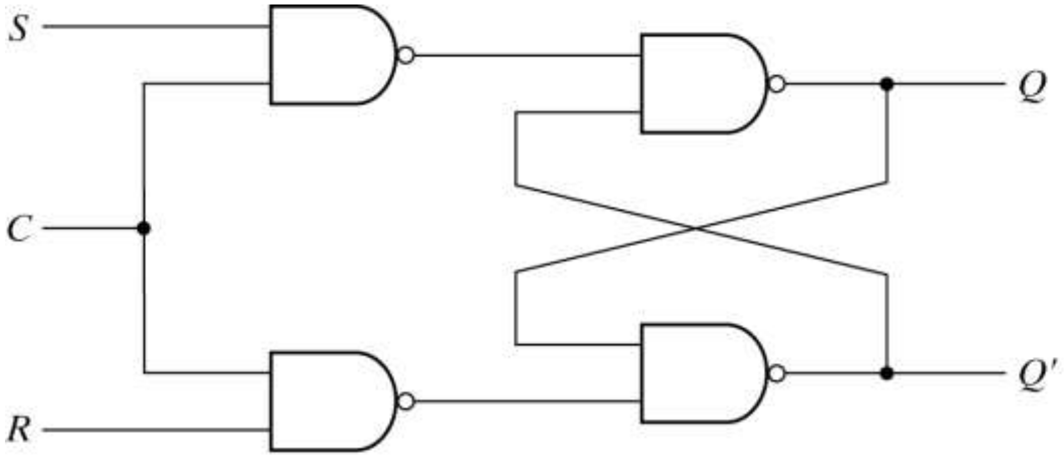
(a) Logic diagram (b) Function table

Fig. 5-4 *SR* Latch with NAND Gates

- D Latch Logic
- Modifying Latches to make Flip Flops

SR Latch With Control Input

- Gated SR Latch



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

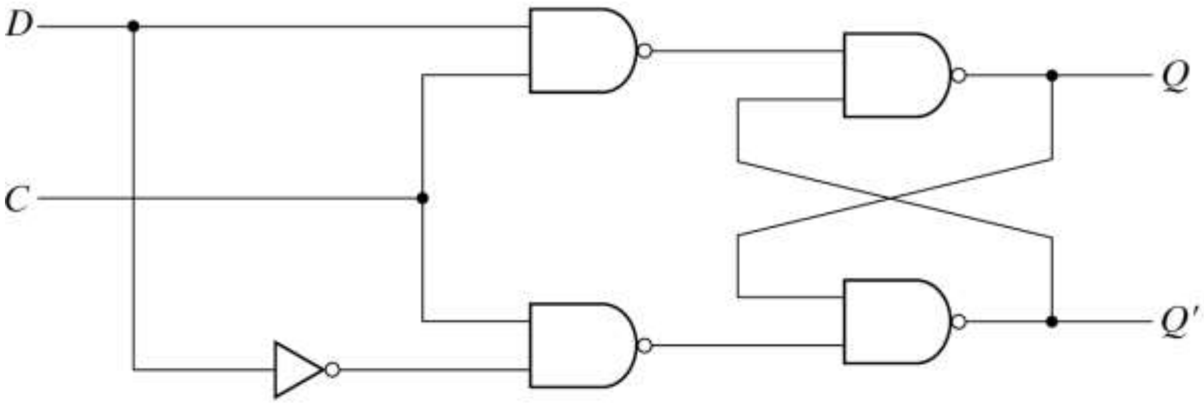
(b) Function table

SR Latch Modification

- The basic SR latch can be modified by providing an additional control input that determines when the state of the latch can be changed.
  - The following example uses the C enable input with 1 allowing inputs S and R to flow through and 0 disallowing the flow of the inputs S and R. In other words S and R are allowed to change the flip-flop only when C = 1 and If C=0, S and R can't change output
  - It consists of basic SR latch and two additional NAND gates
  - The control input C acts as an enable input for the other two inputs
  - The output of the NAND gates stay at the logic 1 level as long as the control input remains at 0. This is quiescent (inactive) state.
  - When the control input goes to 1, the information for S or R is allowed to effect the SR latch (active state)
  - The set state is reached with S=1, R=0 and C=1. To change to the reset state, the inputs must be S=0, R=1 and C=1. In either cases when C returns to 0, the circuit remains in its current state

D Latch Logic

- Gated D Latch



(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	$Q = 0$; Reset state
1	1	$Q = 1$; Set state

(b) Function table

D Latch

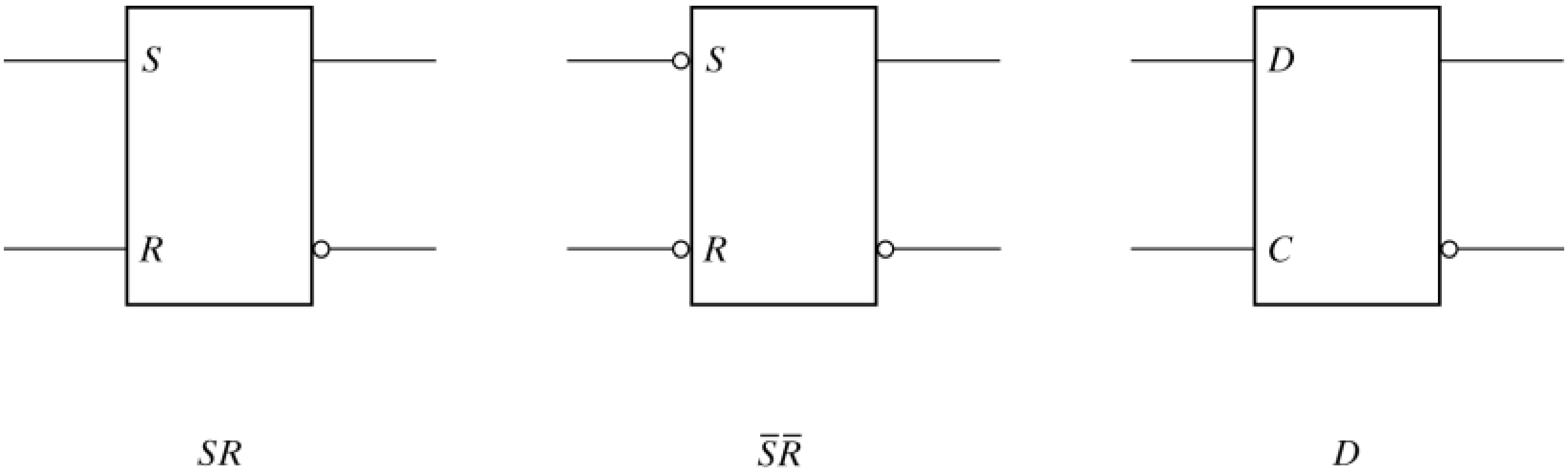
- A D latch modifies the SR latch to avoid the undesirable condition of the indeterminate state by ensuring that S and R are never equal to 1 at the same time.
  - There are only two inputs:
    - D is the data input
    - C is the control input
  - The D input goes directly to the S input and its complement goes to the R input.
  - When control input C is left at 0 the state of the latch remains constant (regardless of value of D).
  - If C = 1 and D = 1 the output Q goes to 1, placing the circuit in the set state.
  - If C = 1 and D = 0 the output Q goes to 0, placing the circuit in the reset state.

Notes on D Latches

- The D Latch has the ability to hold data in its internal storage.
- The data input of the D latch is transferred to the Q output when the control input is enabled.
  - The output follows changes in the data input as long as the control input is enabled.
  - For this reason, the latch is also called the transparent latch.
- When the control input is disabled, the output of the latch remains in the state it was in just prior to the control input being disabled.

Graphic Symbols for Latches

- IEEE Symbols

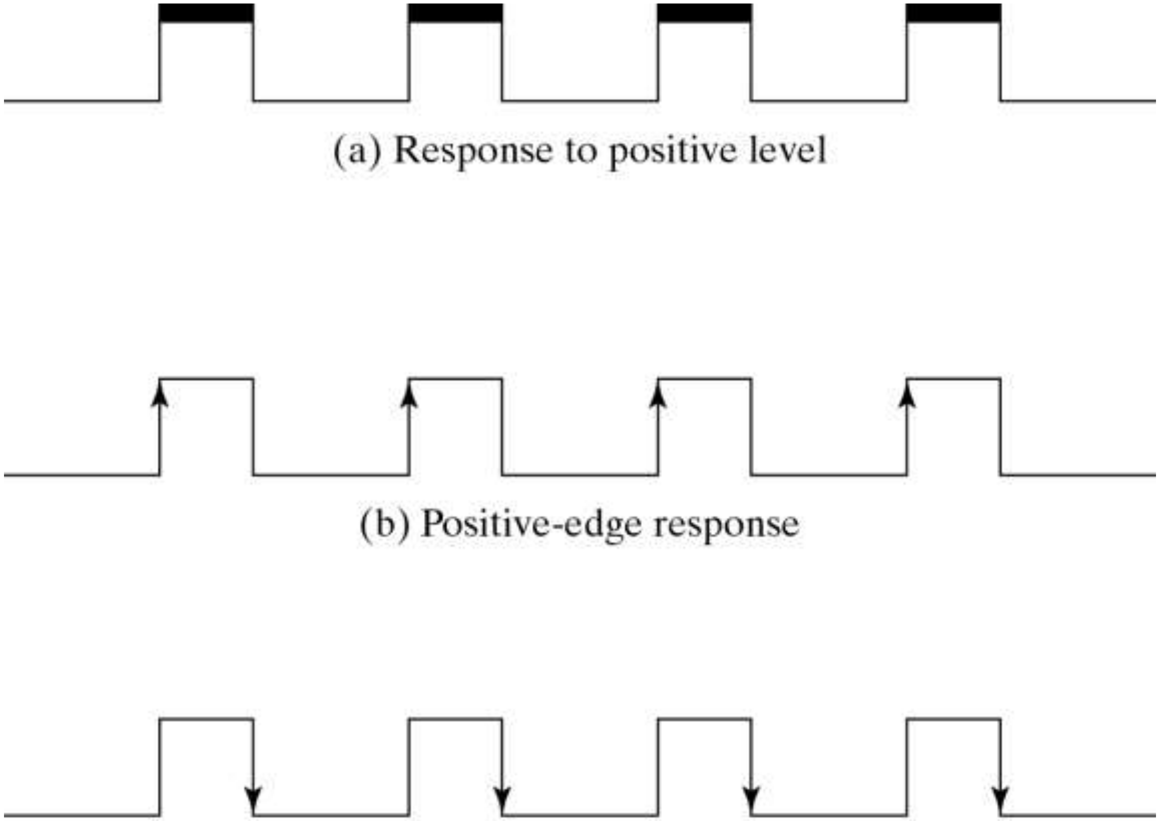


~~S~~ ~~R~~ : NAND gate Latch

Problems With Latches

- The problem with the latch is that it responds to a change in the level of a clock pulse.
  - A positive level response in the control input allows changes in the output when the D input changes while the clock pulse stays at logic-1.
- The key to solving the latch problem in flip flops is to ensure that changes are only allowed to occur during a signal transitions (at the point in value change).
  - A positive transition is called a positive-edge response.
  - A negative transition is called a negative-edge response.

Clock Responses



(a) Response to positive level

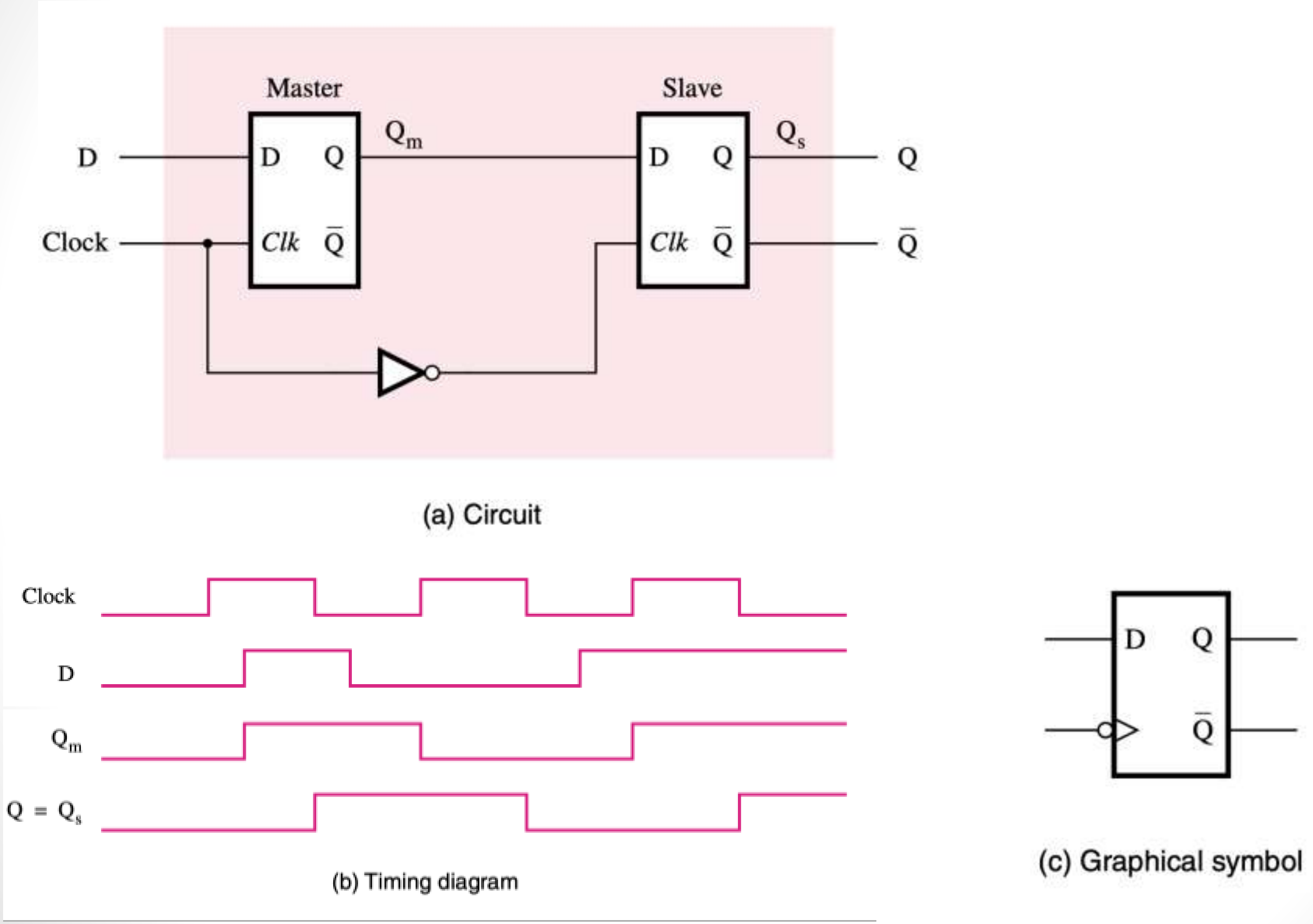
(b) Positive-edge response

(c) Negative-edge response

Modifying Latches

- There are two ways that a latch can be modified to form a flip-flop.
  - One way is to employ two latches in a special configuration that isolates the output of the flip-flop from being affected while its input is changing.
  - Another way is to produce a flip-flop that triggers only during a signal transition (from 0 to 1 or from 1 to 0), and is disabled during the rest of the clock pulse duration.

Master Slave D Flip Flop



(a) Circuit

(b) Timing diagram

(c) Graphical symbol

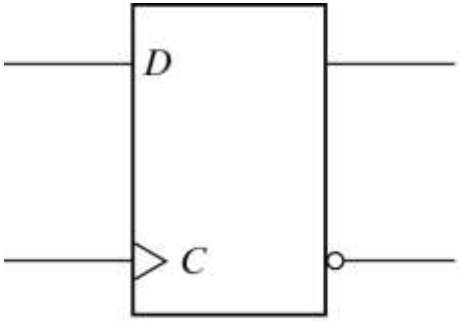
Edge-Triggered D Flip-Flop

- An edge-triggered D flip flop is constructed with two D latches and an inverter.
  - The first latch is called the master and second the slave.
  - The circuit samples the D input and changes its output Q only at the negative-edge of the controlling clock.
  - When the clock is 0, the output of the inverter is 1, the slave latch is enabled and its output Q is equal to the master output Y.
    - The master latch is disabled because the clock is 0.
  - When the input pulse changes to the logic 1 level, the data from the external D input is transferred to the master.
    - The slave is disabled as long as the clock remains in the 1 level because its C input is equal to 0.
    - Any change in the input changes the master output at Y, but cannot affect the slave output.
    - When the pulse returns to 0 the master is disabled and the slave is enabled causing the value of Y to be transferred to output Q.

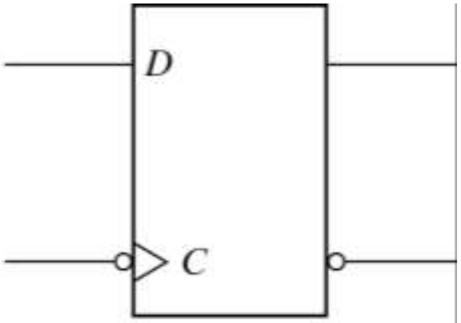
Edge Transition

- The previous implementation uses a negative edge transition.
  - The output only changes during the negative edge of the clock.
- A positive edge transition implementation can be constructed by placing an inverter on the CLK input prior to any other gate or inverter. i.e. between the CLK terminal and the junction between the other inverter and input C of the master latch.
- Such flip flop is triggered with a negative pulse, so that negative edge of the clock affects the master and the positive edge affects the slave and the output terminal

Edge-Triggered D Flip Flop Graphic Symbols

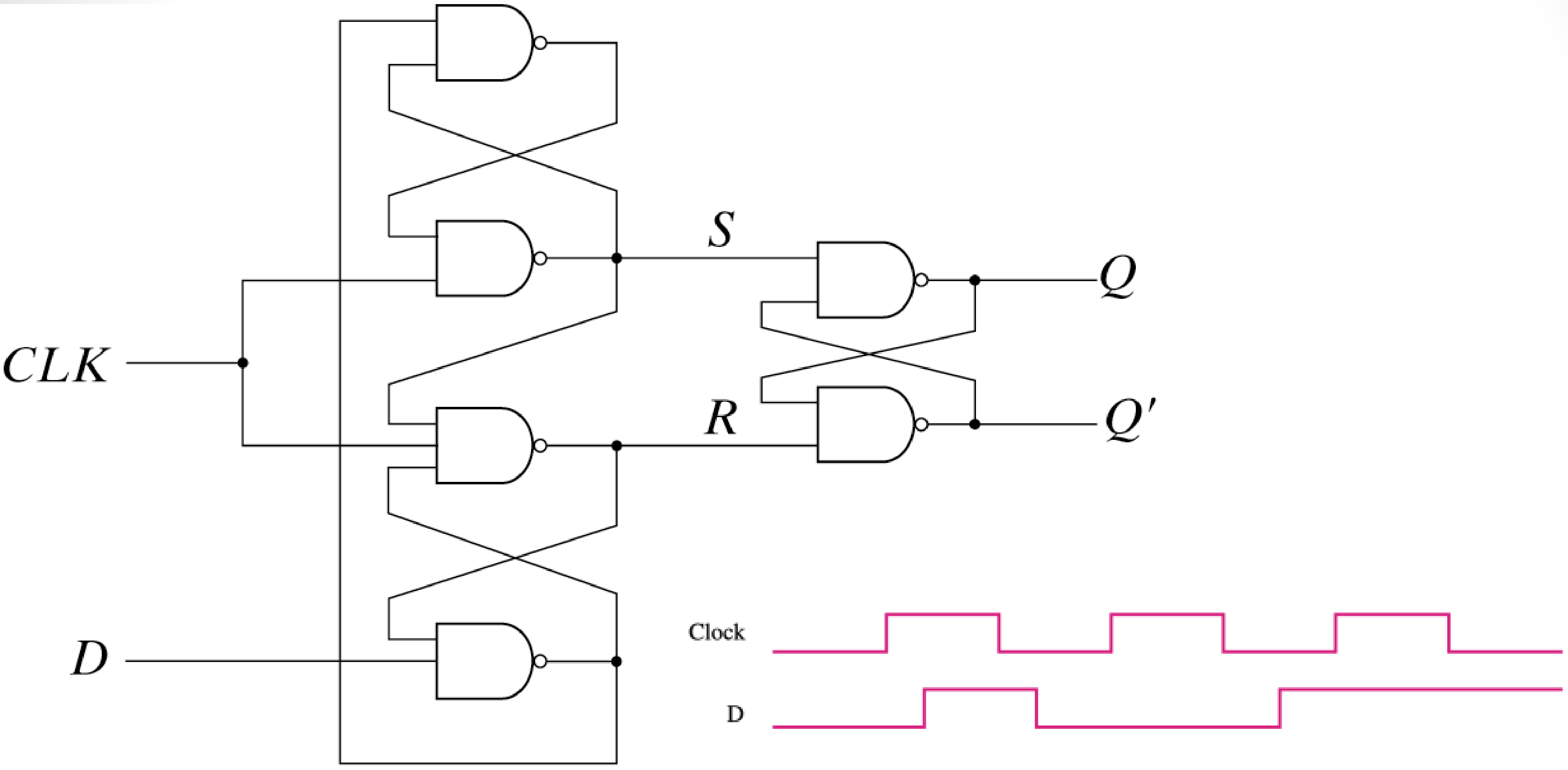


(a) Positive-edge



(a) Negative-edge

3 – SR Latch Flip Flop



Alternative Positive Edge Flip Flop

- A more efficient construction of an edge-triggered D flip flop uses three SR latches.
  - Two latches respond to the external D (data) and CLK (clock) inputs.
  - The third latch provides the outputs for the flip flop.
  - The S and R inputs of the output latch are maintained at logic 1 level when CLK = 0 causing the output to remain in its present state.
  - If D = 0 when CLK = 1, R changes to 0 causing a reset state and making Q = 0.
  - If there is a change in D while CLK = 1, terminal R remains at 0, thus locking out the flip flop (unresponsive to further changes in the input).
  - If D = 1 when CLK = 1, S changes to 0 causing the circuit to go to the set state making Q = 1.

D-Type Positive Edge Triggered Flip Flop – Summary

- When the input clock makes the positive transition, the value of D is transferred to Q
- A negative transition from 1 to 0 (or steady CLK state: logic 1 or logic 0) doesn’t affect the output
- This flip flop respond to transition from 0 to 1 only

Notes on Flip Flops

- The timing of the response of a flip flop to input data and clock must be taken into consideration when using edge-triggered flip flops.
- There is a minimum time, called setup time, for which the D input must be maintained at a constant value prior to the occurrence of the clock transition.
- There is a minimum time, called hold time, for which the D input must not change after the application of the positive transition of the clock.
- The propagation delay time of the flip flop is defined as the time interval between the trigger edge and the stabilization of the output to a new state.

The End