



**The University of Jordan**  
**School of Engineering**  
**Department of Computer Engineering**  
**First semester (2023-2024).**

## **VLSI Lab**

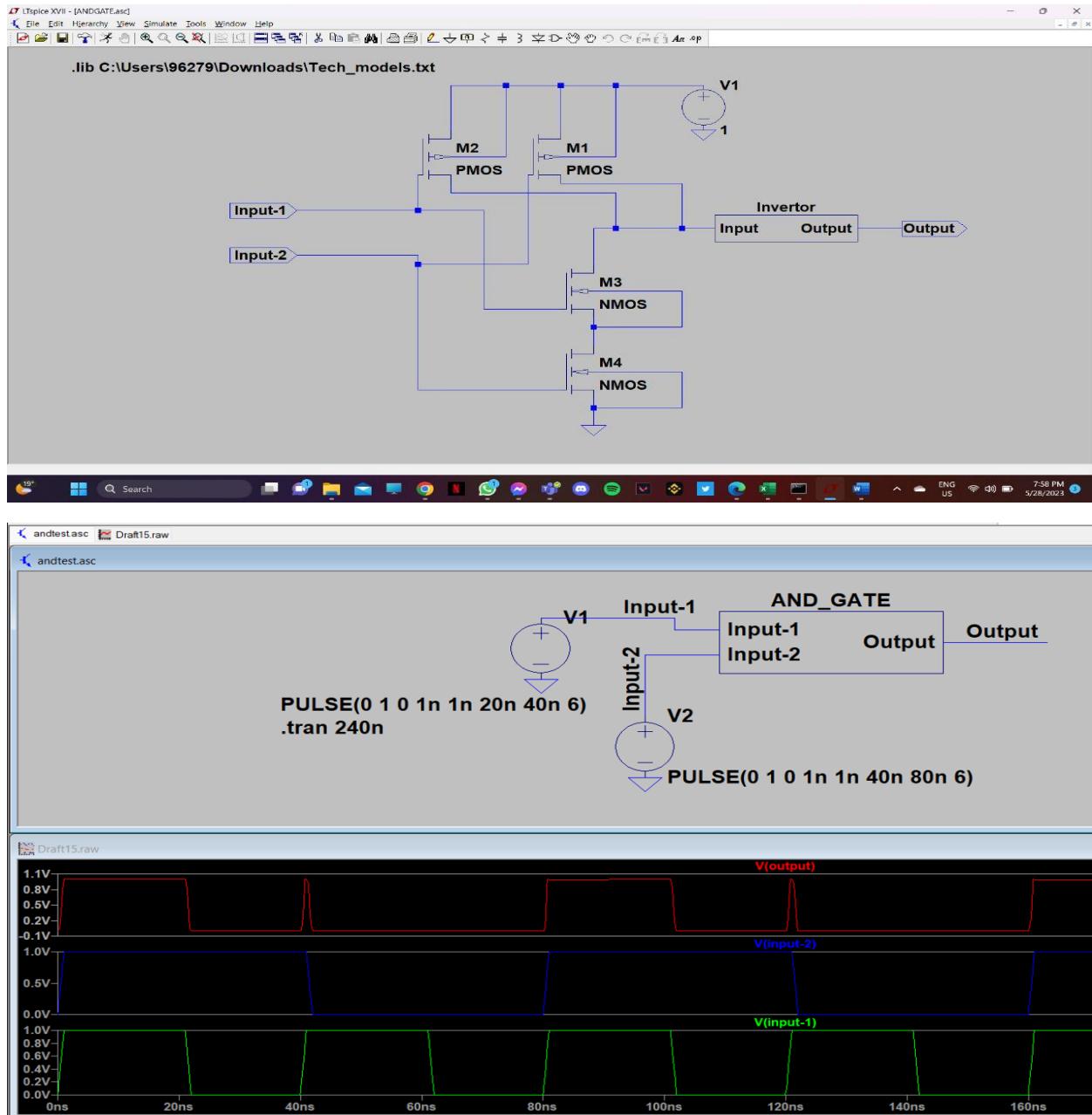
**Done by:**

- Hamzeh Al Masri (0197900)**
- Hamza Qtaishat(0171273)**

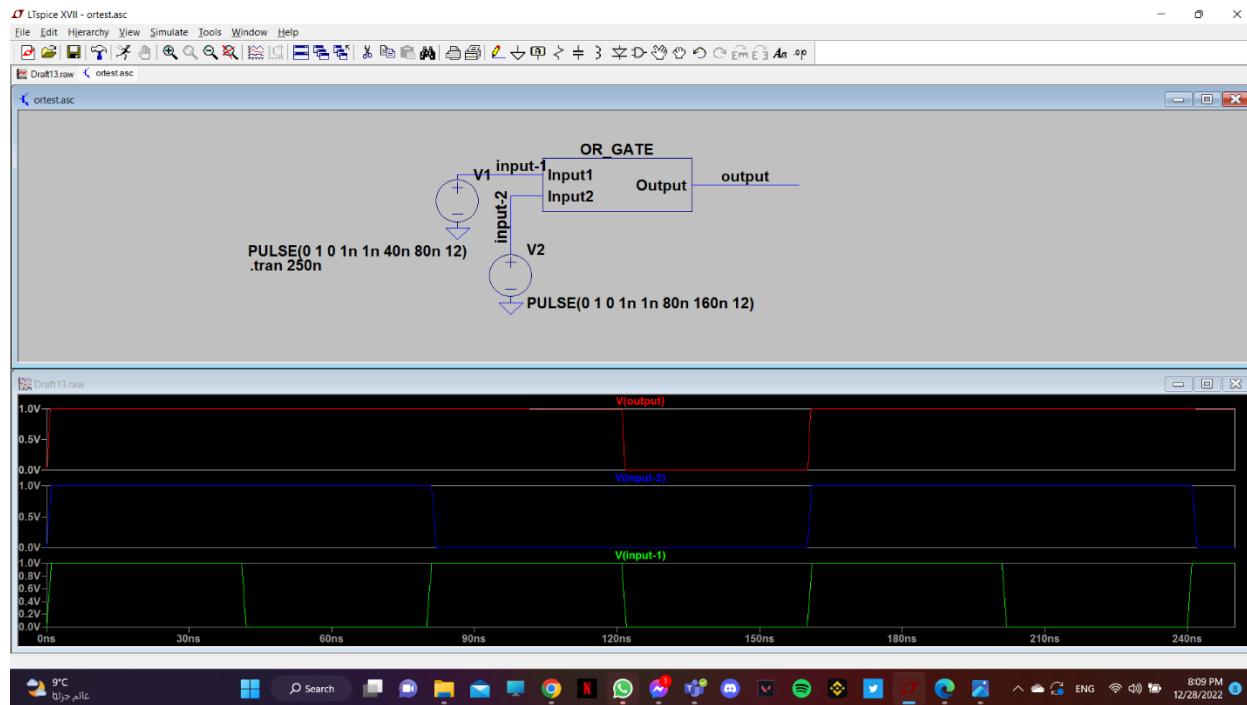
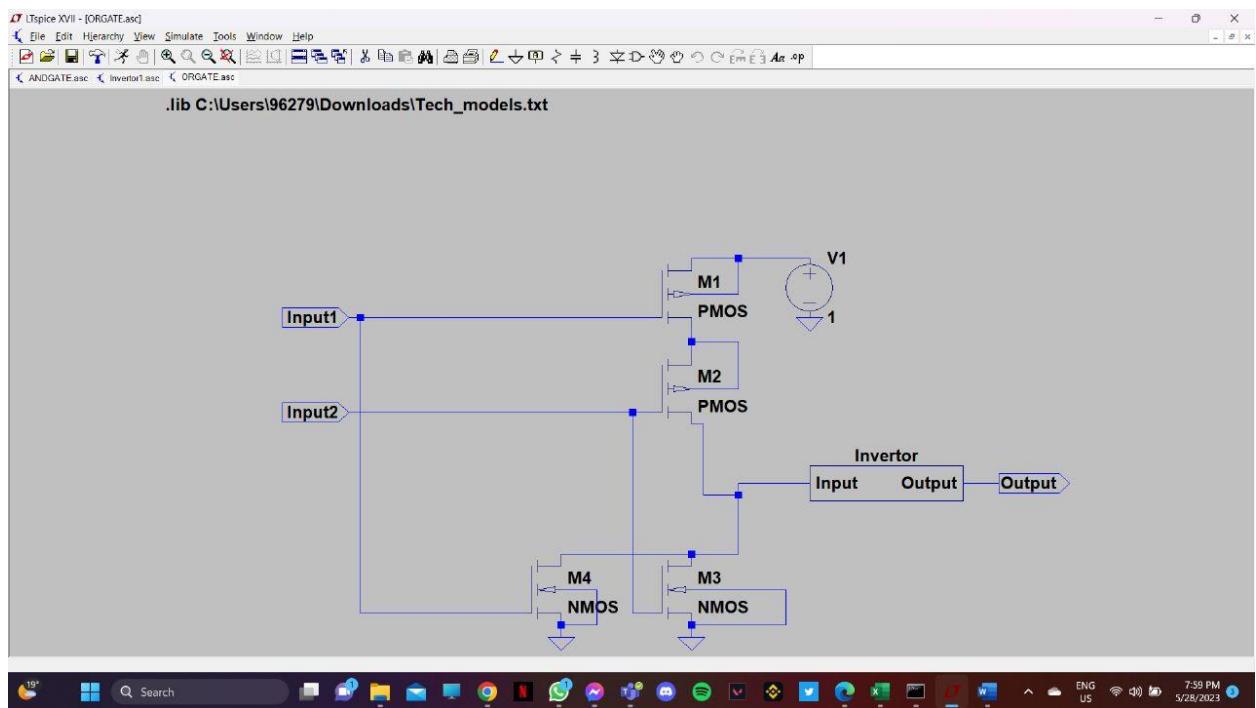
# Schematic

## • 2 bit XOR Gate

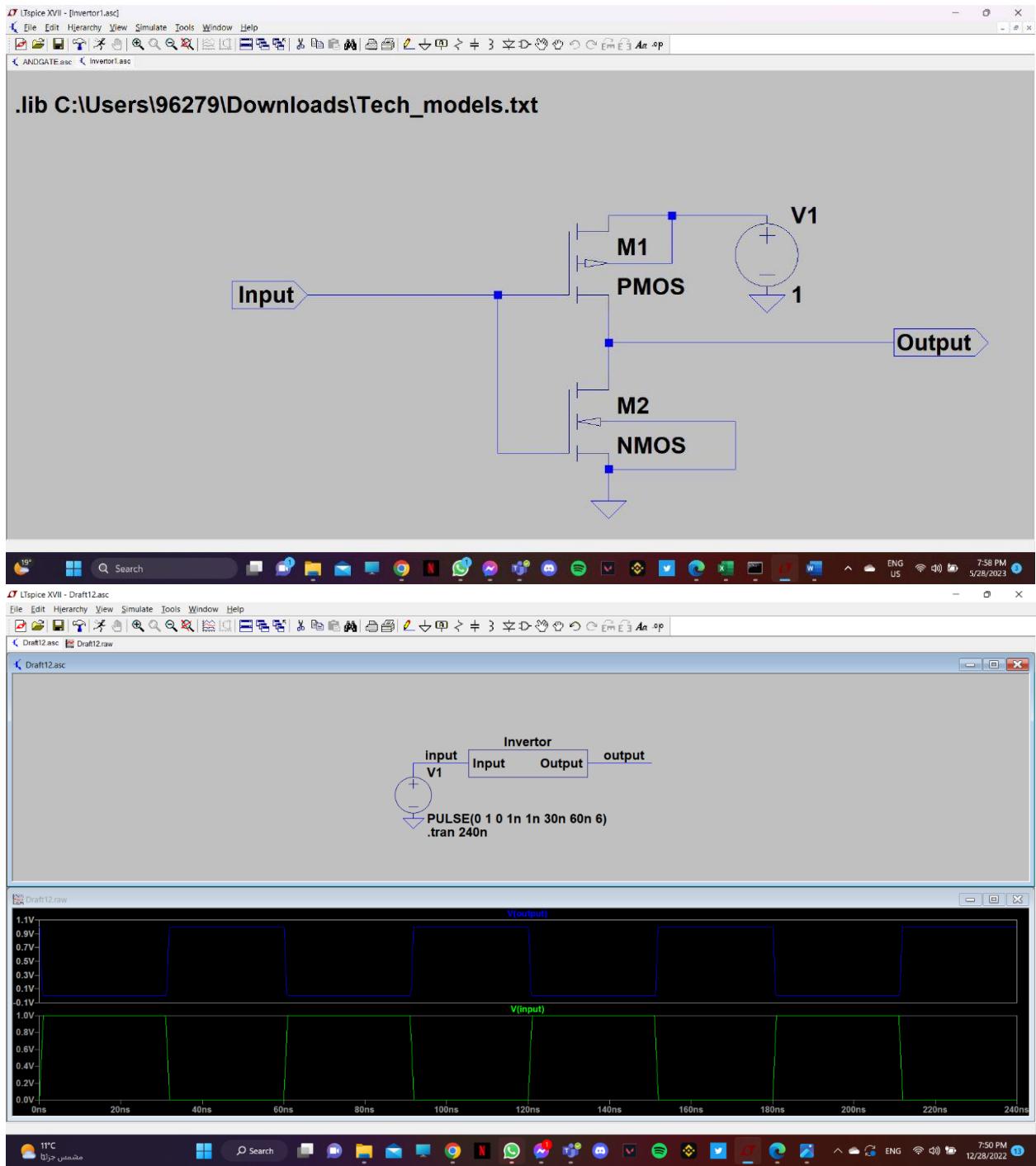
### - And Gate



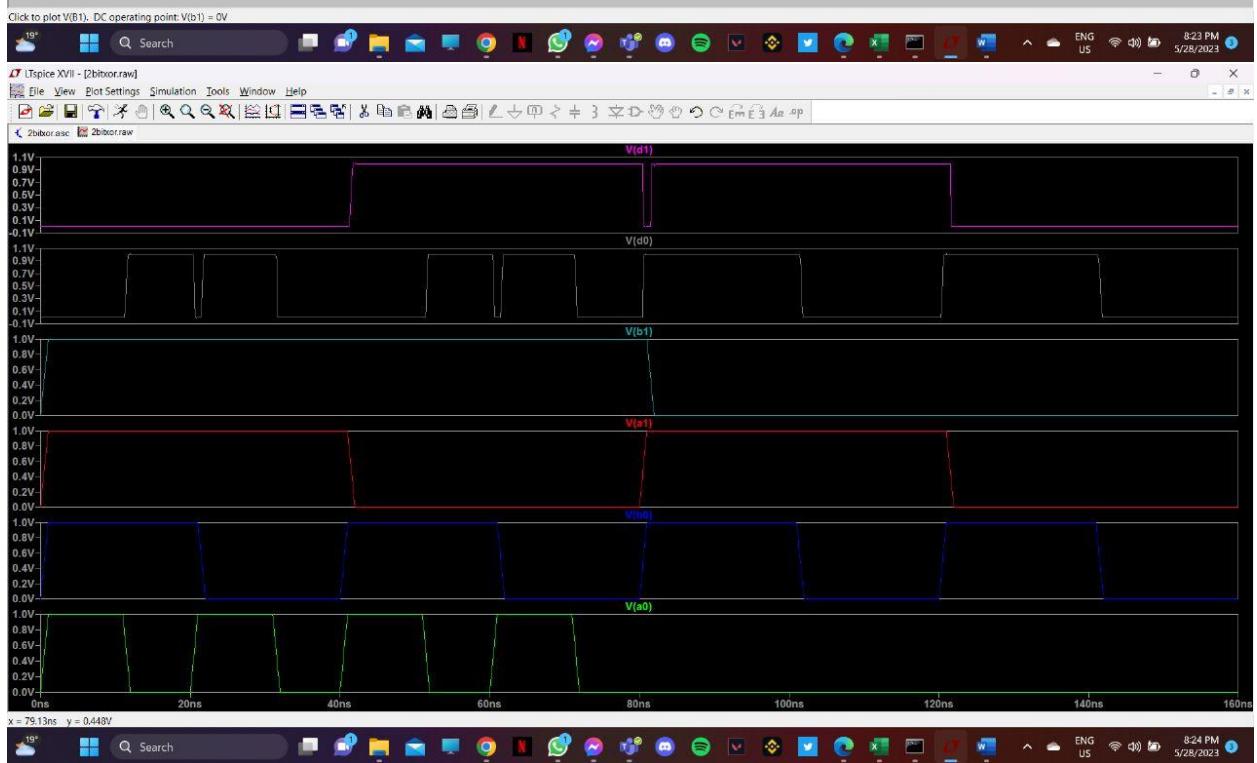
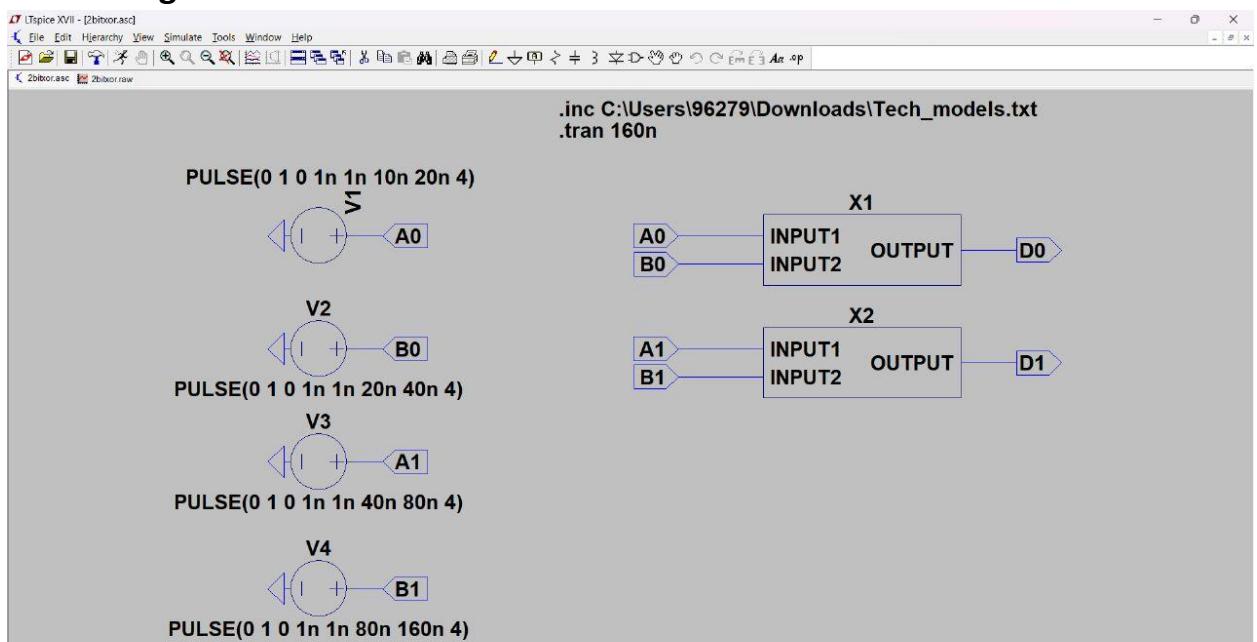
## - Or Gate



## - Inverter

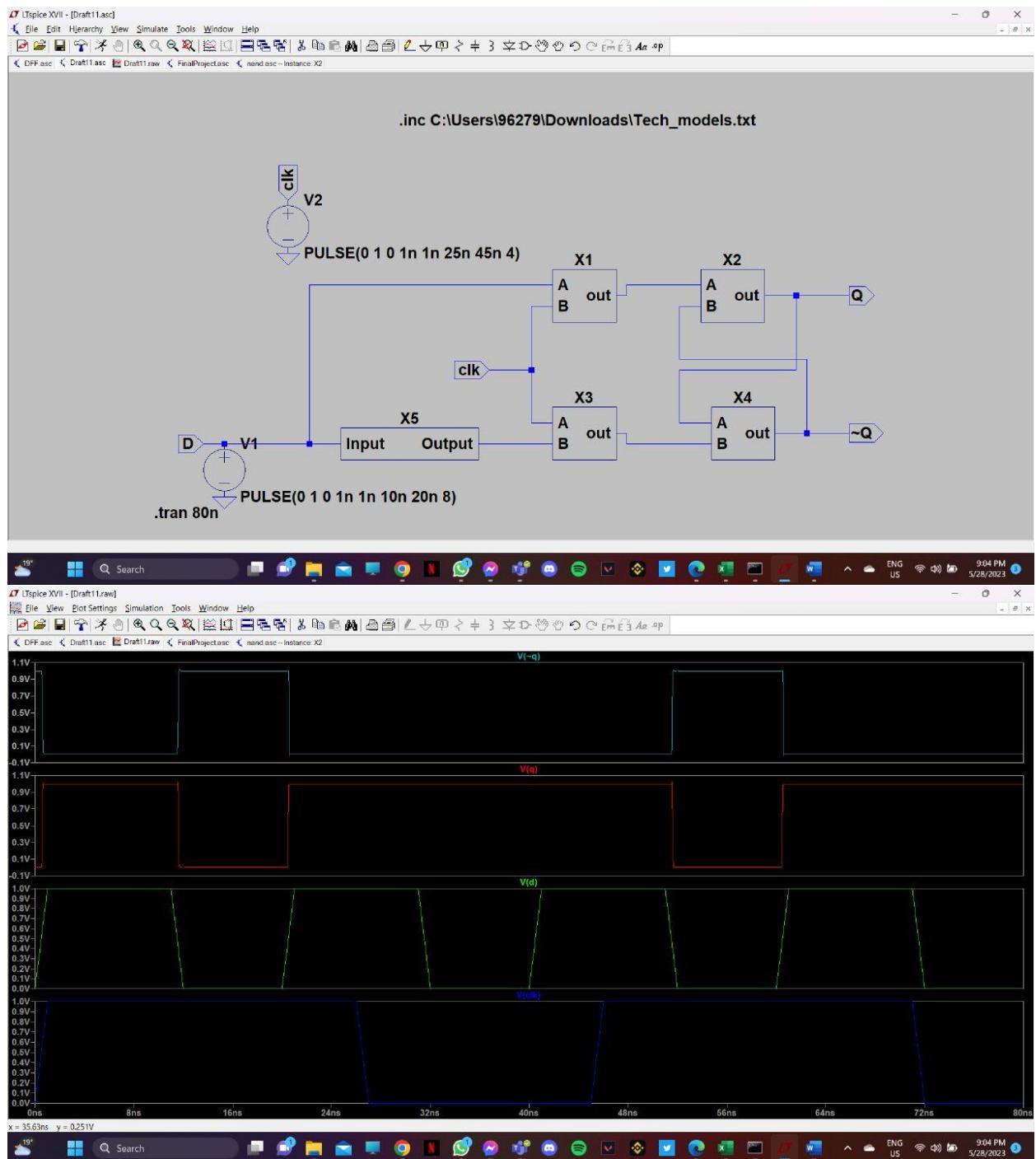


## - 2 bit XOR gate

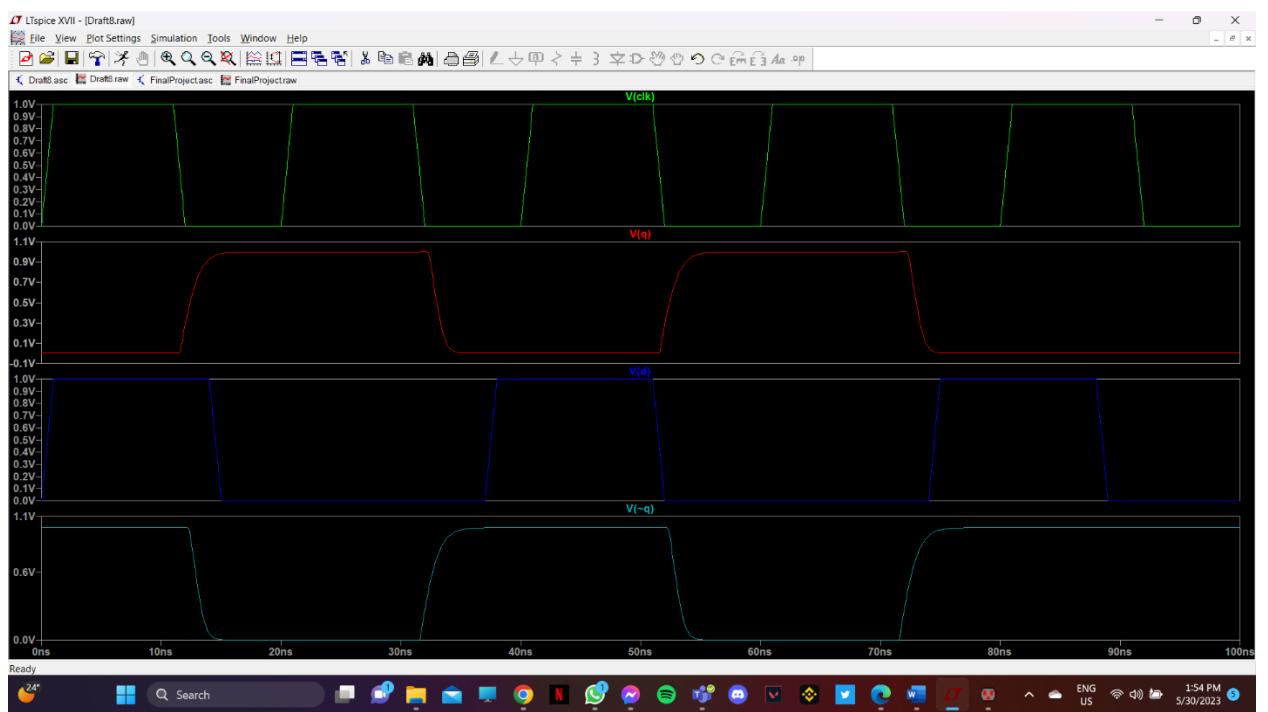
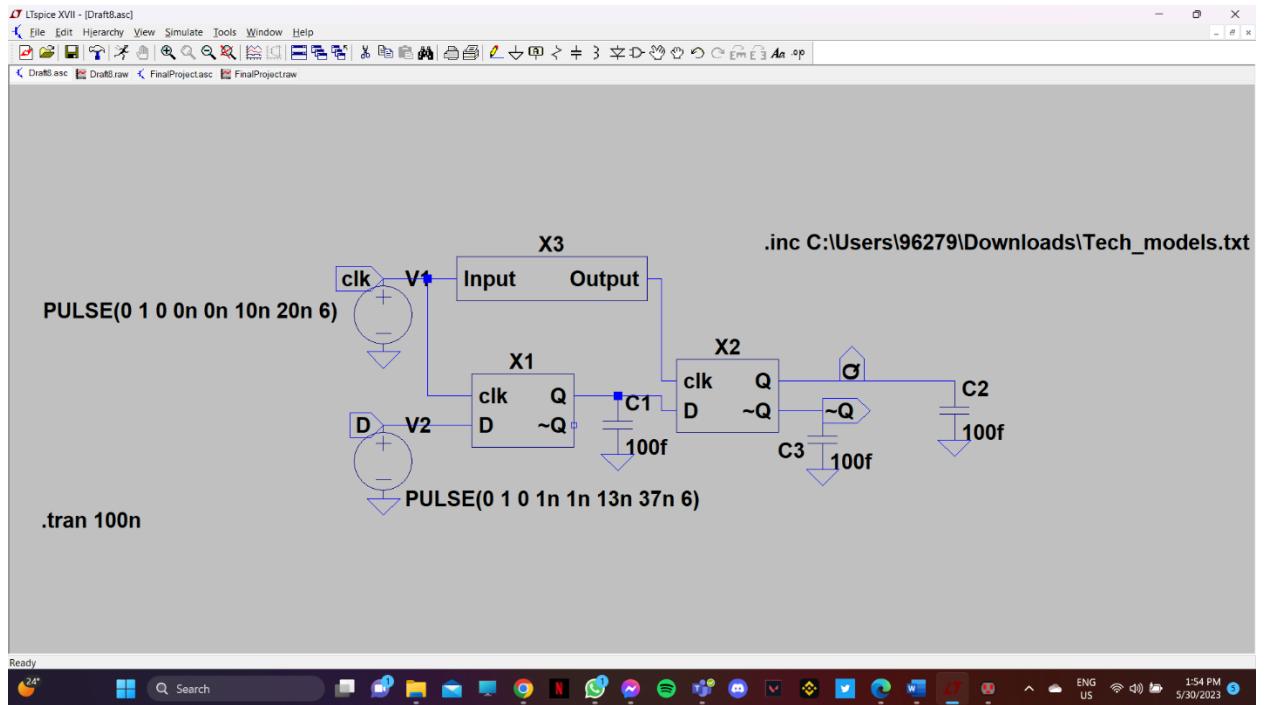


- Pipeline register

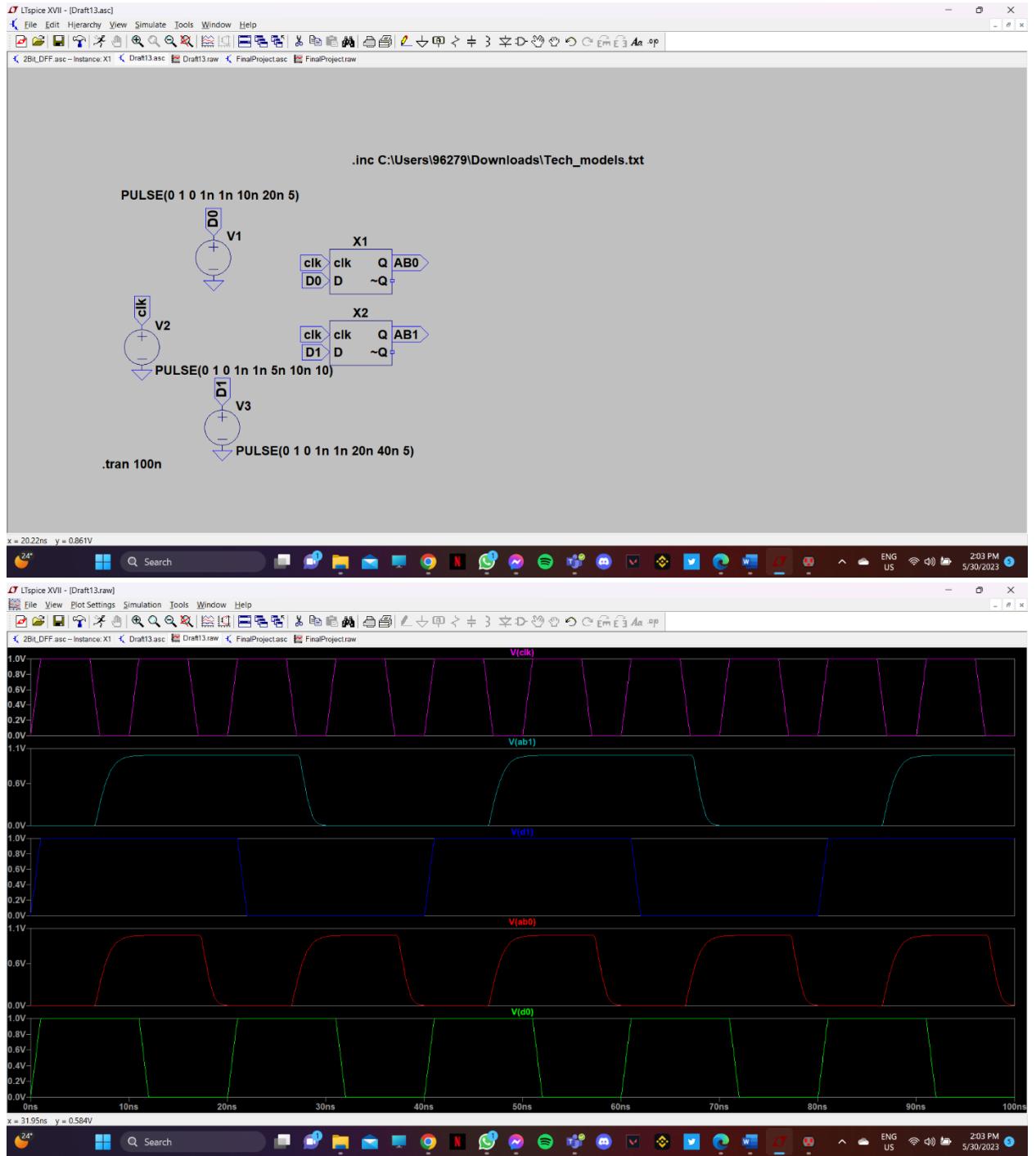
## D-latch



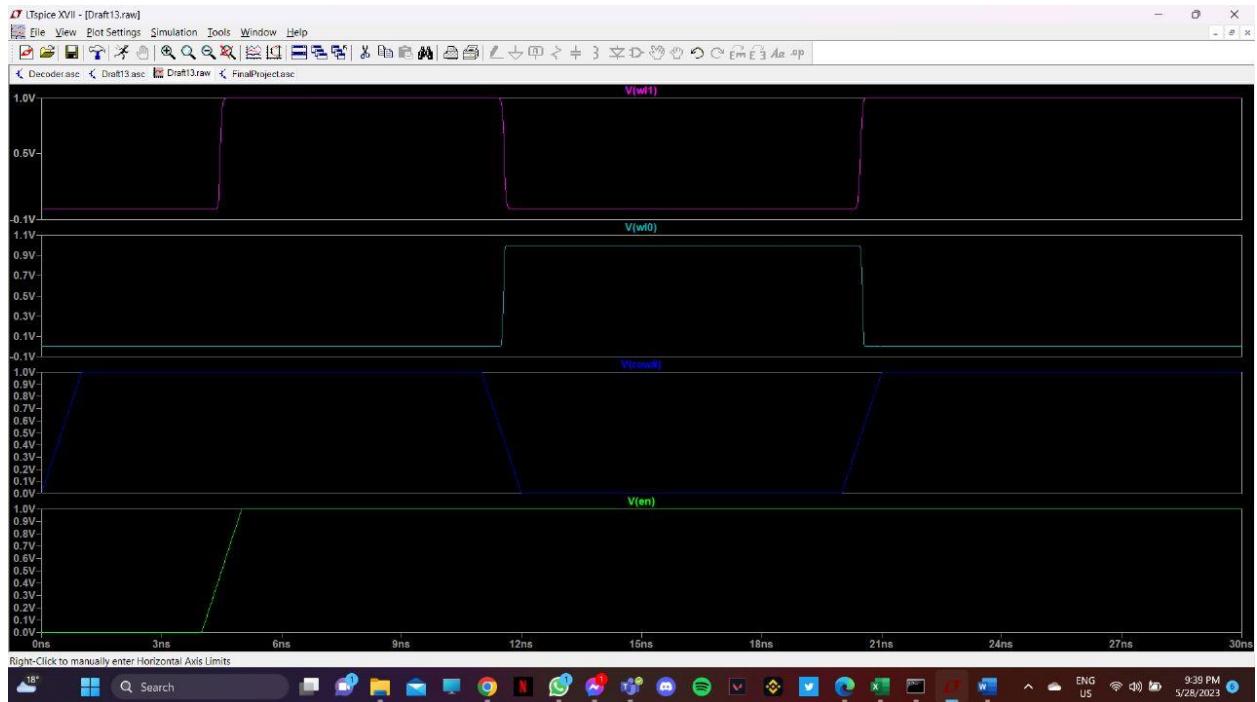
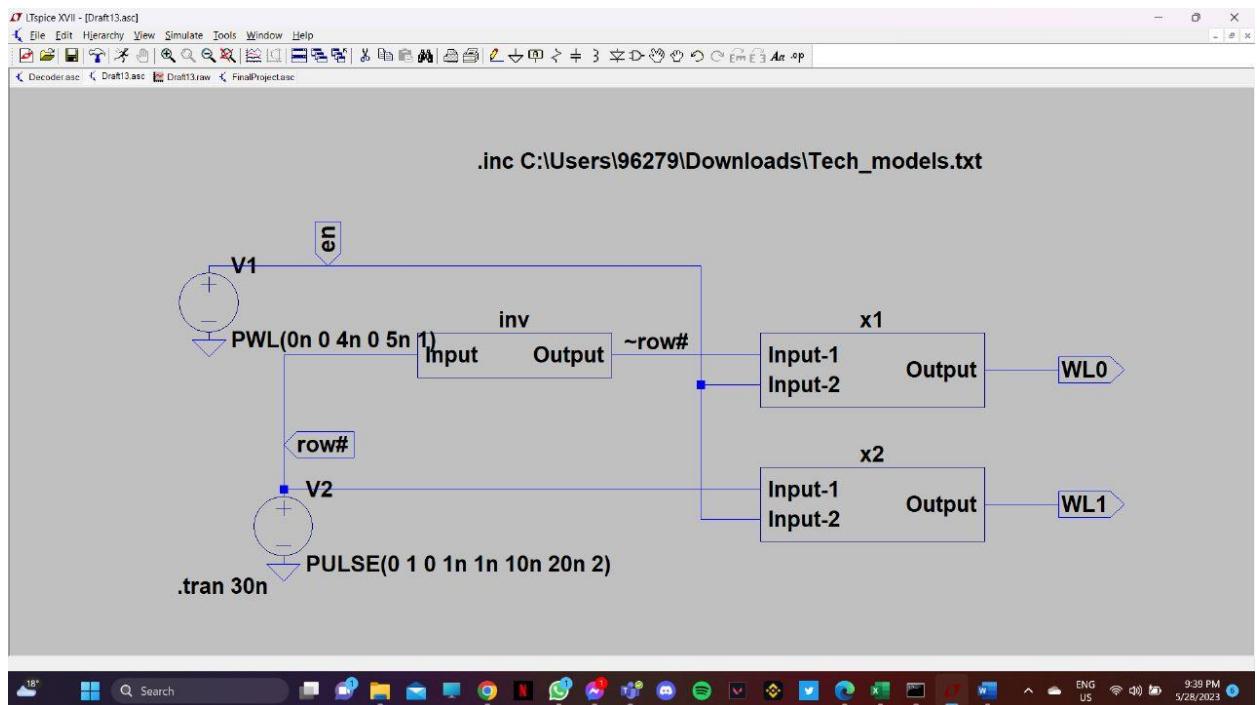
## - Master-Slave DFF



## 2-bit Master-Slave DFF

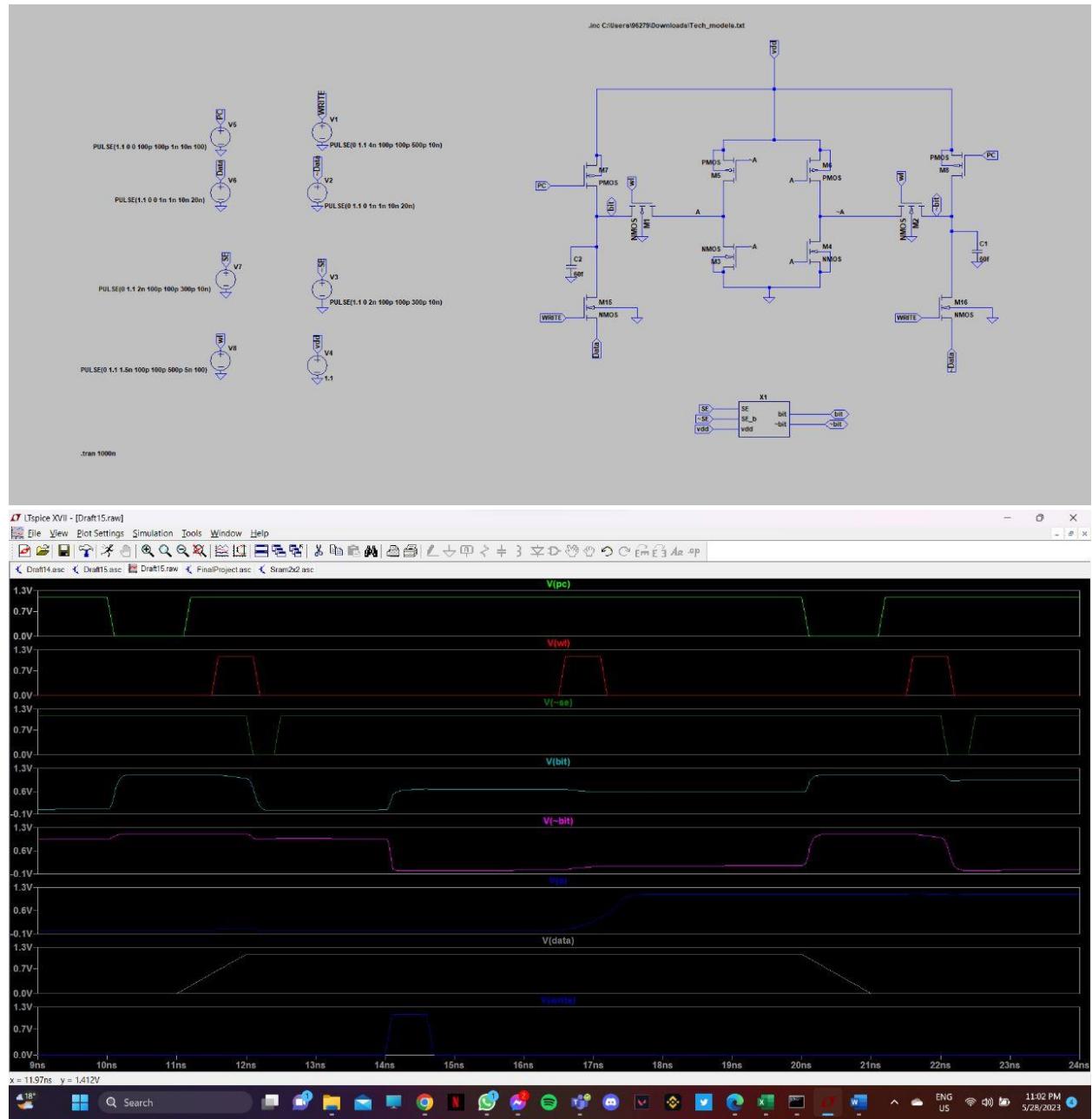


## • Decoder

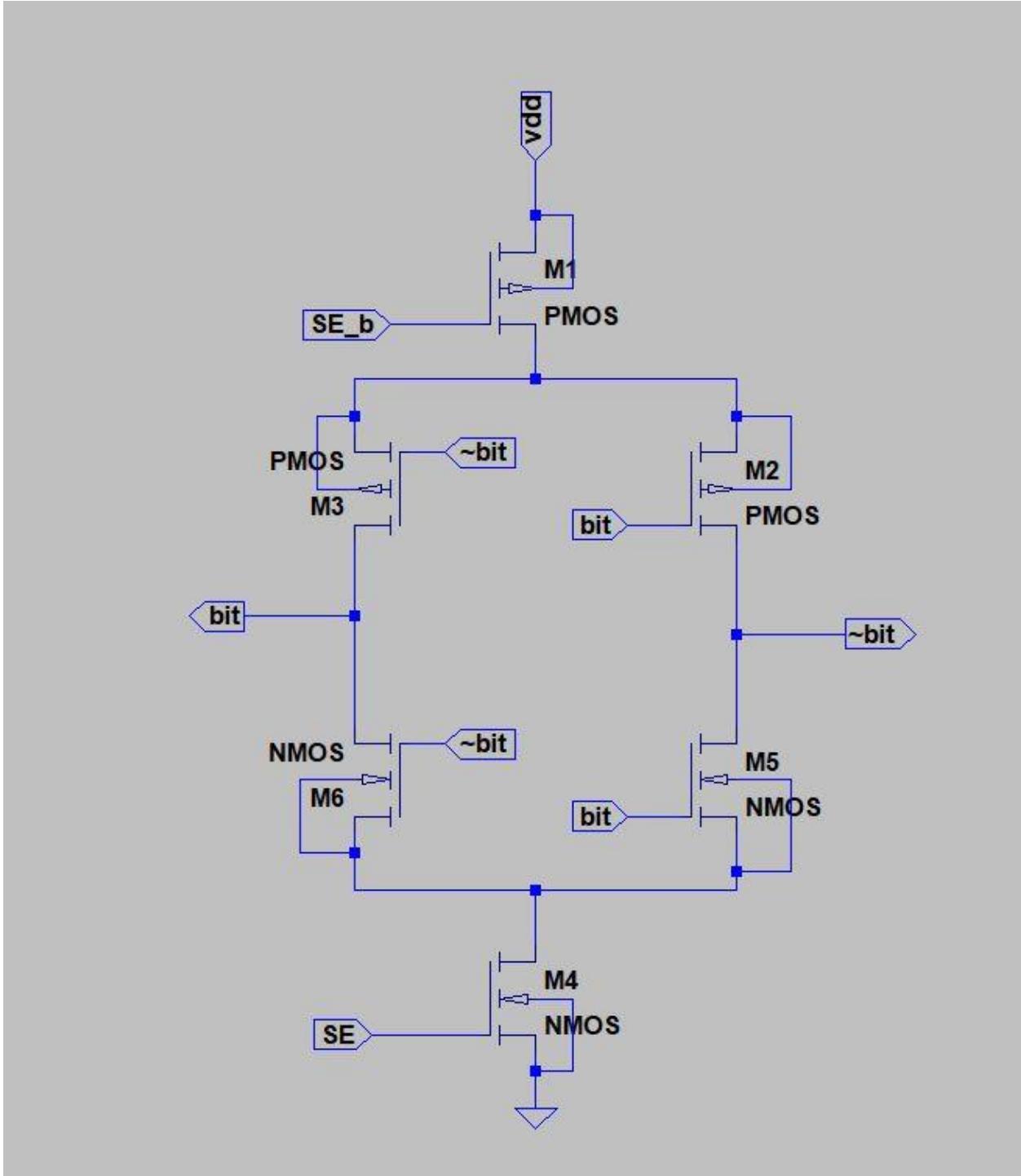


## ● SRAM

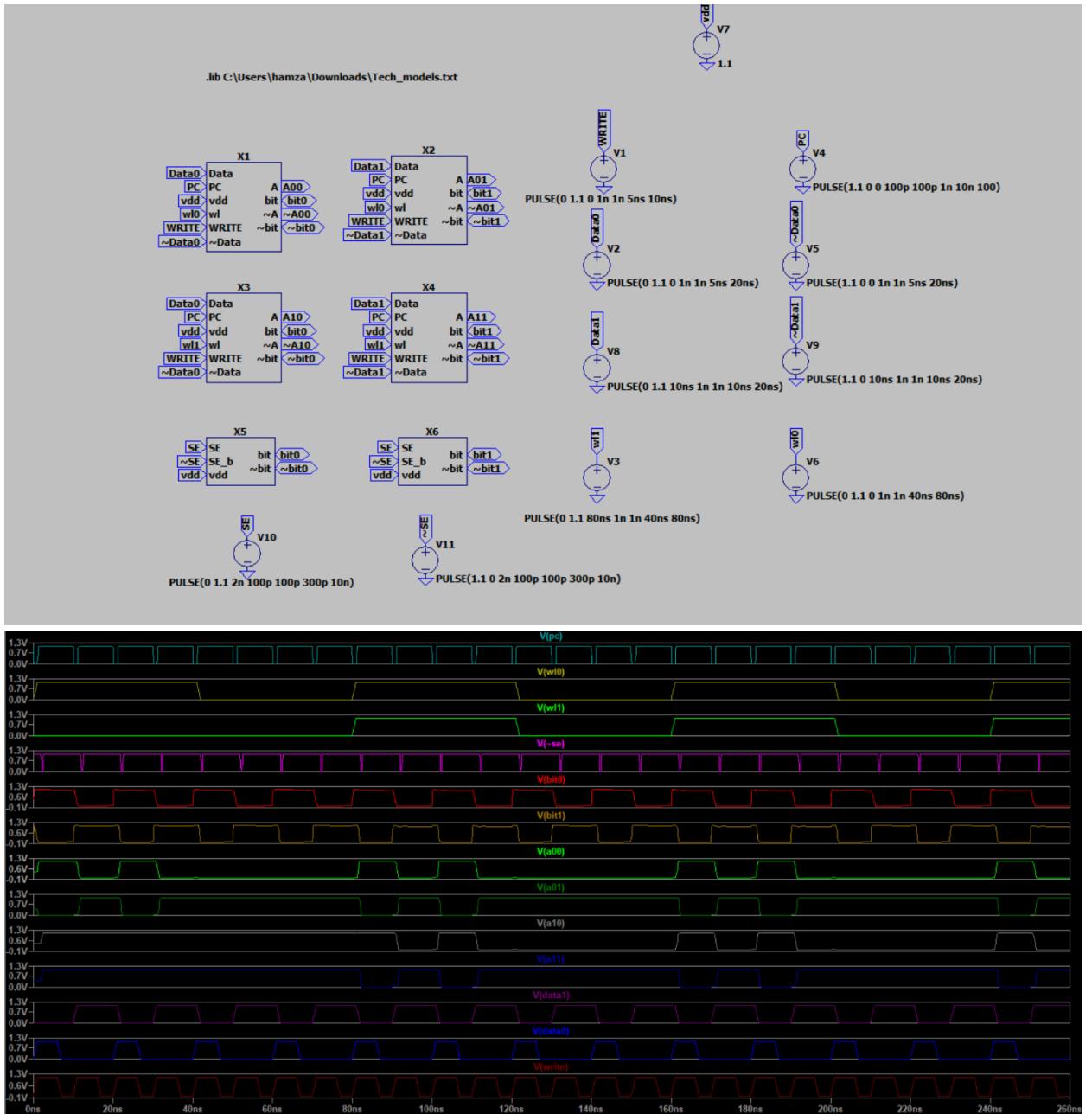
### -Cell



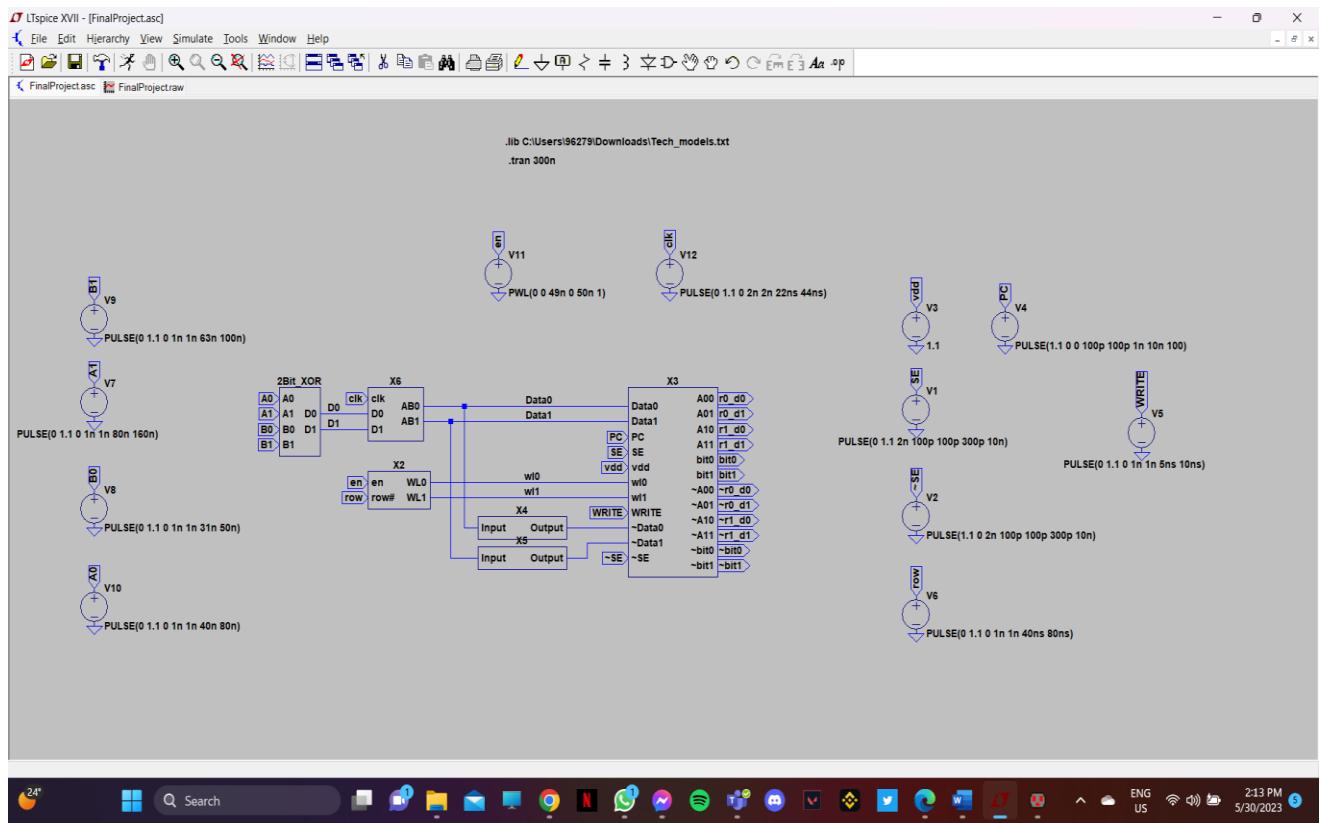
-SE

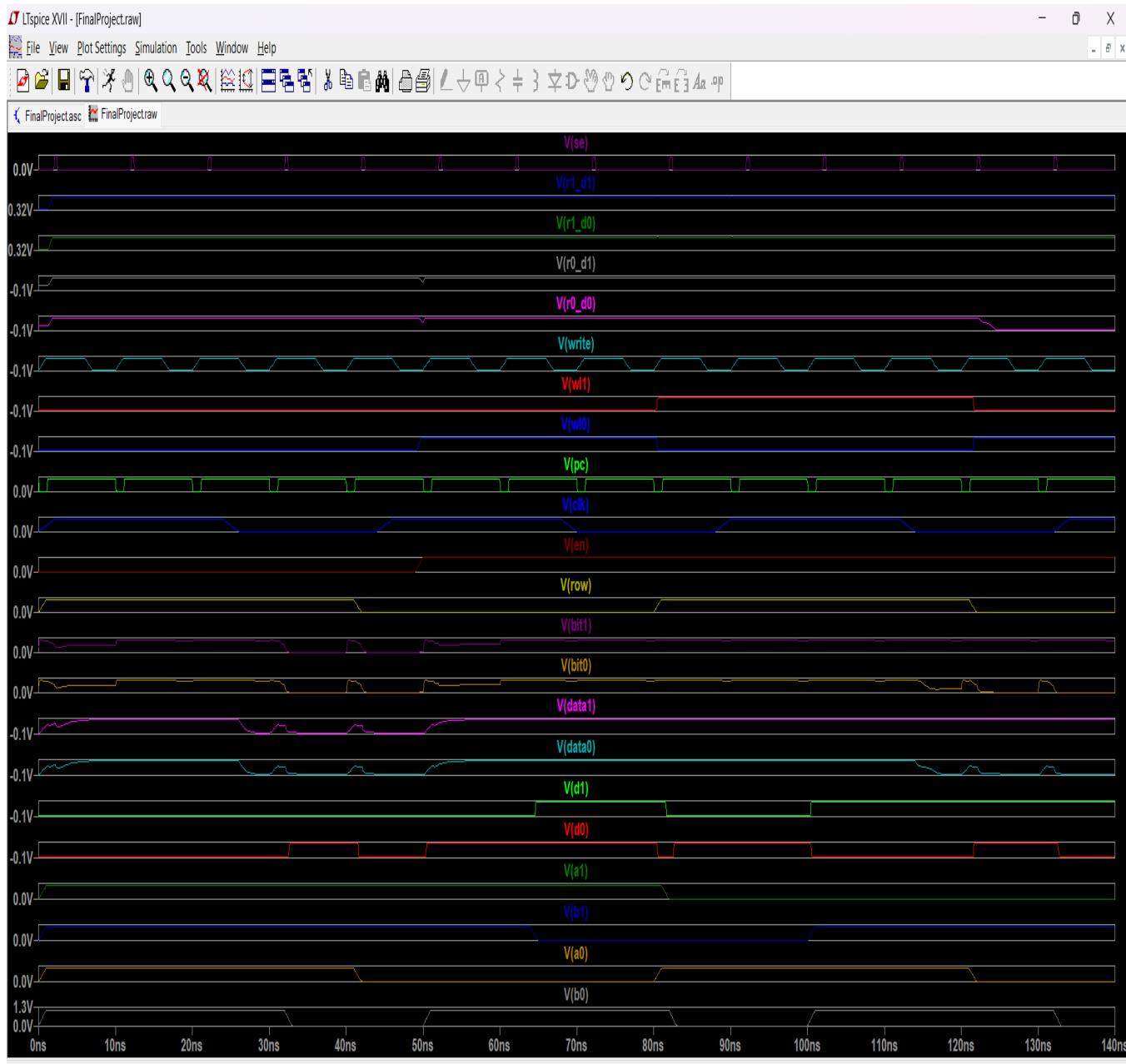


## -2x2 SRAM



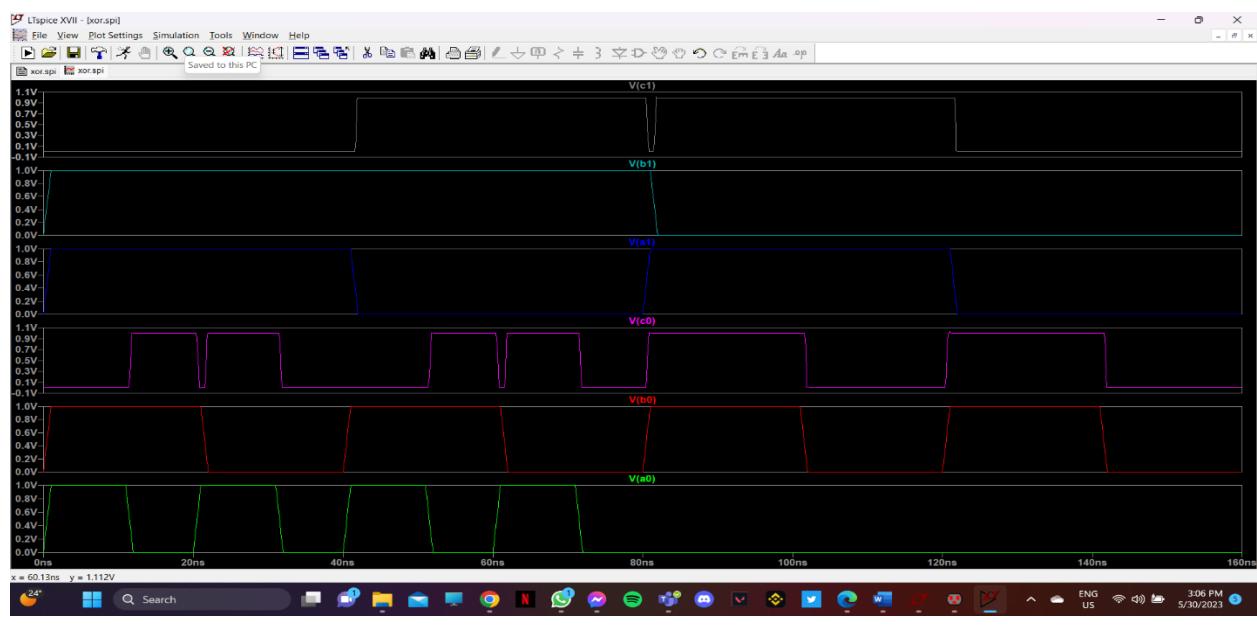
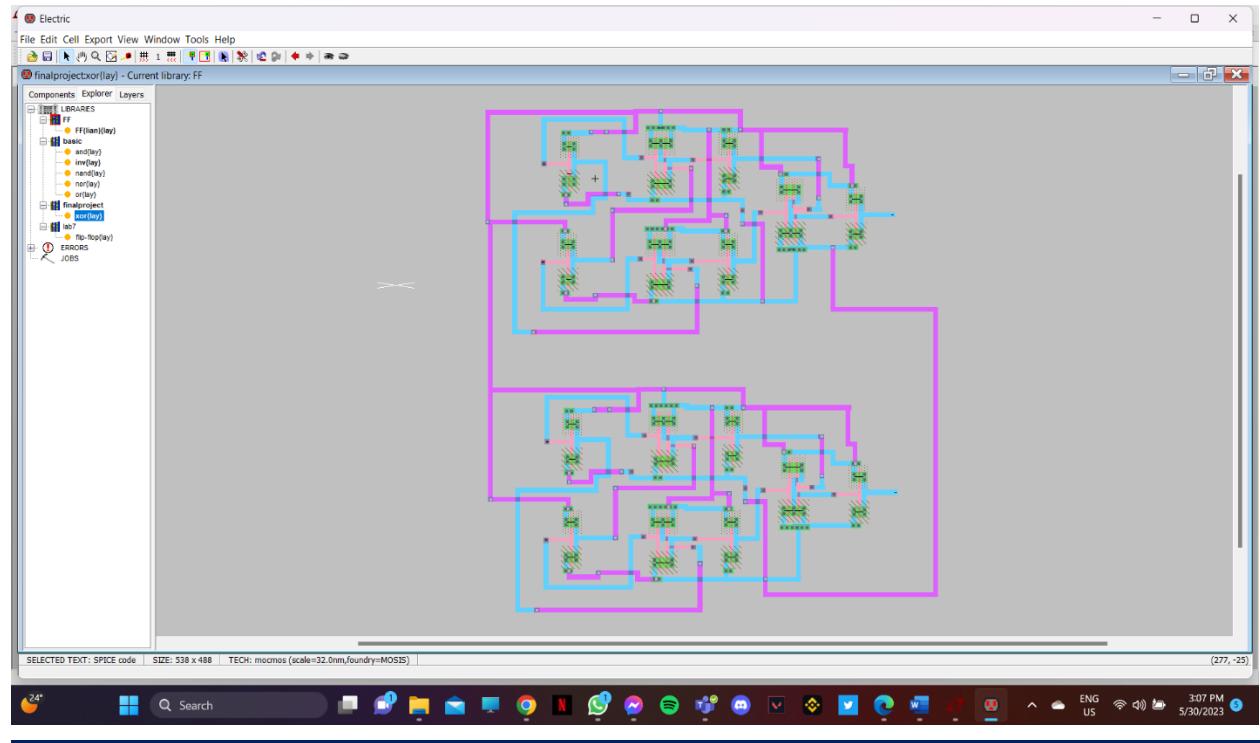
# -Full project



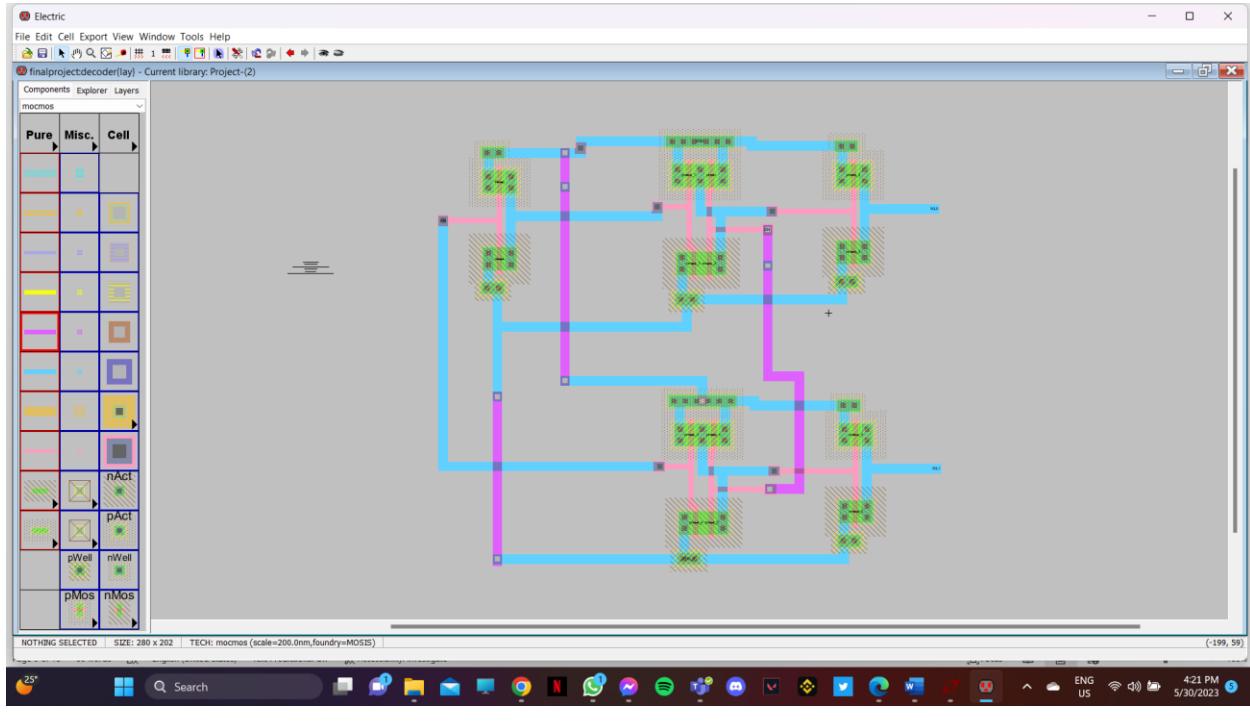


# Layout

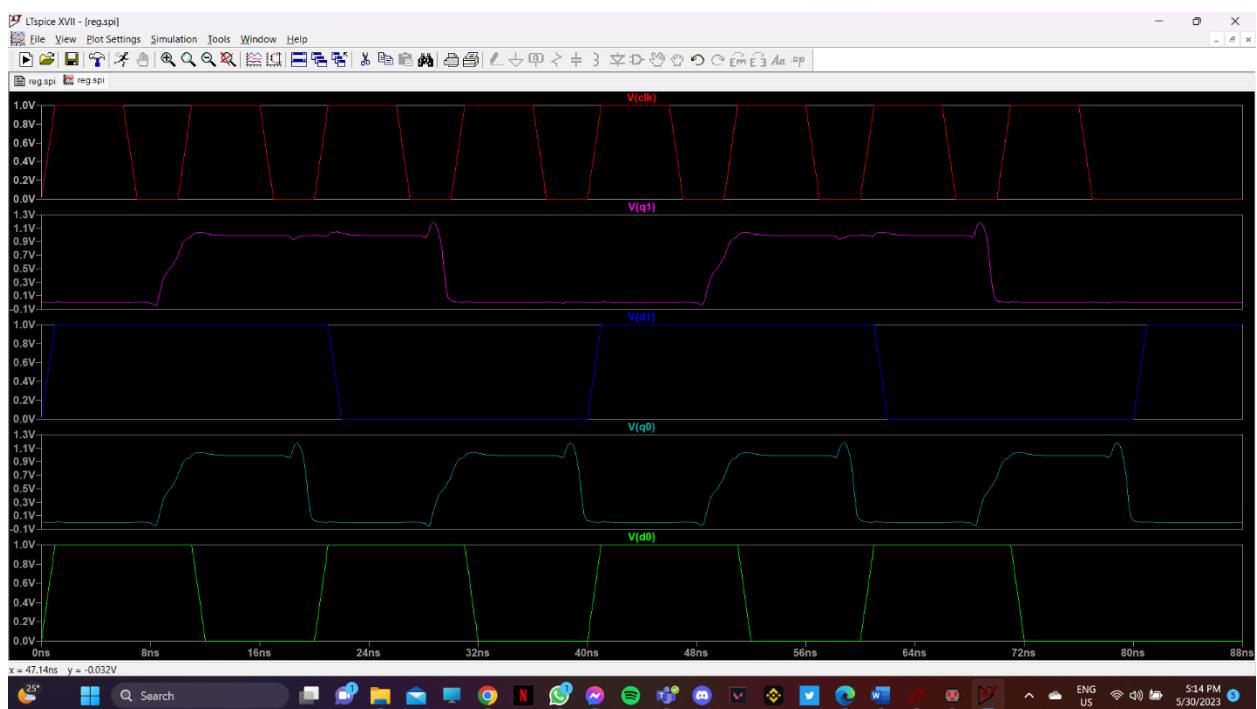
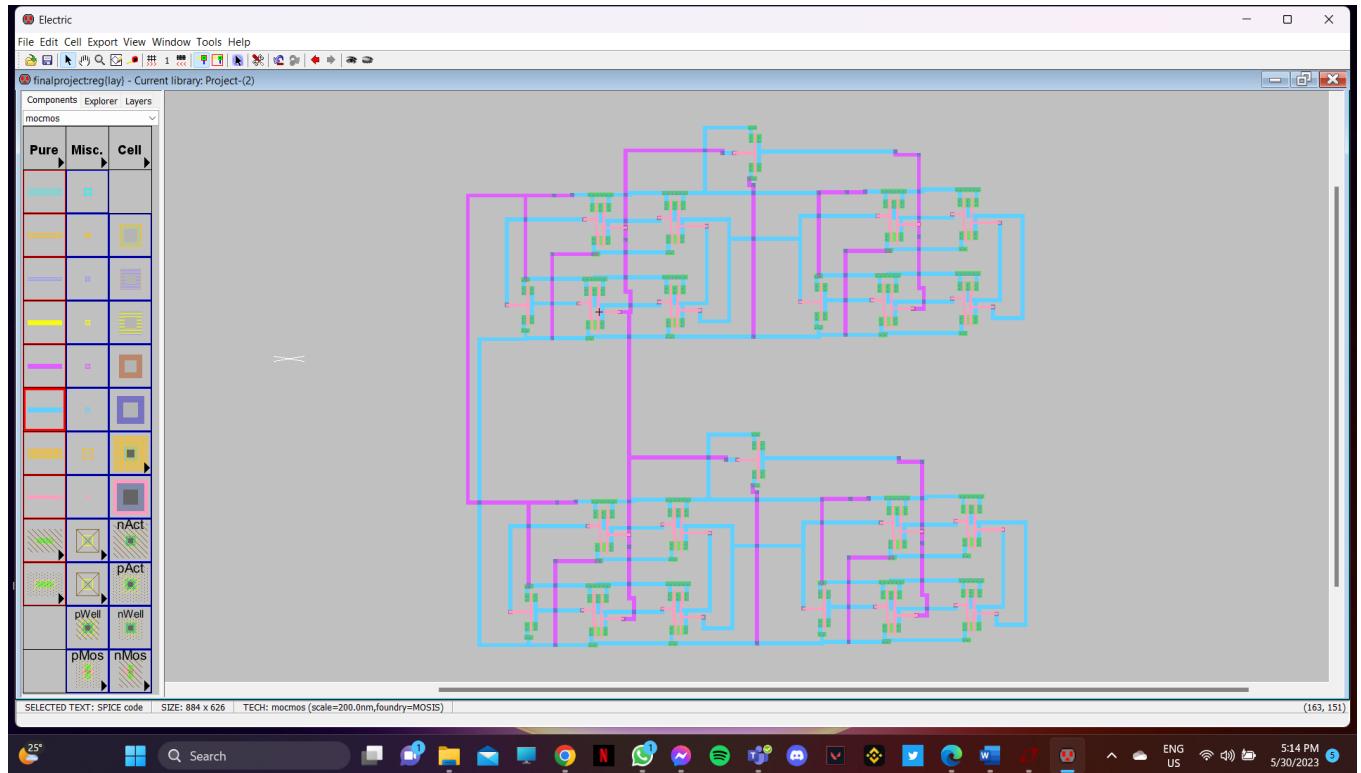
## • 2 bit XOR Gate



# Decoder:

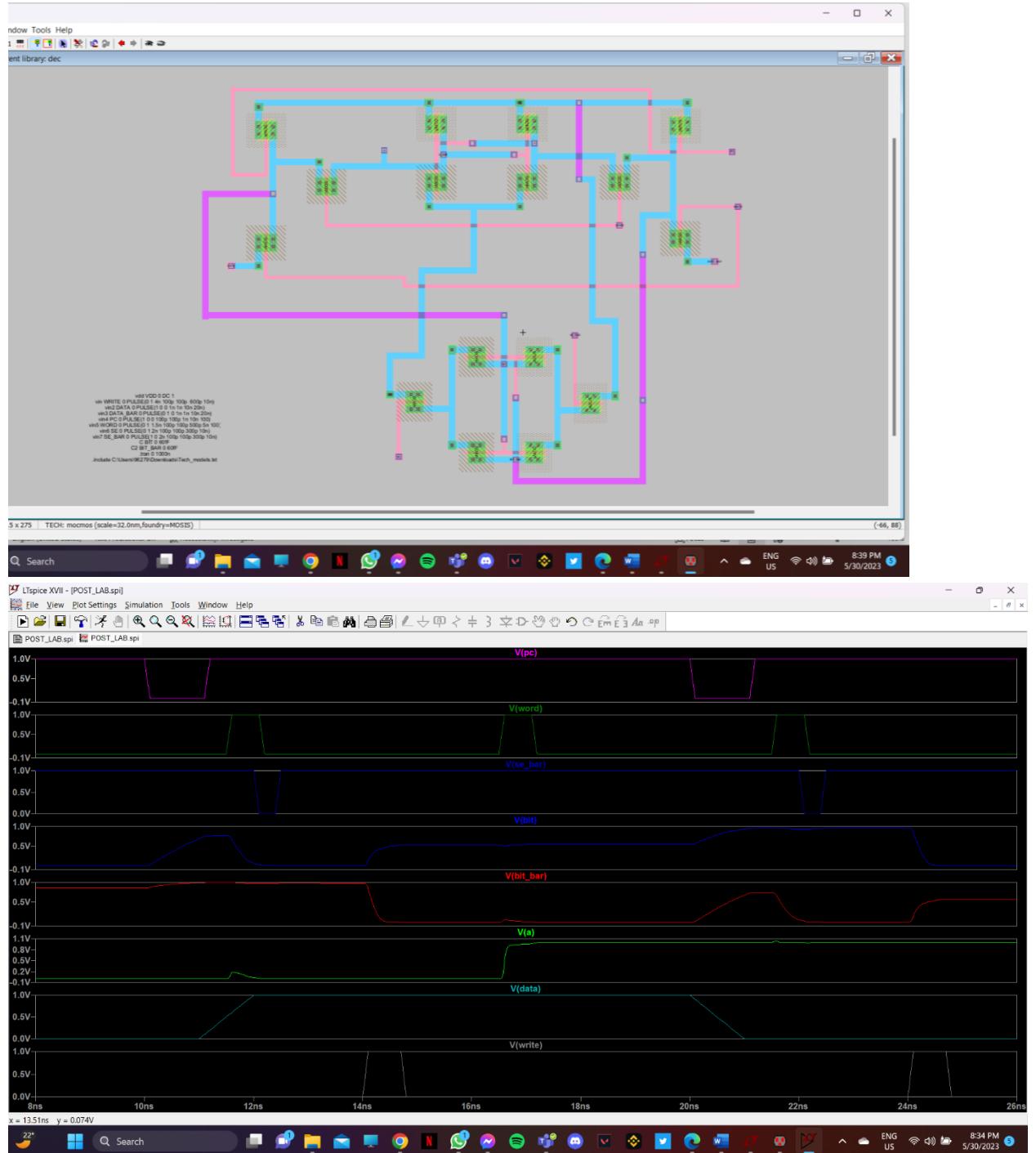


# Register:

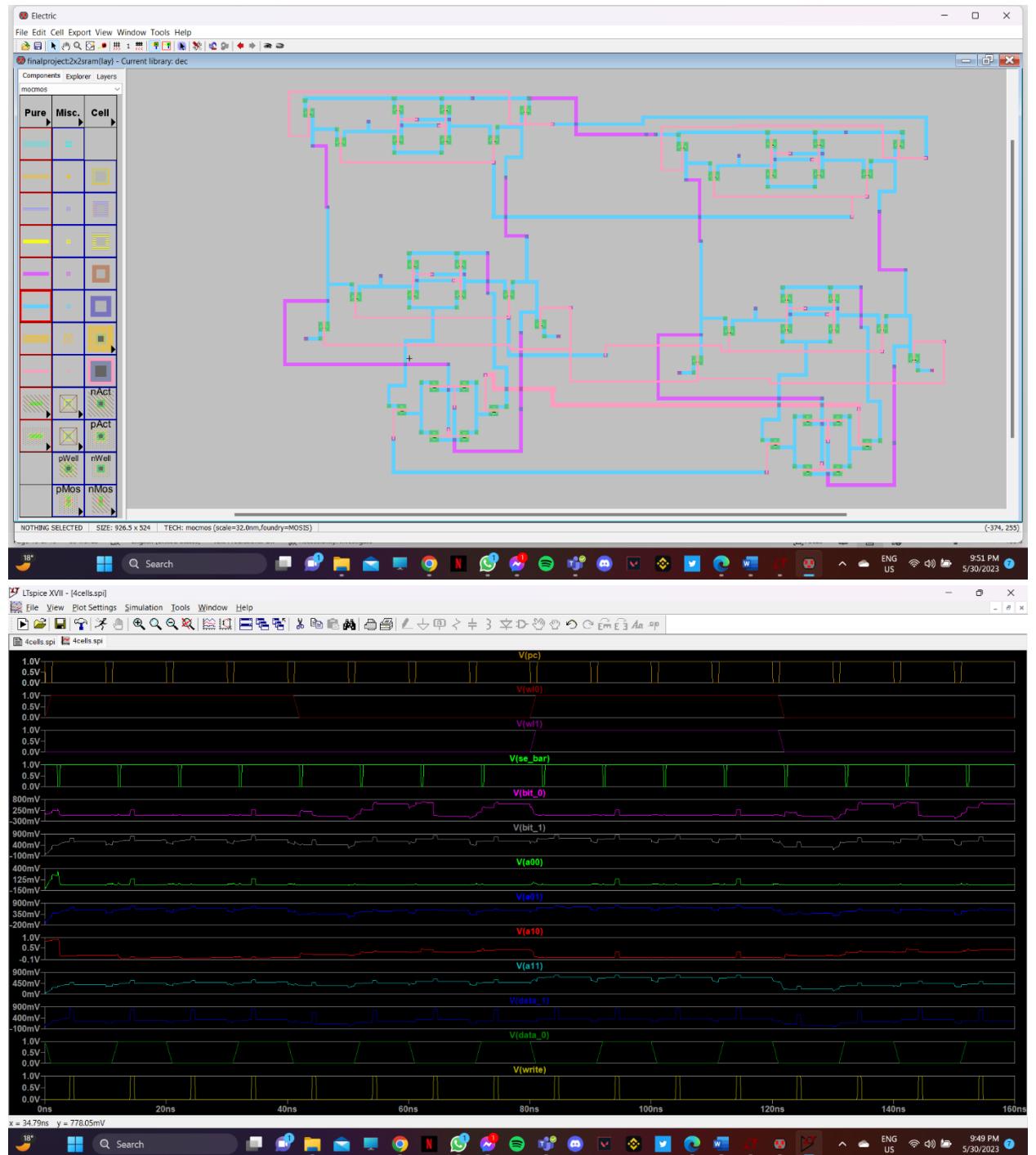


# SRAM:

-Cell



## -2x2Cell



# Full design:

