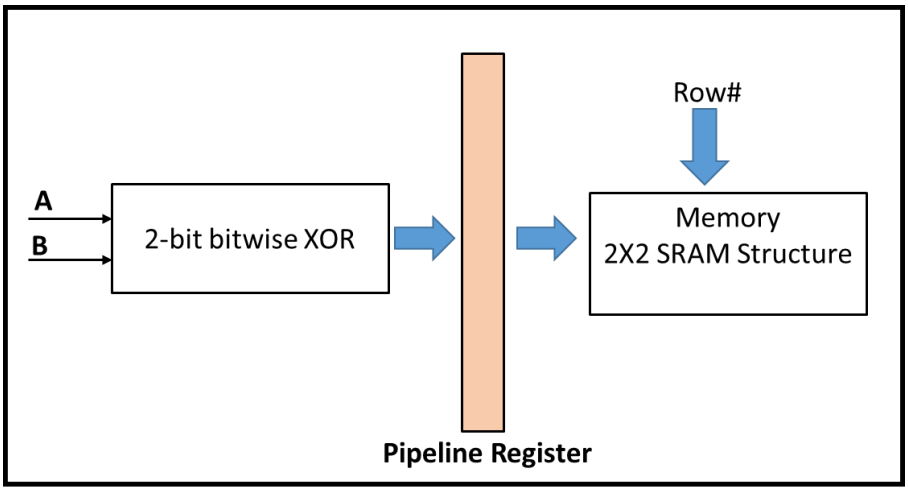
Digital Electronics Lab (CPE 462)

Project

Due Date (30/5/2023)

In this project you are required to make a comprehensive design that contains Memory cells, Flip Flops and Combinational Circuits. The required design is a two stage pipeline shown below and the technical details are as follows:

1- A and B are 2-bit variables defined by the user
2- Row# is a one-bit variable that defines in which row the result will be stored
3- The result should be stored in the mem



In this project you have to:

1- Design all the blocks in the design at the schematic level
2- Integrate the blocks and verify its functionality
3- Design all the blocks in the design at the layout level
4- Integrate the blocks and verify its functionality.
5- You have to submit a report that contains the screenshots and the output waveforms for all the buildings blocks
6- After the deadline time slot will be assigned to each group to discuss their project.

- Submission Rules
  - **Students can work in teams of 2.**
  - **Cheating will result in automatic Zero.**
  - **Late submissions are not allowed.**