

EDUCATION

M.S. in Electronics, SJTU	GPA: Overall 3.59/4.0; Major 3.71/4.0	09/2013-03/2016
B.S. in Microelectronics, SJTU	GPA: Overall 3.65/4.0; Major 3.76/4.0	09/2009-06/2013
B.S. in Applied Physics (minor), SJTU	GPA: Overall 3.81/4.0	02/2011-06/2013

PUBLICATIONS

- [1] Shuwen Deng, **Hanbin Hu**, and Guoyong Shi, "[A Symbolic Sensitivity Method for Mismatch Analysis and CMRR Improvement](#)," in *Proc. IEEE Int'l Symposium on Circuits and Systems (ISCAS)*, 2016, submitted.
- [2] **Hanbin Hu**, Guoyong Shi, Andy Tai, and Frank Lee, "[Topological Symbolic Simplification for Analog Design](#)," in *Proc. IEEE Int'l Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 2644-2647.
- [3] **Hanbin Hu**, Guoyong Shi, and Yan Zhu, "[Incremental Symbolic Construction for Topological Modeling of Analog Circuits](#)," in *Proc. IEEE Int'l Conf. on ASIC (ASICON)*, 2013, pp. 1-4.

RESEARCH EXPERIENCE

Advisor: **Professor Guoyong Shi**, Shanghai Jiao Tong University, China

Automatic Generation of Low-Order Models for Analog Circuit Analysis 06/2015-Present

- Working on automatic operational amplifier modeling considering common mode rejection ratio (CMRR), power supply rejection ratio (PSRR) and slew-settling behavior.
- Applying current limiting techniques to emulate the slew-settling behavior, and analyzing the effectiveness of using different nonlinear functions to exert current limiting on each circuit element.

[Symbolic Sensitivity Method for Mismatch Analysis and CMRR Improvement \[1\]](#) 03/2015-10/2015

- Proved the symbolic construction condition for multiport analysis in Graph-Pair Decision Diagram (GPDD) based on Binary Decision Diagram (BDD).
- Reduced memory consumption for the GPDD structure by 50% on average and shortened the symbolic construction time by 3-4 times, using a multi-port symbolic construction approach.
- Applied symbolic sensitivity computation to recognize most sensitive circuit elements to mismatch, instead of using the time-consuming Monte-Carlo analysis.
- Optimized CMRR performance by means of sensitivity observation of peripheral capacitors, and reduced the mismatch due to parasitic elements in an operational amplifier.

[SPICE Simulation Engine Design](#) 07/2014-11/2014

- Developed a SPICE simulation engine to analyze a circuit netlist whose sub-circuits contain both linear devices such as resistors and capacitors as well as nonlinear devices such as MOSFETs represented by EKV device model.
- Built a compiler processing circuit netlist that includes sub-circuits and device models using Flex/Bison.
- Performed operational point analysis, transient analysis and small signal analysis of analog circuits with various numerical algorithms including Backward Euler and Newton-Raphson Iteration.

[Symbolic Topological Simplification Algorithm for Analog Circuits \[2\]](#) 03/2014-06/2014

- Proposed a topological symbolic simplification algorithm for analog circuits by automatically providing an interpretable simplified circuit topology for operational amplifier analysis; validated and experimented on a symbolic simulation engine.
- Obtained matching topologies automatically, compared to methods given in classical analog circuit textbooks, cut down nearly 80% symbols in original circuits.

[Incremental Symbolic Construction for Analog Circuit Topological Modeling \[3\]](#) 10/2012-06/2013

- Developed a GPDD simulation engine to symbolically compute small-signal transfer function.
- Implemented an efficient symbolic modification algorithm for GPDD based on symbol limit value when adjusting the circuit topology.
- Proposed symbol reordering and novel sign reduction algorithms to significantly reduce memory consumption of the BDD structure by about 40% in the experiment.

Advisor: **Professor Mohamad Sawan**, Polytechnique Montréal, Canada

[Low Voltage Low Power Sigma-Delta Modulator Design](#) 07/2013-08/2013

- Designed a bulk-driven fully differential operational amplifier, working under 1.0V power supply and 245nA current, with an open loop gain of 73dB and a GBW of 226.6kHz.
- Built a first-order Sigma-Delta Modulator (SDM) with an OSR of 20 and an SNR of 22.5dB, integrated a low power track and latch comparator with 39nA current.

INTERNSHIP EXPERIENCE

Summer Internship at Synopsys, Shanghai 07/2015-09/2015

- ♦ Contributed codes to the commercial product HSPICE, and passed all regression tests according to the report from the Quality Assurance team.
- ♦ Refactored 3 commands input routines from Fortran to C++.
- ♦ Reconstructed the simulation engine for transfer function simulation in HSPICE.
- ♦ Detected and fixed 6 bugs in HSPICE, such as malfunction in appearance of multiple specific commands, disunity in manual description, misalignment in output format, etc.
- ♦ Invited to present the project on FY16 Synopsys Greater China R&D Demo Day.

Summer Internship at Synopsys, Shanghai 07/2014-09/2014

- ♦ Built a Perl script to gather netlist information, such as the number of elements, for database construction from the entire test suite with 20,586 test cases in quality assurance system.
- ♦ Detected 5 bugs in HSPICE and HSP_PACK2GO, such as several file path errors, etc.

Teaching Assistant on Introduction to Design Automation 03/2014-06/2014

- ♦ Graded homework and held office hours to answer questions from students.
- ♦ Provided a fundamental compiler template for the course project.
- ♦ Held final project presentations and assessed students' performance.

SELECTED EXTRA-CURRICULAR ACTIVITIES

Manager , Irving T. Ho Fellows Google Group, Irving T. Ho Memorial Foundation	01/2012-Present
Class Commissary , Academy Affairs, School of Microelectronics (SoME), SJTU	09/2013-Present
Point Contact , Bai-I Elementary School, Irving T. Ho Memorial Foundation	01/2014-06/2014
Volunteer , Shanghai Science Museum, Shanghai	11/2013
Vice Minister , Academic Department, Student Union of SoME, SJTU	09/2010-06/2011
Member , Summer Social Practice: Survey of Mental Health Status of Volunteers in EXPO; Awarded with Third Prize by SJTU	07/2010-09/2010
Secretary , Academic Department, Student Union of SoME, SJTU	09/2009-06/2010

SELECTED HONORS & AWARDS

Guanghua Scholarship	Top 5%	09/2014-06/2015
SanDisk Scholarship	Top 3%	09/2013-06/2014
Merit Student Award	Top 10%	09/2013-06/2014
Irving T. Ho Memorial Scholarship	Top 3%	09/2010-06/2011
Academic Excellence Scholarship Second-class (3 years)	Top 10%	09/2009-06/2012
Second Prize, National Olympiad in Informatics in Provinces		12/2008
Second Prize, Intel Shanghai Adolescents Science & Technology Innovation Fair		03/2008

SELECTED COURSES (* in Applied Physics)

<i>Mixed-Signal Design Automation Methods</i>	A+	<i>Circuit Design for Biomedical Implants</i>	A
<i>Introduction to Design Automation</i>	96	<i>Signals and Systems</i>	99
<i>Analog Integrated Circuits</i>	94	<i>Artificial Intelligence</i>	97
<i>Electromagnetic Field</i>	95	<i>Introduction to RF IC Design</i>	95
<i>Semiconductor Physics *</i>	100	<i>Theory and Technology of Laser *</i>	96
<i>Introduction to Solid State Physics *</i>	98	<i>Fundamental of Modern Physics *</i>	90

MOOC COURSES IN COURSERA

<i>Algorithms: Design and Analysis, Part I</i>	Prof. Tim Roughgarden, Stanford	06/2015-09/2015
<i>VLSI CAD: Logic to Layout</i>	Prof. Rob A. Rutenbar, UIUC	02/2015-04/2015
<i>Machine Learning</i>	Prof. Andrew Ng, Stanford	07/2014-09/2014

COMPUTER SKILLS

Programming	C/C++, Perl, Python, MATLAB/Simulink, Qt, Flex/Bison, Fortran, Verilog HDL
Software	Synopsys HSPICE, Cadence Spectre, Virtuoso and OrCAD, LTC LTspice
Skills	Git, Vim, Doxygen, Gnuplot, Linux, MS Office