Hanbin Hu

CONTACT INFORMATION
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EDUCATION

Texas A&M University, College Station, Texas, U.S.
Ph.D., Computer Engineering — Aug. 2016 - Dec. 2020 (Expected)
- Advisor: Prof. Peng Li
- Overall GPA: 4.0/4.0

Shanghai Jiao Tong University, Shanghai, China
M.S., Electronic Science and Technology — Sept. 2013 - Mar. 2016
- Overall GPA: 3.59/4.0; Major GPA: 3.71/4.0

Shanghai Jiao Tong University, Shanghai, China
B.S., Microelectronics (Major) and Applied Physics (Minor) — Sept.2009 - Jul. 2013
- Overall GPA: 3.65/4.0; Major GPA: 3.76/4.0; Minor GPA: 3.81/4.0

RESEARCH EXPERIENCE

Research Assistant, *Computer Engineering & Systems Group* — Aug. 2016 - Present
Advisor: Prof. Peng Li, Texas A&M University
- Working on efficient verification techniques for Analog & Mixed-Signal (AMS) circuit with **extremely high reliability requirements** in **safety-critical systems**.
- Utilized **machine-learning-based** and **formal verification** techniques to achieve efficient and accurate extremely-rare failure detection, and got a paper published in *DAC 2018*.
- Applied Bayesian optimization based on Gaussian process to **efficient** rare failure detection with **limited simulation budget** in **high-dimension space**, and got two papers published in *ICCAD 2018* and *DAC 2019*.
- Developing robust statistical and deep learning techniques for assessment and verification of **machine learning model robustness** to enable **trustworthy ML-driven EDA**.
- Engaging with industrial verification engineers from *Texas Instruments*, *Intel*, and *IBM*.

Research Assistant, *Mixed-Signal Design Automation Lab* — Sept. 2013 - Mar. 2016
Advisor: Prof. Guoyong Shi, Shanghai Jiao Tong University
- Conducted research on symbolic simulation methods and model order reduction for insightful analog circuit modeling.
- Built the circuit simulation library for lab usage using Binary Decision Diagram (BDD).
- Completed first industrial research projects in the lab with *TE Connectivity Ltd.*
- Published one journal paper in *TODAES 2017*, and two conference papers in *ISCAS 2015* and *ASICON 2013*, respectively.

PUBLICATIONS

[C1] **Hanbin Hu**, Peng Li and Jianhua Z. Huang, "Enabling High-Dimensional Bayesian Optimization for Efficient Failure Detection of Analog and Mixed-Signal Circuits", *Proceedings of the Annual 56th Design Automation Conference (DAC '19)*, 2019, accepted.

[C2] **Hanbin Hu**, Peng Li and Jianhua Z. Huang, "Parallelizable Bayesian Optimization for Analog and Mixed-Signal Rare Failure Detection in High Coverage", *Proceedings of the 37th International Conference on Computer-Aided Design (ICCAD '18)*, 2018, no. 98, pp. 1-8, (**Best Paper Award Nomination**).

[C3] **Hanbin Hu**, Qingran Zheng, Ya Wang and Peng Li, "HFMV: Hybridizing Formal Methods and Machine Learning for Verfication of Analog and Mixed-Signal Circuits", *Proceedings of the Annual 55th Design Automation Conference (DAC '18)*, 2018, no. 95, pp. 1-6.

[C4] **Hanbin Hu**, Guoyong Shi, Andy Tai, and Frank Lee, "Topological Symbolic Simplifi-cation for Analog Design," *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 2644-2647.

[C5] **Hanbin Hu**, Guoyong Shi, and Yan Zhu, "Incremental Symbolic Construction for Topological Modeling of Analog Circuits," *2013 IEEE 10th International Conference on ASIC (ASICON)*, 2013, pp. 1-4.

[J1] Guoyong Shi, **Hanbin Hu**, and Shuwen Deng, "Topological Approach to Automatic Symbolic Macromodel Generation for Analog Integrated Circuits," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 22, no. 3, pp. 1-25, 2017.

Awards

Paper Award

- IEEE/ACM William J. Mccalla ICCAD Best Paper Award Nomination (6/398) Oct. 2018

Industrial Award

- Best Internship Project Award, Synopsys, Shanghai (Best 2 in Shanghai site) Oct. 2015

Student Awards — Shanghai Jiao Tong University, Graduate Program

- Distinguished Master Graduate from SJTU (Top 10%) Mar. 2016
- 3rd. Prize for the Best Thesis in the Department (Top 15%) Mar. 2016
- Kwang-Hua Scholarship (Top 5%) 2015 - 2016
- SanDisk Scholarship (Top 3%) 2014 - 2015
- Merit Student Award (Top 10%) Oct. 2014

Student Awards — Shanghai Jiao Tong University, Undergraduate Program

- Irving T. Ho Memorial Scholarship (Top 3%) 2011 - 2012
- Second-class Academic Excellence Scholarship (3 times) (Top 10%) 2010 - 2013

Competition Awards — Shanghai Yan'an High School

- Second Prize, National Olympiad in Informatics in Provinces Dec. 2008
- Second Prize, Intel Shanghai Adolescents Science & Technology Innovation Fair Mar. 2008

Work Experience

Graduate Intern, *Cadence Design Systems*, San Jose, CA May 2018 - Aug. 2018
Circuit Simulation, Custom and PCB Design Group

- Optimized the sparse matrix solver in commercial Spectre simulator for S-parameter analysis.
- Utilized memory sharing and parallelization using OpenMP to accelerate the matrix solving procedure in C++.
- Achieved around 50x speedup for forward and backward substitution and 2x overall speedup for hundreds of right-hand-side vectors and large sparse matrix with millions of non-zero elements.

Software Engineer Intern, *Synopsys*, Shanghai Jul. 2015 - Sept. 2015
R&D Department, HSPICE, Analog & Mixed-Signal Group

- Refactored 3 commands input routines in HSPICE parser from Fortran to C++.
- Reconstructed the simulation engine for transfer function simulation in HSPICE.
- Revealed and fixed 6 bugs in commercial simulation tool HSPICE.
- Invited as one of the 2 best internship projects at Shanghai site on FY16 Synopsys Greater China R&D Demo Day.

Quality Assurance Engineer Intern, *Synopsys*, Shanghai Jul. 2014 - Sept. 2014
Quality Assurance Department, HSPICE, Analog & Mixed-Signal Group

- Built Perl scripts to gather netlist information for database construction from 20,586 test cases in quality assurance system.
- Analyzed 674 test cases to recognize corresponding circuit types by manual analysis.
- Detected 5 bugs in HSPICE and HSP_PACK2GO.

Teaching Experience

Teaching Assistant, *Shanghai Jiao Tong University*, Shanghai Mar. 2014 - May 2014
Course: *Introduction to Design Automation*
Instructor: Prof. Guoyong Shi, Department of Micro-Nano Electronics

- Provided a fundamental compiler template for the course project.
- Organized final project presentations and assessed students' performance.
- Graded homework and held office hours to answer questions from students.

Selected Course Projects

Computational Methods for Integrated System Design, TAMU Jan. 2017 - May 2017

- Implemented a SPICE simulator for DC, AC and transient simulation of AMS circuits.
- Utilized adversarial samples to attack well trained neural networks reducing the classification accuracy from 98.49% to 4.51%.

Parallel Distributed Numerical Algorithms, TAMU Aug. 2017 - Dec. 2017

- Implemented LU factorization and triangular system inversion with OpenMP, obtain a 2.12x speedup with 4 cores and a 8.34x speedup with 20 cores, respectively.
- Achieved a 7.60x speedup for Gaussian process regression with CUDA using Cholesky decomposition on a high performance computing (HPC) system.

Introduction to Hardware Verification, TAMU Jan. 2017 - May 2017

- Implemented a UVM verification framework for a multi-core MESI-based cache design.
- Revealed and fixed 22 bugs in the design under verification.
- Documented the verification plan with *vManager* and *vPlanner*.

Skills

Computer Programming

C/C++, Python, Perl, Linux, MATLAB, Git, OpenMP, MPI, CUDA, LaTeX, R, Flex/Bison, Qt, HTML & CSS, Pascal, Visual Basic, Fortran

Machine Learning

Bayesian inference, Gaussian process, Bayesian optimization, Deep learning, Statistical sampling, Adversarial attack, Ensemble methods, PyTorch, TensorFlow

Circuit Simulation and Verification

Synopsys HSPICE, Cadence Spectre, Virtuoso, SystemVerilog, UVM, Verilog HDL