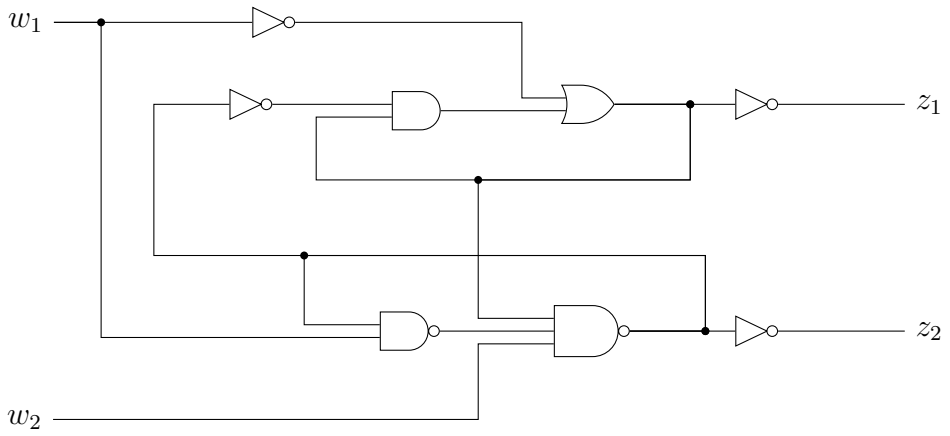
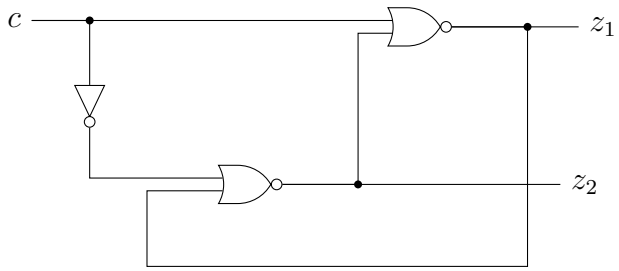
ECE 124 digital circuits and systems
Assignment #10

Q1: Consider the asynchronous circuit shown below. Derive the transition table and flow table for the circuit. Remember to circle stable states.



Q2: Consider the asychronous circuit shown below. Derive a transition table and flow table for the circuit. Draw waveforms for signals c, z_1 and z_2 assuming that c is a square wave clock signal and that each gate has a propagation delay of Δ units of time.

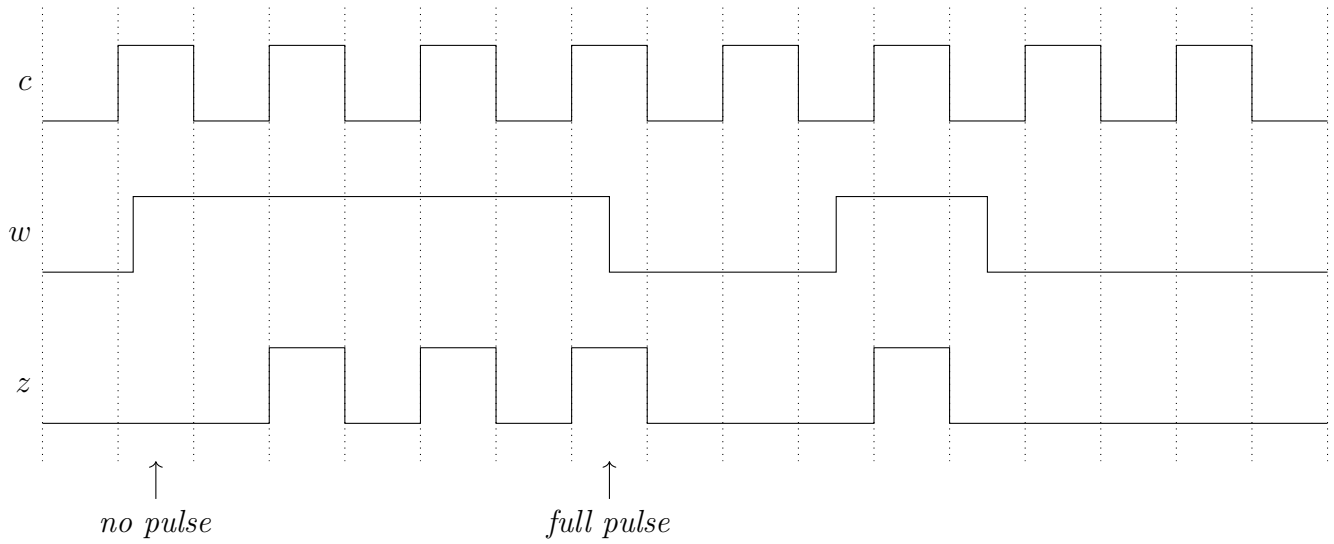


Q3: An asynchronous sequential circuit with two inputs x_1 and x_2 and one output z is described by the following equations and output functions: $Y = x_1x_2' + (x_1 + x_2')y$ and $z = y$. Here, Y's represent the excitation variables (next state variables) and y's represent the secondary variables (current state variables).

Draw the logic diagram of the circuit. Derive the transition table and flow table for the circuit.

Q4: A control mechanism for a vending machine accepts nickels and dimes. It dispenses merchandise when 20 cents is deposited; it does not give change if more than 20 cents is deposited. Design a state diagram assuming that the control mechanism will be implemented via an asynchronous sequential circuit (the state diagram might have a large number of states). When deriving your state diagram, assume that the circuit operates in fundamental mode (only one input changes at a time).

Q5: Assume that you are to design an asynchronous sequential circuit with the following specifications. The circuit has two inputs c and w. The input c is a series of pulses. The output z replicates the input c when $w = 1$, otherwise $z = 0$. The pulses on z must be full pulses. That is, if $c = 1$ when w changes from $0 \rightarrow 1$, then the circuit will not produce a partial pulse on z but will wait until the next pulse to generate $z = 1$. If $c = 1$ when w changes from $1 \rightarrow 0$, then a full pulse must be generated. The desired operation is illustrated below.



Derive a primitive flow table for this problem assuming fundamental mode operation. Perform state minimization to obtain a reduced flow table. Finally, perform state assignment and derive a circuit.

Q6: Obtain a state diagram and a primitive flow table for an asynchronous sequential circuit with two inputs x_1 and x_2, and two outputs z_1 and z_2. The circuit must have the following behaviour:

(a) When $x_1x_2 = 00$, the output is $z_1z_2 = 00$;

(b) When $x_1 = 1$ and x_2 changes from $0 \rightarrow 1$, the output is $z_1z_2 = 01$;

(c) When $x_2 = 1$ and x_1 changes from $0 \rightarrow 1$, the output is $z_1z_2 = 10$;

(d) Otherwise, then output does not change.

Q7: Consider an asynchronous sequential circuit with two inputs x_1 and x_2, and one output z. Initially, both inputs are equal to 0. When either x_1 or x_2 becomes 1, the output z becomes 1. When the other input becomes 1, the output z changes back to 0. The output z remains 0 until both inputs return to 0 and the process repeats itself.

Assume fundamental mode operation. Derive a state diagram and a primitive flow table. Perform state minimization to show that the state table can be reduced to the following flow table.

Current State	Next State $x_1x_2 = 00$	01	11	10	Output (z) $x_1x_2 = 00$	01	11	10
a	$\boxed{a}$	$\boxed{a}$	b	$\boxed{a}$	0	1	-	1
b	a	$\boxed{b}$	$\boxed{b}$	$\boxed{b}$	-	0	0	0

Q8: Find a hazard-free minimum cost SOP implementations for the following functions:

(a) $f(a, b, c, d) = \sum(0, 4, 11, 13, 15) + D(2, 3, 5, 10)$.

(b) $f(a, b, c, d, e) = \sum(0, 4, 5, 24, 25, 29) + D(8, 13, 16, 21)$.

Q9: Finda hazard-free minimum cost POS implementations for the following functions:

(a) $f(a, b, c, d) = \Pi(0, 2, 3, 7, 10) + D(5, 13, 15)$.

(b) $f(a, b, c, d, e) = \Pi(2, 6, 7, 25, 28, 29) + D(0, 8, 9, 10, 11, 21, 24, 26, 27, 30)$.

Q10: Perform state minimization to reduce the following flow table to one with fewer states which exhibits the same functional behaviour.

Current State	Next State $x_1x_2 = 00$	01	11	10	Output z
a	$\boxed{a}$	b	c	-	0
b	k	$\boxed{b}$	-	h	0
c	f	-	$\boxed{c}$	m	0
d	$\boxed{d}$	e	j	-	1
e	a	$\boxed{e}$	-	m	0
f	$\boxed{f}$	l	j	-	0
g	d	$\boxed{g}$	-	h	0
h	-	g	j	$\boxed{h}$	1
j	f	-	$\boxed{j}$	h	0
k	$\boxed{k}$	l	c	-	1
l	a	$\boxed{l}$	-	h	0
m	-	g	c	$\boxed{m}$	1

Q11: Consider the following flow table.

Current State	Next State $x_1x_2 = 00$	01	11	10	Output (z) $x_1x_2 = 00$	01	11	10
a	$\boxed{a}$	b	d	$\boxed{a}$	0	-	1	1
b	c	$\boxed{b}$	$\boxed{b}$	d	0	1	0	0
c	$\boxed{c}$	$\boxed{c}$	b	a	0	1	0	1
d	a	c	$\boxed{d}$	$\boxed{d}$	-	-	1	0

Find a suitable race-free state assignment which

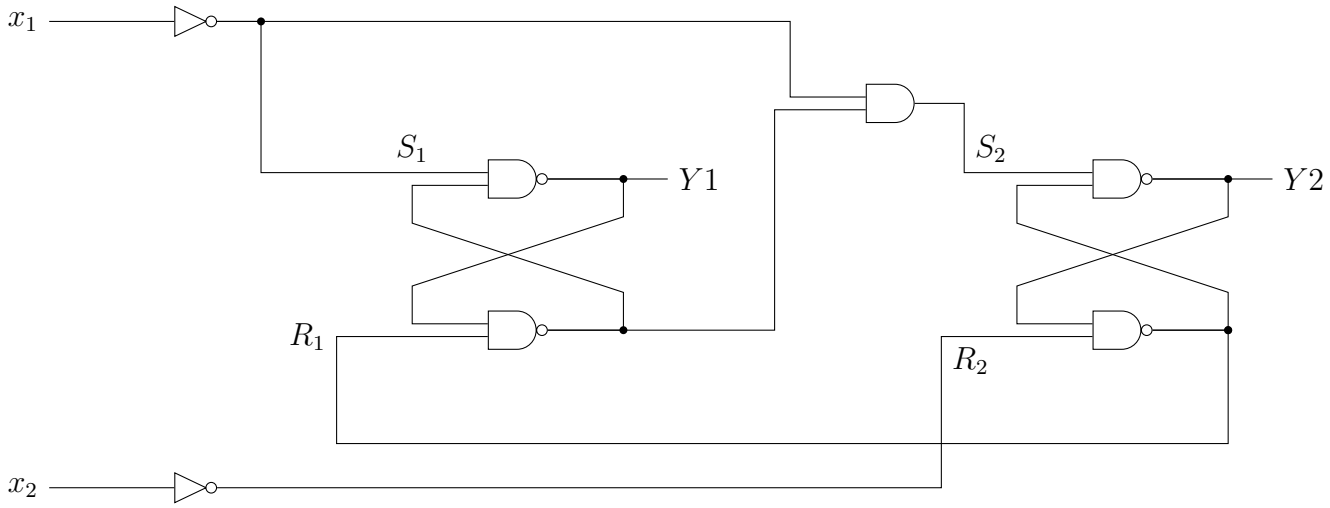
(a) Uses as few states as possible.

(b) Uses the method of state duplication.

(c) Uses the method of one-hot encoding.

Q12: Consider an asynchronous sequential circuit defined by the equations $Y = x_1x_2 + (x_1 + x_2)y$ and $z = y$. Implement this circuit using a NOR SR latch. Implement this circuit using a NAND $S'R'$ latch.

Q13: Consider the circuit shown below which consists of two $S'R'$ latches.



Write down equations for the latch inputs S_1, R_1, S_2 and R_2. Derive equations for the latch outputs Y_1 and Y_2. Derive a transition table for the circuit.