ECE-124 Lab-1 Submission Form – Winter 2018			
GROUP NUMBER:	Lab1 Demo	Lab1 Quiz	**TA:**
SESSION NUMBER:	Out of 5	Out of 5	

I am submitting this report for grading. I certify that this report, including any code, descriptions, flowcharts as part of the submission were written by the team member(s) below and there has not been any use of prior academic credit at this university or any other institution. The penalty for plagiarism or submission without signature(s) will be a grade of zero

NAME: (Print)	**UW User ID (not Student ID)**	**Signature**
Partner A:		
Partner B:		

LAB1 DESIGN DEMO	**Marks Allotted**	**A**	**B**
With BOTH sw[0], sw[1] OFF and using PB[1..0] verify AND, NAND, OR, XOR of schem/VHDL gates driven LEDs	1		
Verify with sw[1] ON, sw[0] OFF that the LED's invert when using the previous step of AND, NAND, OR, XOR	1		
With sw[1] OFF and sw[0] ON verify the LED SEQUENCE on LEDS[3..0] together with LED's[7..4]: 0010, 1110, 1110, 0101	2		
With sw[1] ON and sw[0] ON verify the LED SEQUENCE on LEDS[3..0] together with LED's[7..4]: 1101, 0001, 0001, 1010	1		
LAB1 DEMO MARK	**Out of 5**		

LAB1 QUIZ	**Marks Allotted**	**A**	**B**
Why were inverters added after the PB[1..0] inputs?	1		
Name one typical development process used in an FPGA design.	1		
What are the two main components of a VHDL design file?	1		
What style of coding was used in the Lab1 VHDL Architecture section?	1		
For your Polarity Control block what kind of gate was used?	1		
QUIZ BONUS: For automation we added a counter to the 50 MHz clock input. The highest bits (COUNT[27..26]) of the counter selected to drive the logic block operations. Why?	+1 BONUS		
QUIZ BONUS: What change(s) could make the LED's flash faster?	+1 BONUS		
LAB1 QUIZ MARK	TOTAL (Up to 7) out of 5		