ECE 124 digital circuits and systems
Assignment #6

Q1: Show how a JK flip-flop can be implemented with a T flip-flop and other logic gates.

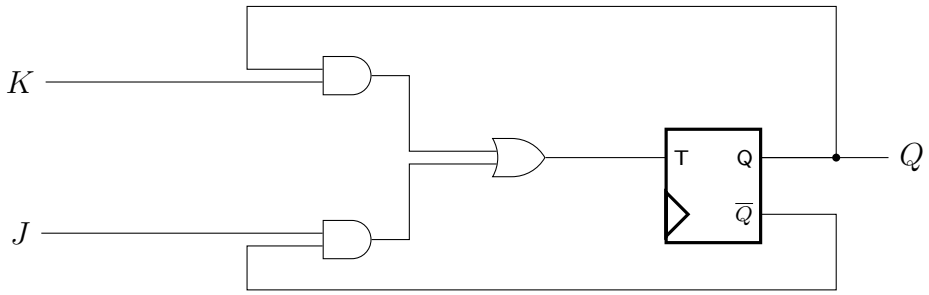
Solution:
Start with the table describing how a $JKFF$ works. Then, find the values for a TFF necessary to get the desired changes — the values for T are found by comparing $Q(t)$ and $Q(t+1)$ for the $JKFF$.

J	K	$Q(t)$	$Q(t+1)$	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Next, write down the equation for T:

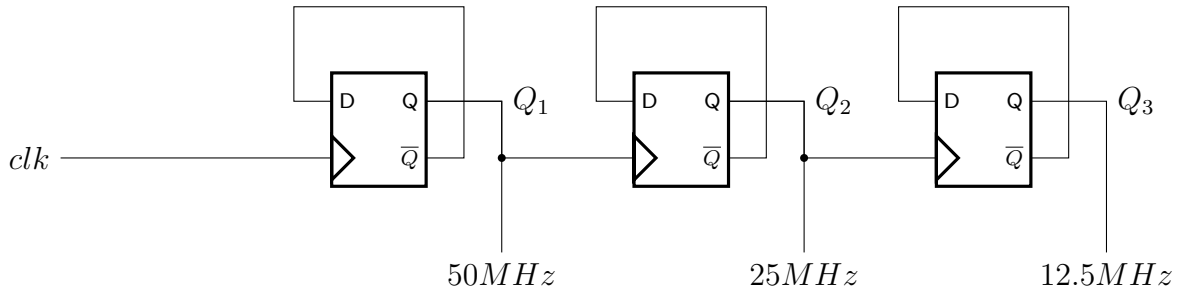
$$\begin{aligned} T &= \overline{J}KQ(t) + J\overline{K}\,\overline{Q(t)} + JK\overline{Q(t)} + JKQ(t) \\ &= +J\overline{Q(t)} + KQ(t) \end{aligned}$$

The circuit...

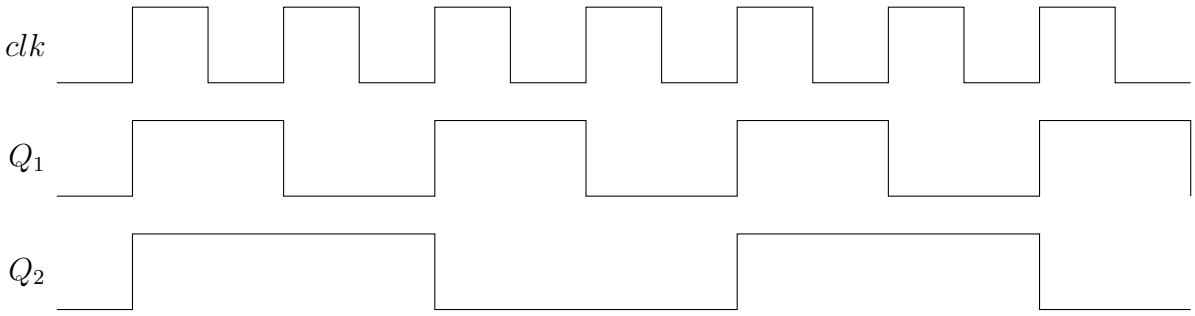


Q2: Assume that you have a 100-MHz clock signal. Derive a circuit using D flip-flops to generate a 50-MHz and 25-MHz clock signal. Draw a timing diagram for all three clock signals.

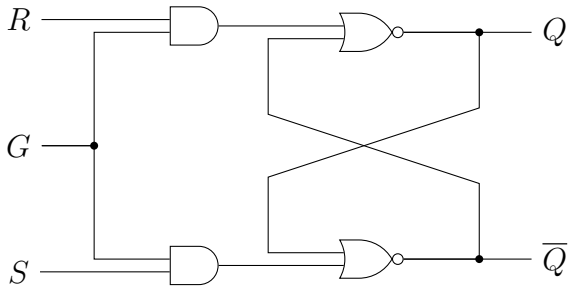
Solution:
Circuit...



The timing diagram...



Q3: Shown below is a gated SR latch and a table explaining its operation.

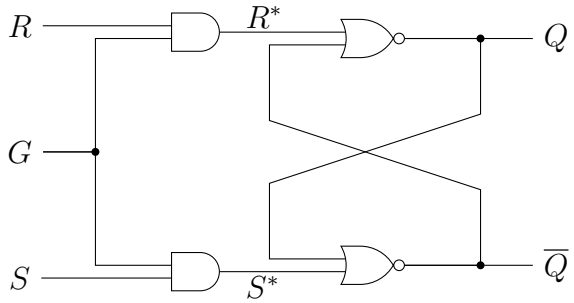


G	S	R	$Q(t+1)$
0	X	X	$Q(t)$ (no change)
1	0	0	$Q(t)$ (no change)
1	0	1	0
1	1	0	1
1	1	1	X

Figure 1: Gated SR latch for Problem 3.

This latch has undefined behaviour when $S = 1$ and $R = 1$ and G changes from 1 to 0. This problem can be solved by making a *set dominated gated SR latch* in which $S = 1$ and $R = 1$ causes the latch to be set to 1. Design a set dominated gated SR latch and draw its circuit.

Solution: Mark the inputs to the regular SR latch as R^* and S^*.



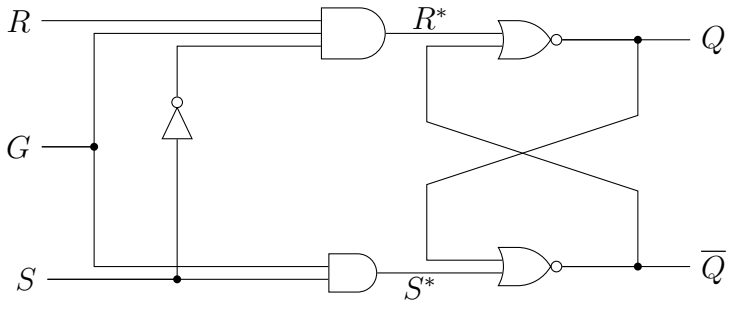
The problem happens when $G = 1$, $R = 1$ and $S = 1$ because this causes $R^* = 1$ and $S^* = 1$. We would like $R^* = 0$ and $S^* = 1$ when $G = 1$, $R = 1$ and $S = 1$. Shown below is what we have as well as what we would want.

G	S	R	S^*	R^*	
0	X	X	0	0	
1	0	0	0	0	
1	1	0	1	0	
1	0	1	0	1	
1	1	1	1	1	← bad

$\rightarrow$

G	S	R	S^*	R^*	
0	X	X	0	0	
1	0	0	0	0	
1	1	0	1	0	
1	0	1	0	1	
1	1	1	1	0	← set dominated

Therefore, we only need to change the equation for R^* to $R^* = GR\overline{S}$. In other words, add an inverter as shown:



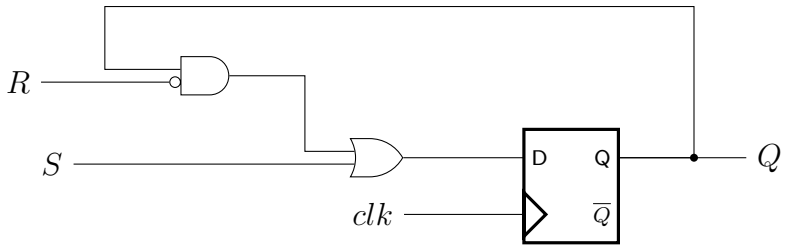
Q4: An SR flip flop is a flip-flop that has set and reset inputs like a gated SR latch. Show how to construct an SR flip-flop using a D flip-flop and other logic gates.

Solution:
Start with the table for the gated SR latch. Then, figure out what the DFF input needs to be in each case to obtain the desired behaviour (Note that the gate G becomes the clock input).

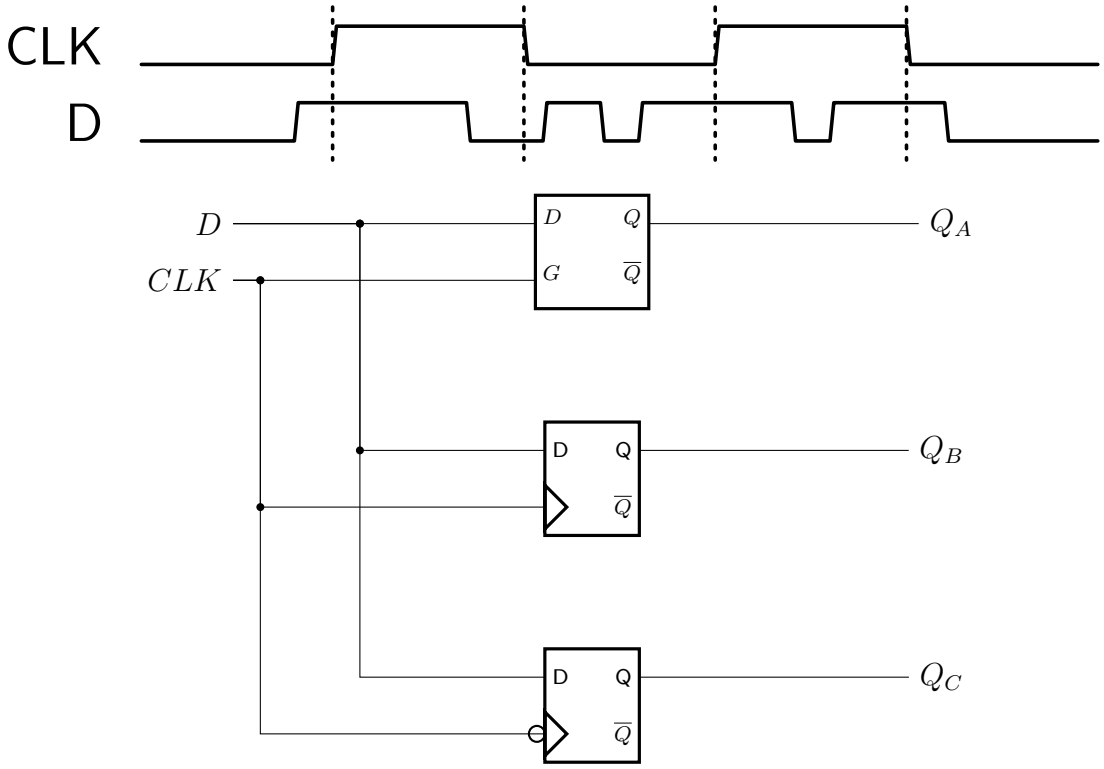
S	R	$Q(t)$	$Q(t+1)$	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	X	X
1	1	1	X	X

Since the inputs $S = 1$ and $R = 1$ are undefined, they become don't care conditions.

We can use a Karnaugh map to find the optimized expression for D is $D = S + \overline{R}Q(t)$. We get the following circuit.



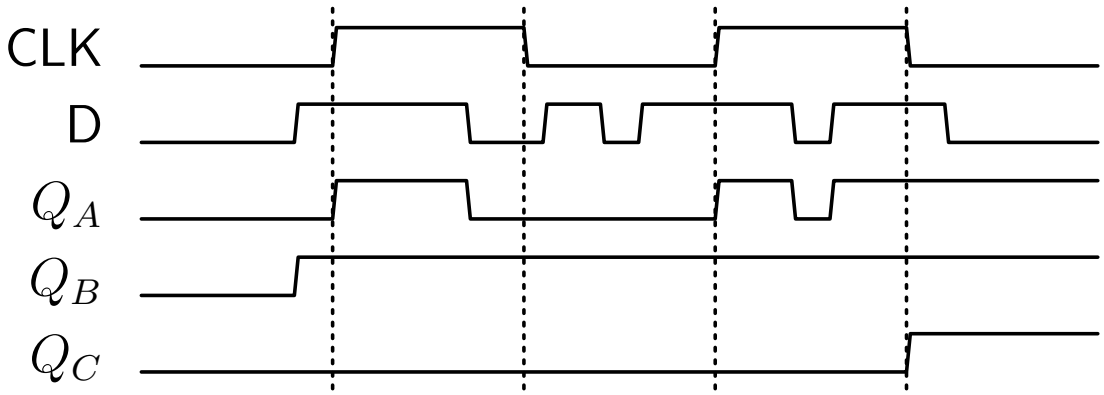
Q5: Consider the timing diagram below which shows a clock signal and a data input signal connected to the inputs of a gated D-latch, a positive edge triggered DFF and a negative edge triggered DFF. Draw the outputs Q_a, Q_b and Q_c for each of the elements.



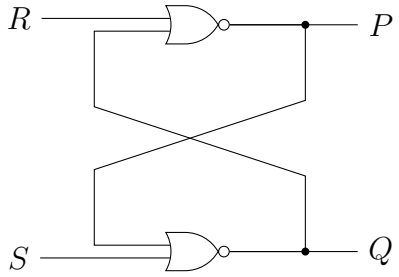
Solution:

1. The gated D latch output holds when $G = 0$ and outputs D when $G = 1$.
2. Positive edge triggered DFF samples D at the rising edge of the clock and keeps that value for one clock period until the next rising edge.
3. Negative edge triggered DFF samples D at the falling edge of the clock and keeps that value for one clock period until the next falling edge.

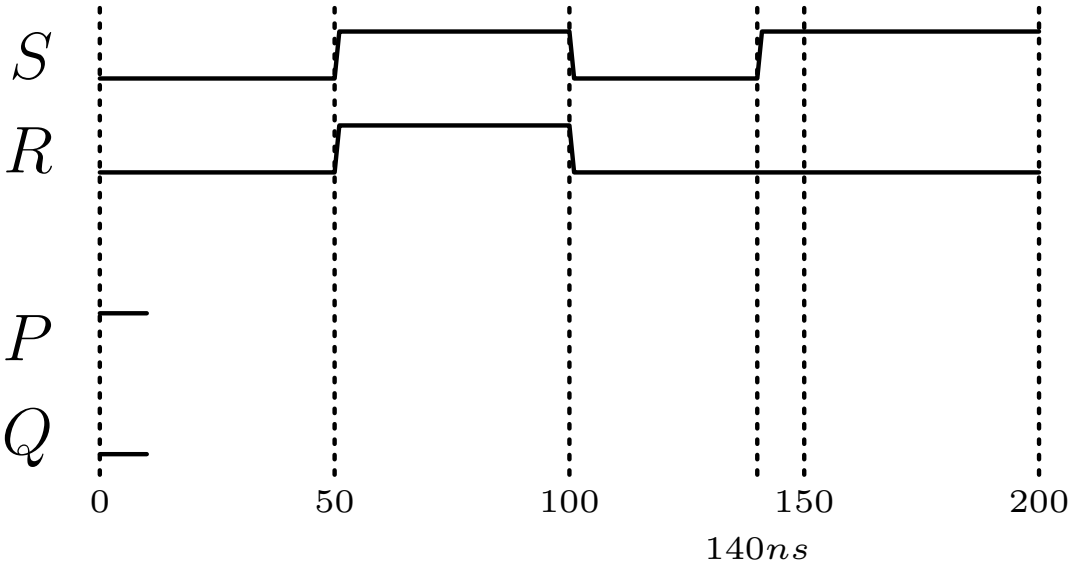
Therefore...



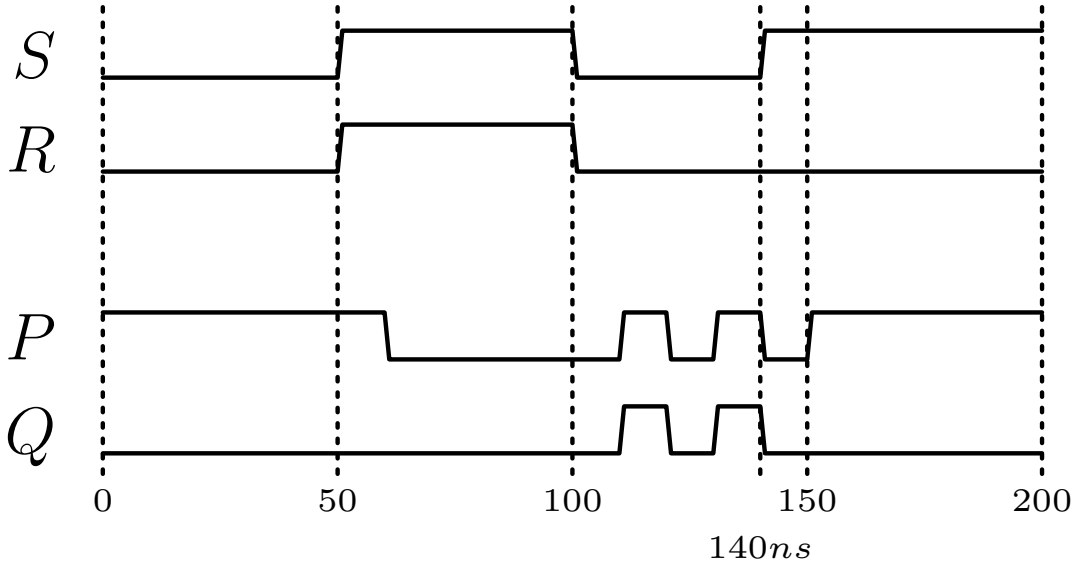
Q6: Consider the SR latch shown below and the accompanying timing diagram — this problem is intended to illustrate the improper operation of the latch if both inputs of the latch are 1 and then changed to 0 at the same time.



Complete the following timing chart. Assume that $P = 1$ and $Q = 0$ initially. Assume that each NOR gate has a delay of $10ns$. Note that when $t = 100ns$, S and R are both changed to 0. Then, $10ns$ later, both P and Q will change to 1. Because the 1's are fed back to the gate inputs, what will happen after another $10ns$?

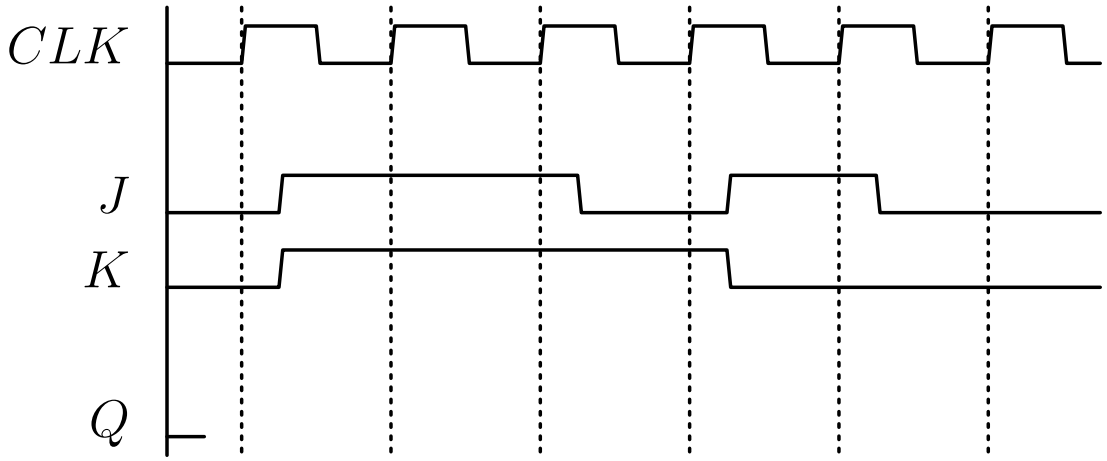


Solution:



1. Initially both $S = 0$ and $R = 0$ which means hold.
2. At $50ns$, both S and R change to 1 which is the undefined state. Both **NOR** gates will output 0, but it takes $10ns$ for P to change to 0.
3. As long as S and R are 1, both outputs are 0 and remain 0.
4. At $100ns$, S and R change to 0. Both **NOR** gates change and P and Q changeto 1 after $10ns$.
5. As long as S and R are 0, the P and Q will propagate back to the **NOR** gate inputs and cause the output to continually flip back and forth.
6. Once $P = 1$ at $140ns$, the latch enters the set state and $P = 1$ and $Q = 0$ after $10ns$.

Q7: Complete the following timing diagram for a JK flip-flop.



Solution:

We just need to recall how a $JKFF$ works. $JK = 00$ means hold, $JK = 11$ means toggle, $JK = 10$ means set and $JK = 01$ means reset.