Comparators

- Common to want to compare two n-bit unsigned numbers $A = a_{n-1}a_{n-2}\cdots a_1a_0$ and $B = b_{n-1}b_{n-2}\cdots b_1a_0$. to determine if $A > B$, $A < B$ or $A = B$.
- Want to build a circuit with 3 outputs $f_{A>B}$, $f_{A=B}$ and $f_{A<B}$ such that:
  1. $f_{A>B} = 1$ when the magnitude of A is larger than B,
  2. $f_{A=B} = 1$ when the magnitude of A is equal to B, and
  3. $f_{A<B} = 1$ when the magnitude of A is smaller than B.
- Let's consider how we compare two numbers and come up with an algorithm.
- Of course, to compare numbers we start at the most significant digit and work towards the least significant digit comparing as we go.

Equality

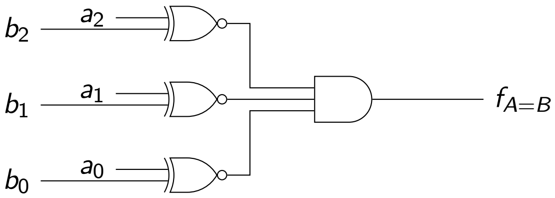
- Equality is straightforward — compare each pair of digits of A and B (a_i and b_i, $\forall i$).
- If all pairs of digits are equal, then the two numbers are equal. Introduce an equality signal for each pairs of bits of A and B as follows: $e_i = a_i' b_i' + a_i b_i = \overline{a_i \oplus b_i}$.

a_i	b_i	$a_i = b_i$?
0	0	1
0	1	0
1	0	0
1	1	1

- Then $f_{A=B} = e_{n-1} e_{n-2} \cdots e_1 e_0$.

Equality

- Circuit for 3-bit comparison $A = B$:



Greater than

- To determine if $A > B$ requires consideration of the *algorithm* used to compare two numbers.
- Consider comparing bits a_i and b_i — bit a_i is larger than bit b_i when $a_i b_i^{'}$ is true.

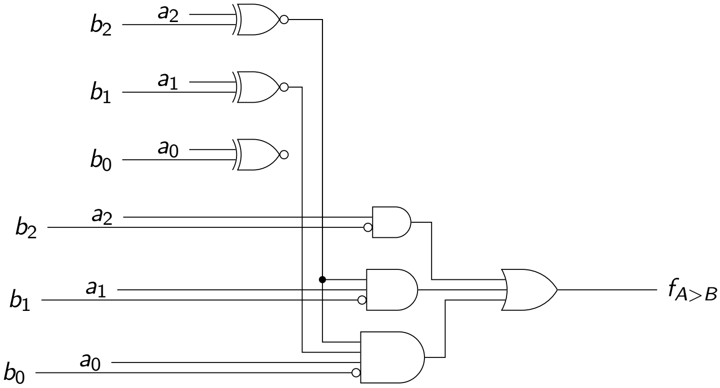
a_i	b_i	$a_i > b_i$?
0	0	0
0	1	0
1	0	1
1	1	0

- To compare for $A > B$: start at MSB and work towards the LSB. At bits a_i and b_i, we can declare $A > B$ if: i) all higher order bits are equal; and ii) $a_i > b_i$.
- Expressed by the equation

$$\begin{aligned} f_{A>B} &= a_{n-1}b_{n-1}^{'} + e_{n-1}a_{n-2}b_{n-2}^{'} + \\ &\quad \cdots + e_{n-1}e_{n-2}\cdots e_2 a_1 b_1^{'} + e_{n-1}e_{n-2}\cdots e_2 e_1 a_0 b_0^{'}. \end{aligned}$$

Greater than

- Circuit for 3-bit comparison $A > B$:



Less than

- Very similar to greater than.
- To determine if $A > B$ requires consideration of the *algorithm* used to compare two numbers.
- Consider comparing bits a_i and b_i — bit a_i is less than bit b_i when $a_i^{'} b_i$ is true.

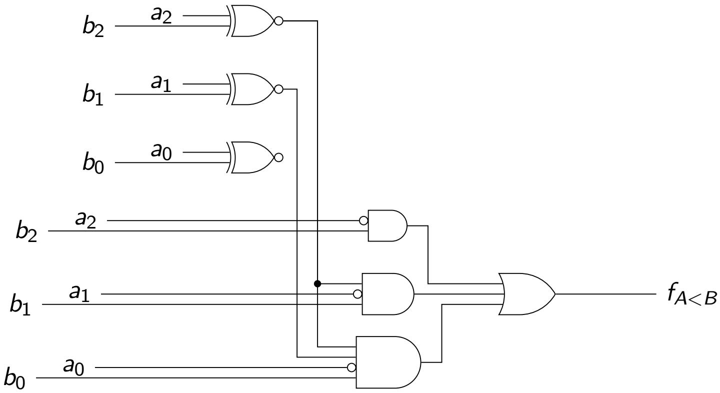
a_i	b_i	$a_i < b_i$?
0	0	0
0	1	1
1	0	0
1	1	0

- To compare for $A < B$: start at MSB and work towards the LSB. At bits a_i and b_i, we can declare $A < B$ if: i) all higher order bits are equal; and ii) $a_i < b_i$.
- Expressed by the equation

$$\begin{aligned} f_{A>B} &= a_{n-1}^{'} b_{n-1} + e_{n-1} a_{n-2}^{'} b_{n-2} + \\ &\quad \cdots + e_{n-1} e_{n-2} \cdots e_2 a_1^{'} b_1 + e_{n-1} e_{n-2} \cdots e_2 e_1 a_0^{'} b_0. \end{aligned}$$

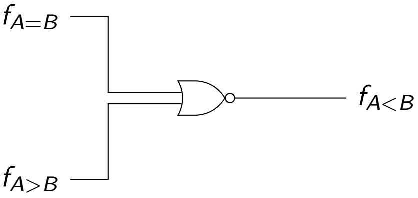
Less than

- Circuit for 3-bit comparison $A < B$:



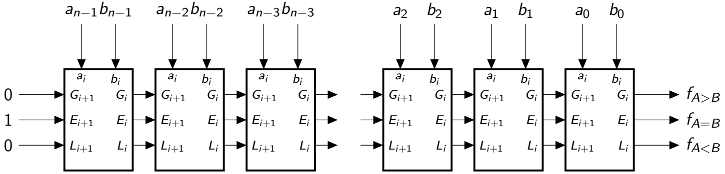
Alternative for $A < B$

- If we already have a circuit for $A = B$ and $A > B$, then we can compute $A < B$ with less circuitry.
- We know $A < B$ if A is not equal to B and A is not greater than B. Logically, this can be expressed as $f_{A<B} = \overline{f_{A=B} + f_{A>B}}$.



Hierarchical or iterative comparator design

- Circuits for $A = B$, $A > B$ or $A < B$ as previously designed only require a few levels of logic.
- However, as we have more bits n, the gates get prohibitively large (they require a large number of inputs). For example, to test $A = B$ for n-bits requires an n-input **AND** gate.
- We can design an iterative comparator by designing a single smaller circuit and then copying this smaller circuit n times.

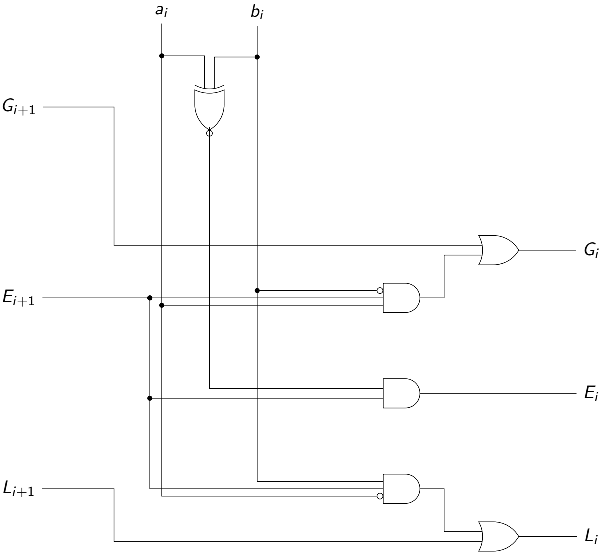


Hierarchical or iterative comparator design

- Each block i receives as input a_i and b_i and *results of the comparison of higher bits* G_{i+1}, L_{i+1} and E_{i+1}.
- Each block i produces outputs G_i, L_i and E_i which indicate the decision made about the comparison based on bits larger than or equal to i.
- $$E_i = \underbrace{E_{i+1}}_{\text{higher bits are all equal}} \overbrace{(\overline{a_i \oplus b_i})}^{\text{current bits equal}} = E_{i+1}(\overline{a_i \oplus b_i})$$
- $$G_i = \underbrace{G_{i+1}}_{\text{higher bits imply } A>B} + \overbrace{E_{i+1}a_ib_i^{'}}^{\text{current bits indicate } A>B} = G_{i+1} + E_{i+1}a_ib_i^{'}$$
- $$L_i = \underbrace{L_{i+1}}_{\text{higher bits imply } A<B} + \overbrace{E_{i+1}a_i^{'}b_i}^{\text{current bits indicate } A<B} = L_{i+1} + E_{i+1}a_i^{'}b_i$$

Hierarchical or iterative comparator design

- Circuit:



Hierarchical or iterative comparator design

- This circuit would suffer from worse performance compared to the original comparator.
- However, this circuit — at the most — requires a 3-input **AND** gate.