ECE 124 digital circuits and systems
Assignment #8

Q1: Design a modulo-6 counter which counts in the sequence $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5$ and repeats. The counter has one input *count*. The circuit should count only when *count* $= 1$, otherwise the circuit should not count. Design the counter using D flip-flops, T flip-flops and JK flip-flops.

Q2: Consider a counter-like circuit with one input x. When $x = 1$, the circuit should add 2 to its current value, wrapping around if the count reaches 8 or 9 — this means that if the current value is 8 or 9, then the next count value becomes 0 or 1, respectively. If $x = 0$, then the counter subtracts 1 from its current value, thus acting like a normal down-counter. Design this circuit using D flip-flops, T flip-flops and JK flip-flops.

Q3: The state table for a Moore sequential circuit with one input w and one output z is shown below. States are already assigned binary patterns.

Current State	Next State		Output
	$w = 0$	$w = 1$	
$q_1 q_0$	$q_1 q_0$	$q_1 q_0$	z
00	10	11	0
01	01	00	0
10	11	00	0
11	10	01	1

Derive a circuit for this state table using D flip-flops and then another circuit for this state table using JK flip-flops.

Q4: A clocked Mealy sequential circuit has one input x and one output z. The output should be $z = 1$ when the input sequences 1001 or 1111 appear at the input x, otherwise $z = 0$. Overlapping input patterns are allowed. An example of the desired behaviour is:

x:	0	1	0	1	1	1	1	0	0	1	1	0	0	1	1	1	1	1	...
z:	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	1	1	...

Find a Mealy state diagram and state table for this problem.

Q5: A sequential circuit has one input x and one output z. The circuit examines groups of four consecutive inputs and produces an output $z = 1$ if the input sequence 0101 or 1001 occurs. The circuit resets after every four inputs. An example of the desired behaviour is:

x:	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0	0	...
z:	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	...

Find a Mealy state diagram for this problem.

Q6: A sequential circuit has two inputs x and y and one output z. Its function is to compare the input sequences on the two inputs. If $x = y$ during any four consecutive clock cycles, the circuit produces $z = 1$, otherwise $z = 0$. An example of the desired behaviour is:

x:	0	1	1	0	1	1	1	0	0	0	1	1	0	...
y:	1	1	1	0	1	0	1	0	0	0	1	1	1	...
z:	0	0	0	0	1	0	0	0	0	1	1	1	0	...

Find a state diagram and state table for this problem.

Q7: A sequential circuit has two inputs x and y and one output z. the output remains a constant value unless one of the following input sequences occurs:

(a) The input sequence $xy = 01, 11$ causes the output to become 0;

(b) The input sequence $xy = 10, 11$ causes the output to become 1;

(c) The input sequence $xy = 10, 01$ causes the output to change value.

The notation $xy = 01, 11$ means $x = 0, y = 1$ followed by $x = 1, y = 1$. Derive a Moore state diagram for this problem.

Q8: A sequential circuit has one input x and two outputs z_1 and z_2. The output $z_1 = 1$ occurs every time the input sequence 100 is completed, provided that the sequence 010 has never occurred. An output $z_2 = 1$ occurs every time the input sequence 010 is completed. Note that once $z_2 = 1$ has occurred, then $z_1 = 1$ can never occur but not vice versa. A typical input and output sequence is:

x:	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0 ...
z_1:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0 ...
z_2:	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0	0	0	0	1 ...

Find a Mealy state diagram and state table for this problem (8 states is possible).

Q9: A clocked Moore sequential circuit should have output $z = 1$ if the total number of 0's received at input x is an even number greater than zero, provided that two consecutive 1's have never been received.

Derive a state diagram for this problem. Provide a description for each state (e.g., "s_1" means "odd number of 0's", etc.).

Q10: Derive a state table and a state diagram for the circuit shown below. If you were told that this circuit was a sequence detector, what input sequence is detected by this circuit?