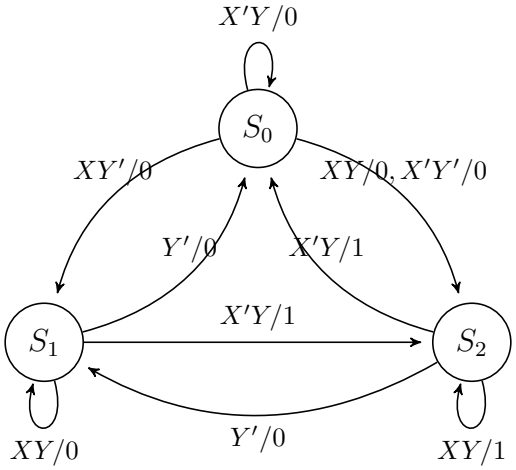
ECE 124 digital circuits and systems
Assignment #9

Q1: Consider the state table shown below for a circuit with one input x and one output z.

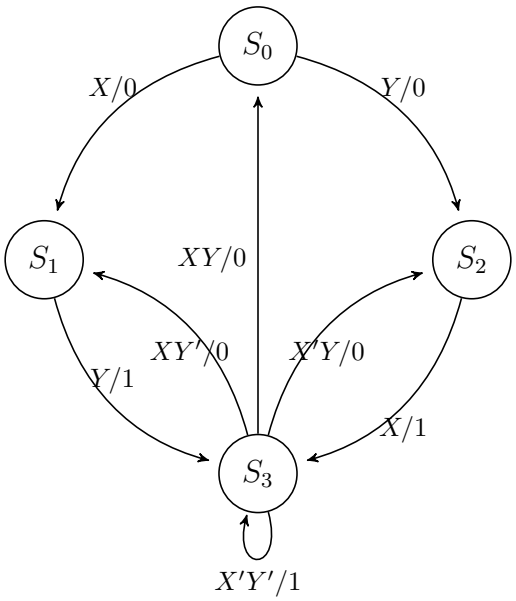
Current State	Next State $x=0$	Next State $x=1$	Output z
A	C	D	0
B	B	A	0
C	D	A	0
D	C	B	1

Use one hot encoding and derive a suitable circuit using D flip-flops that implements this state table.

Q2: Implement the following state diagram using D flip-flops and one-hot encoding. Write down the necessary flip-flop input equations and output equations by inspecting the state diagram directly. Note that all possible input conditions are shown for the transitions leading away from every state.



Q3: Consider the following state diagram for a circuit with two inputs X and Y and one output Z. It was drawn in a weird way; If $X = 1$ and $Y = 1$, then X takes precedence. Further, self-loops are not shown.



Clarify the state diagram by adding self loops where needed. Clarify the input labeling on the edges so that everything is very clear. Finally, using your clarified state diagram, implement the circuit using D flip-flops and one-hot encoding.

Q4: Consider the following state table for a circuit with one input x and one output z. The output is a function of the state only and does not depend on the input. Perform state minimization to reduce the required number of states. Derive a circuit for the reduced state table which requires the minimum number of flip-flops. Use D flip-flops.

Current State	Next State $x = 0$	Next State $x = 1$	Output z
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

Q5: A Mealy sequential circuit has one input x and one output z. During four consecutive clock cycles, a sequence of four values of x are applied. The output is $z = 1$ when either the input sequence 0010 or 1110 is detected, otherwise $z = 0$. The circuit resets after four input bits are applied, ready for the next four bit sequence. Derive a *minimized* state table for the sequential circuit.

Q6: Shown below is a state table. Note that in some situations, the next state is left as *unspecified*; an unspecified state is like a don't care condition and can be matched appropriately. Derive an equivalent state table with a minimum number of states.

Current State	Next State		Output z	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	B	C	0	0
B	D	-	0	0
C	F	E	0	1
D	B	G	0	0
E	F	C	0	1
F	E	D	0	1
G	F	-	0	1

Q7: Shown below is a state table. Note that in some situations, the next state is left as *unspecified*; an unspecified state is like a don't care condition and can be matched appropriately. Derive an equivalent state table with a minimum number of states.

Current State	Next State		Output z	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	B	C	0	0
B	D	-	0	1
C	F	E	0	1
D	B	G	0	0
E	F	C	0	1
F	E	D	0	1
G	F	-	0	0

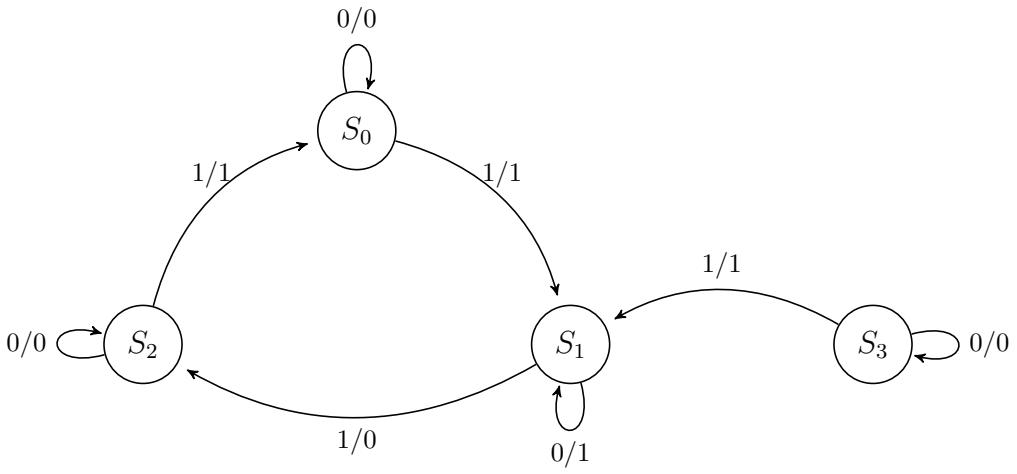
Q8: Reduce the following state table to a minimum number of states.

Current State	Next State $xy = 00$	$xy = 01$	$xy = 11$	$xy = 10$	Output z
a	a	c	e	d	0
b	d	e	e	a	0
c	e	a	f	b	1
d	b	c	c	b	0
e	c	d	f	a	1
f	f	b	a	d	1

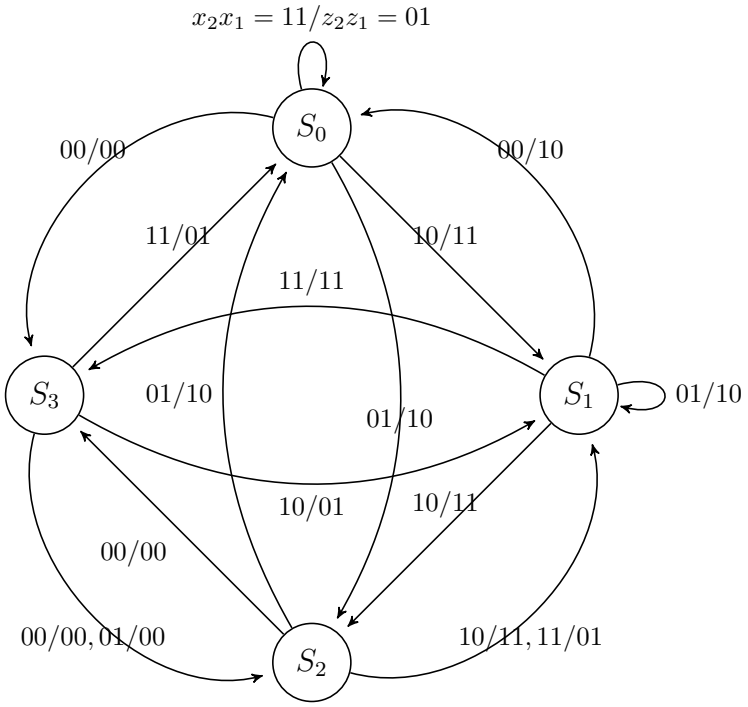
Q9: Reduce the following state table to a minimum number of states.

Current State	Next State $xy = 00$	$xy = 01$	$xy = 11$	$xy = 10$	Output z
a	b	i	c	g	0
b	b	c	f	g	0
c	h	d	d	f	1
d	h	c	e	g	1
e	b	c	i	g	0
f	f	i	i	k	0
g	j	k	g	h	0
h	e	f	c	g	0
i	i	i	i	d	0
j	b	f	c	g	0
k	a	c	e	d	1

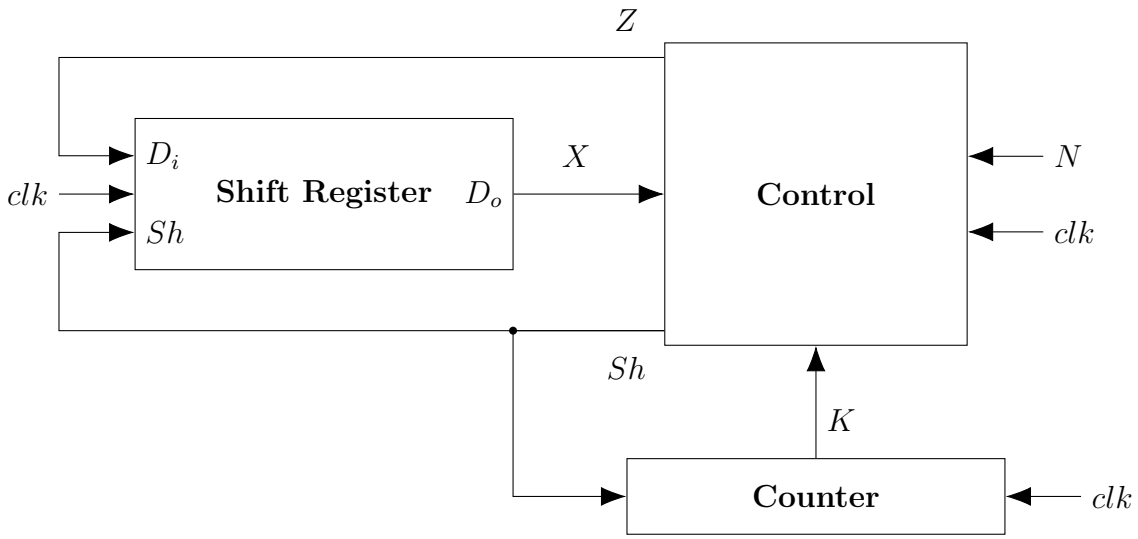
Q10: Shown below is a state diagram for a circuit with one input x and one output z. Convert the following state diagram into an ASM chart.



Q11: Shown below is a state diagram for a circuit with two inputs x_1 and x_2 and two outputs z_1 and z_2. Convert the state diagram into an ASM chart. Test only one variable in each decision box. Try to minimize the number of decision boxes.



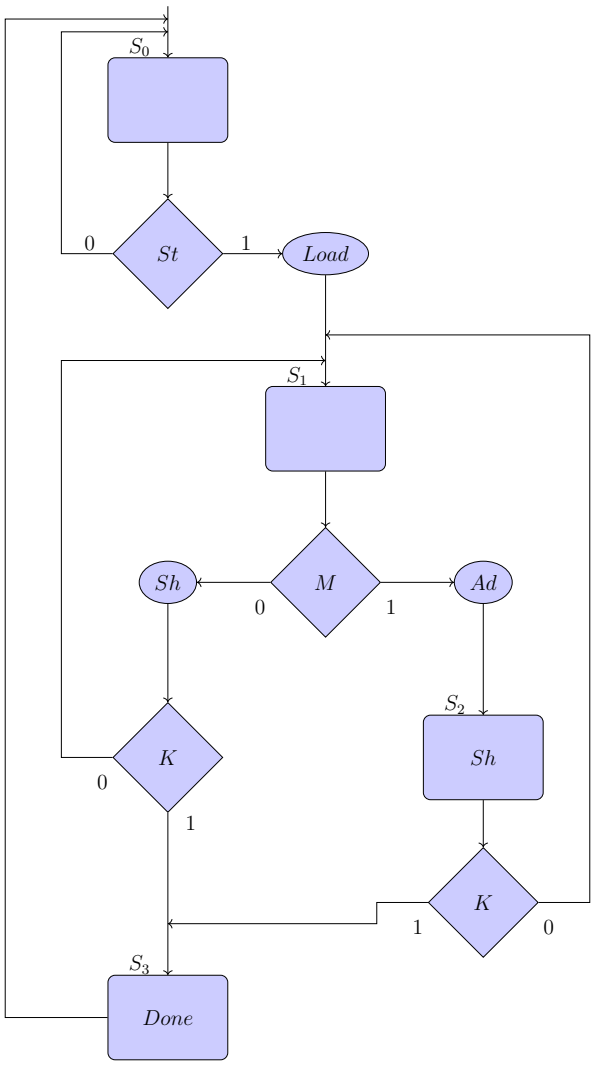
Q12: Shown below is a circuit which forms the 2's complement of a 16-bit binary number. The circuit consists of three main parts — a 16-bit shift register which initially holds the number to be complemented, a control circuit, and a counter circuit which counts the number of shifts. The control circuit processes the number in the shift register one bit at a time (via input X) and outputs the 2's complemented result (via output Z) which is stored back in the shift register one bit at a time. The control circuit also generates the necessary shift signals. The counter counts the number of shifts and outputs $K = 1$ once the counter reaches 15, otherwise $K = 0$. Finally, the control circuit has input N which is a start signal; when $N = 1$ the circuit performs its operation.



To perform the 2's complement using this circuit, the control circuit implements the rule "starting with the least significant bit, complement all the bits to the left of the first 1".

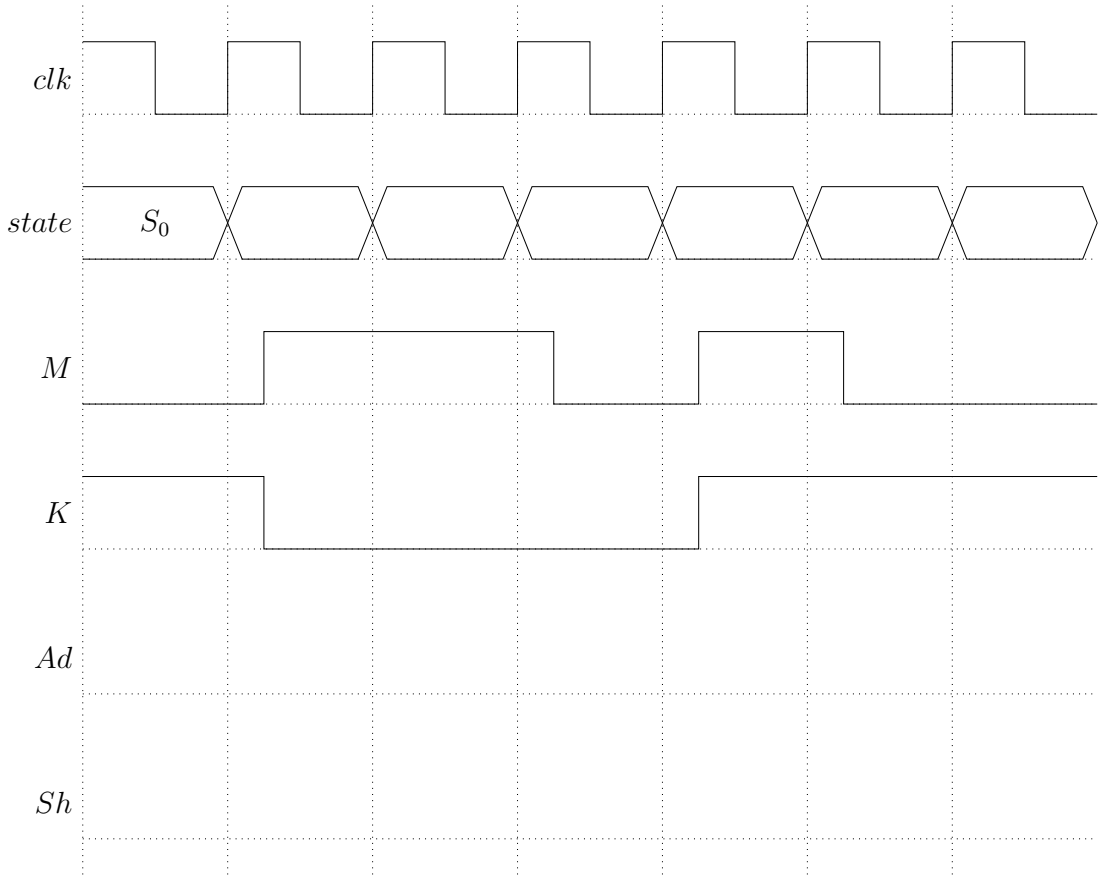
Draw an ASM chart for the control unit (only three states are required).

Q13: Shown below is an ASM chart (4 states) for a circuit with three inputs (St, M and K) and four outputs (*Load*, *Ad*, *Sh* and *Done*).



(a) Draw an equivalent state diagram for this ASM chart.

(b) Complete the following timing diagram showing states and the output signals Ad and Sh. You may assume $St = 1$.


clk
state
S_0
M
K
Ad
Sh