# ECE 124 digital circuits and systems
# Assignment #5

Q1: In class we designed a comparator for two, $n$-bit unsigned binary numbers $A$ and $B$ by deriving 2 level SOP for $(A = B)$, $(A > B)$ and $(A < B)$. Such circuits can require logic gates with many inputs as $n$ increases.

Another way to make a comparator is to design a block which can be replicated $n$ times; this is shown below. Determine the logic inside of each block which will compare two, $n$-bit unsigned binary numbers.

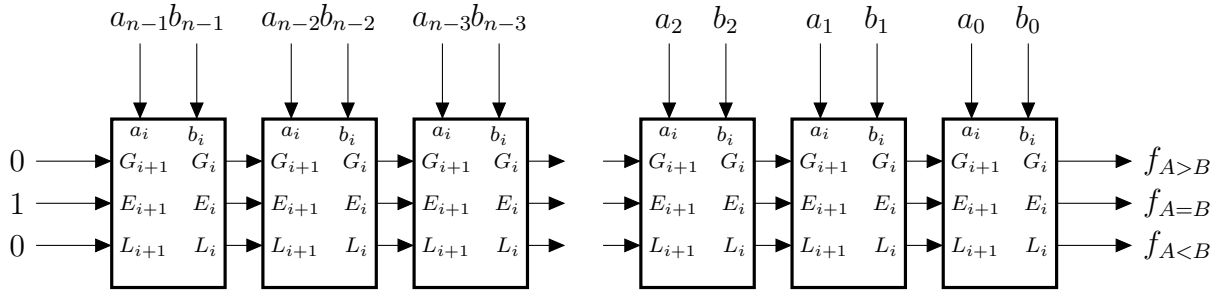


Figure 1: An $n$-bit comparator made from $n$ identical sub-circuits.

Q2: Given the solution to Question 1, how long (in terms of gate delays) does it take to compare two, $n$-bit numbers?

Q3: Given the solution to Question 1 and 2, how would you design a comparator circuit that is faster than the comparator designed in Question 1, but uses logic gates with a reasonable number of inputs?

Q4: Implement the following 3-input binary functions using 3-to-8 decoders and an OR gate.

(a) $f(a, b, c) = \sum(0, 2, 3, 4, 5, 7)$.

(b) $f(a, b, c) = \sum(1, 2, 3, 5, 6)$.

Q5: Implement the following logic functions using a 2-to-1 multiplexer and as few additional logic gates as possible.

(a) $f = a'c' + bc' + a'b$.

(b) $f = b'c' + ab$.

Q6: Implement the 4-input logic function $f(a, b, c, d) = \sum(0, 1, 3, 4, 8, 9, 15)$ using an 8-to-1 multiplexer.

Q7: Use Shannon expansion to derive an implementation for each of the following functions using a 2-to-1 multiplexer and any other necessary logic gates.

(a) $f(a, b, c) = \sum(0, 2, 3, 6)$.

(b) $f(a, b, c) = \sum(0, 4, 6, 7)$.

Q8: Use Shannon expansion to derive the minterms for each of the following expressions.

(a) $f = b' + a'c' + ac$.

(b) $f = b + a'c'$.

Q9: Shown in Figure 2 is a prefabricated block of logic. Show how the function $f = bc' + ac + b'c$ can be implemented in this prefabricated block. You may also use the constants 0 and 1 if needed.

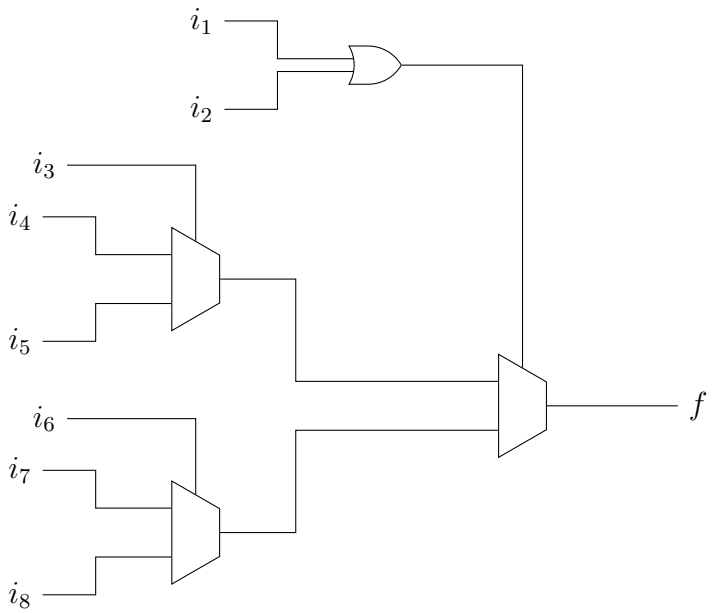


Figure 2: Prefabricated circuit block for Question 9.

Q10: Derive a circuit for an 8-to-3 priority encoder.

Q11: Implement a full adder using two 4-to-1 multiplexers.