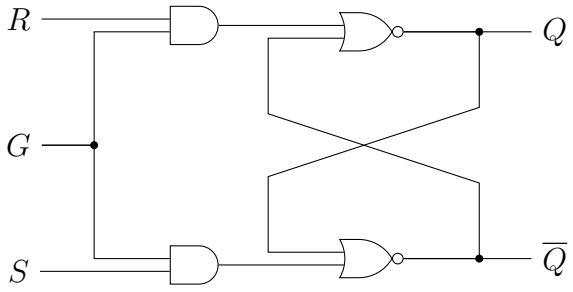
ECE 124 digital circuits and systems
Assignment #6

Q1: Show how a JK flip-flop can be implemented with a T flip-flop and other logic gates.

Q2: Assume that you have a 100-MHz clock signal. Derive a circuit using D flip-flops to generate a 50-MHz and 25-MHz clock signal. Draw a timing diagram for all three clock signals.

Q3: Shown below is a gated SR latch and a table explaining its operation.



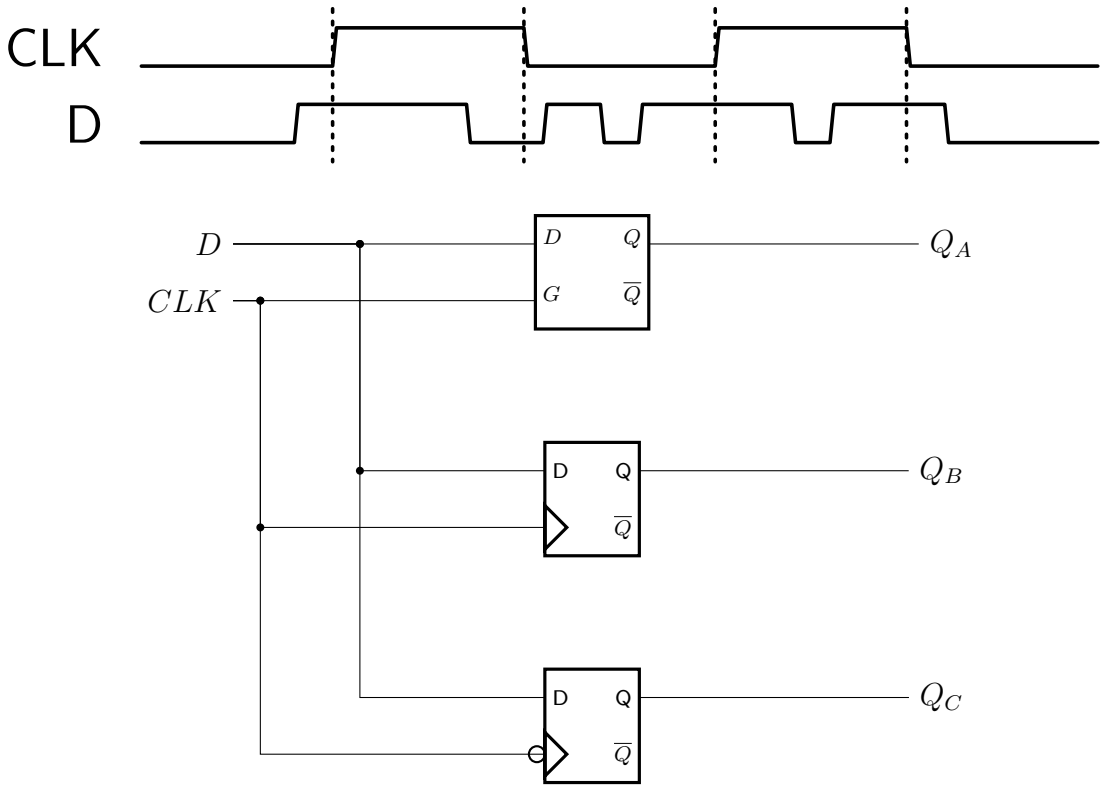
G	S	R	$Q(t+1)$
0	X	X	$Q(t)$ (no change)
1	0	0	$Q(t)$ (no change)
1	0	1	0
1	1	0	1
1	1	1	X

Figure 1: Gated SR latch for Problem 3.

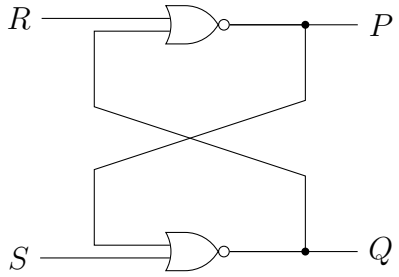
This latch has undefined behaviour when $S = 1$ and $R = 1$ and G changes from 1 to 0. This problem can be solved by making a *set dominated gated SR latch* in which $S = 1$ and $R = 1$ causes the latch to be set to 1. Design a set dominated gated SR latch and draw its circuit.

Q4: An SR flip flop is a flip-flop that has set and reset inputs like a gated SR latch. Show how to construct an SR flip-flop using a D flip-flop and other logic gates.

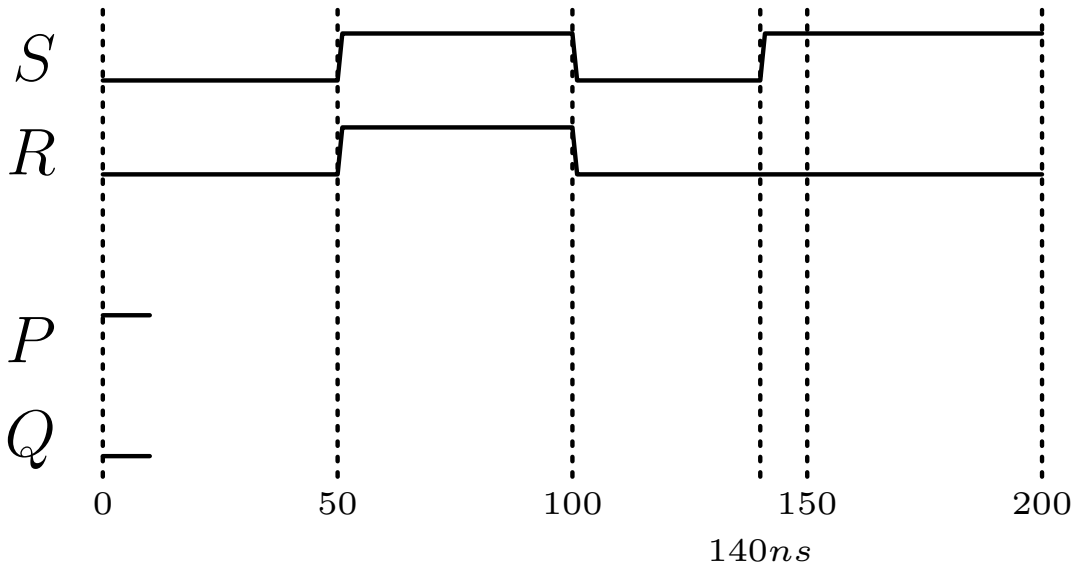
Q5: Consider the timing diagram below which shows a clock signal and a data input signal connected to the inputs of a gated D-latch, a positive edge triggered DFF and a negative edge triggered DFF. Draw the outputs Q_a, Q_b and Q_c for each of the elements.



Q6: Consider the SR latch shown below and the accompanying timing diagram — this problem is intended to illustrate the improper operation of the latch if both inputs of the latch are 1 and then changed to 0 at the same time.



Complete the following timing chart. Assume that $P = 1$ and $Q = 0$ initially. Assume that each NOR gate has a delay of $10ns$. Note that when $t = 100ns$, S and R are both changed to 0. Then, $10ns$ later, both P and Q will change to 1. Because the 1's are fed back to the gate inputs, what will happen after another $10ns$?



Q7: Complete the following timing diagram for a JK flip-flop.