



Department of Electrical and Computer Engineering  
ECE124 Digital Circuits and Systems

MIDTERM EXAMINATION  
Feb 28, 2013

Instructor(s): A. Kennings

Time Allowed: 1 hour 30 minutes

Name:	Andrew Kennings
Id#:	Solutions
Lecture: (check one):	<input type="checkbox"/> LEC 001 (EE/CE Students) <input type="checkbox"/> LEC 002 (SE Students)

Instructions:

1. Answer all questions. The examination is 90 minutes in length.
2. The examination is a closed book examination. There are no "aid sheets" permitted.
3. All cell phones and/or other electronic devices must be turned off and packed away prior to the beginning of the examination.
4. Clearly show all steps used in the solution process. No marks will be given for numerical results unless accompanied by a correct solution method.
5. Please write the examination in pen, not pencil. If you decide to use pencil anywhere, you will not be allowed to request remarking of your examination.

Q1	Q2	Q3	Q4	Q5	TOTAL
12	12	12	12	12	60

**Question #1: Number representations and arithmetic**

**Part A)**

Complete the following table by converting the number  $(1523)_6$  to: (i) base-10; (ii) base-2; and (iii) base-16. [4 marks]

Number System	Representation
Base-6	$(1523)_6$
Base-10	$(411)_{10}$
Base-2	$(110011011)_2$
Base-16	$(19B)_{16}$

$$\begin{aligned}
 (1523)_6 &= 1 \times 6^3 + 5 \times 6^2 + 2 \times 6^1 + 3 \times 6^0 \\
 &= 216 + 180 + 12 + 3 \\
 &= 411 = (411)_{10}
 \end{aligned}$$

$$\begin{array}{rcl}
 2 \overline{) 411} & & \text{LSB} \\
 2 \overline{) 205} & \rightarrow & 1 \\
 2 \overline{) 102} & \rightarrow & 1 \\
 2 \overline{) 51} & \rightarrow & 0 \\
 2 \overline{) 25} & \rightarrow & 1 \\
 2 \overline{) 12} & \rightarrow & 1 \\
 2 \overline{) 6} & \rightarrow & 0 \\
 2 \overline{) 3} & \rightarrow & 0 \\
 2 \overline{) 1} & \rightarrow & 1 \\
 0 & \rightarrow & 1 \quad \text{MSB}
 \end{array}$$

$$\begin{array}{c}
 \underline{110011011} \\
 1 \quad 9 \quad B
 \end{array}$$

Part B)

Convert the number  $(41.6875)_{10}$  to its base-2 representation. [4 MARKS]

$$\begin{array}{r}
 2 \overline{) 41} \\
 \underline{20} \rightarrow 1 \\
 2 \overline{) 10} \rightarrow 0 \\
 2 \overline{) 5} \rightarrow 0 \\
 2 \overline{) 2} \rightarrow 1 \\
 2 \overline{) 1} \rightarrow 0 \\
 0 \rightarrow 1
 \end{array}$$

$$\begin{array}{r}
 0.6875 \times 2 = 1.3750 \\
 0.3750 \times 2 = 0.7500 \\
 0.7500 \times 2 = 1.5000 \\
 0.5000 \times 2 = 1.0000 \\
 0.0000 \times 2 = 0.0000
 \end{array}$$

$$(41.6875)_{10} = (101001.1011)_2$$

Part C)

Perform subtraction of the following two signed 8-bit numbers which are represented using 2's complements. What is the result of the numerical operation expressed in decimal? Has overflow occurred? [4 marks]

$$\begin{array}{r}
 1111\ 1000 \\
 - 0101\ 1111 \\
 \hline
 \end{array}$$

$$\begin{array}{r}
 1010\ 0001 \\
 + 1111\ 1000 \\
 \hline
 1\ 1001\ 1001
 \end{array}$$

result (negative, so 2's complement to set value)

$$\begin{array}{r}
 1001\ 1001 \\
 \xrightarrow{\text{2's comp}} \\
 0110\ 0111 \\
 \hline
 = 103
 \end{array}$$

⇒ result is -103

No overflow

Question #2: Boolean algebra, truth tables and canonical forms

Part A)

Simplify  $f = [(x'y' + z)' + z + xy + wz]'$  using only Boolean algebra. Show all steps clearly to obtain full marks. [6 marks]

Lots of different solutions... Some shorter than this.

$$\begin{aligned}
 f &= [(\overline{x\bar{y} + z}) + z + xy + wz]' \\
 &= [\overline{x\bar{y}} \cdot \bar{z} + z + xy + wz]' \\
 &= [(x+y)\bar{z} + z + xy + wz]' \\
 &= [x\bar{z} + y\bar{z} + xy + z]' \\
 &= [x\bar{z} + y\bar{z} + xy + \overbrace{xz + x\bar{z} + zy + z\bar{y}}^z]' \\
 &= [x + y + xy + z]' \\
 &= [x + y + z]' \\
 &= \bar{x} \cdot \bar{y} \cdot \bar{z}
 \end{aligned}$$



Part B)

Write down the truth table for the following 3-input function  $f = xy + x'z$ . Write down the canonical sum-of-minterms and canonical ~~sum~~<sup>product</sup>-of-maxterms for the function. Do not use shorthand notation! [6 marks]

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Annotations: A bracket labeled  $\bar{x}z$  spans the rows where x=0 and z=1. A bracket labeled  $xy$  spans the rows where x=1 and y=1.

$$f = \bar{x}\bar{y}z + \bar{x}yz + xy\bar{z} + xyz \quad (\text{SOP})$$

$$f = (x+y+z)(x+\bar{y}+z)(\bar{x}+y+z)(\bar{x}+y+\bar{z}) \quad (\text{POS})$$

### Question #3: Karnaugh maps and optimization

#### Part A)

Shown below is the truth table for a 4-input logic function  $f = f(w, x, y, z)$ . Using Karnaugh maps, derive both a minimized sum-of-products and a minimized product-of-sums for the function. Blank Karnaugh maps are provided. [6 marks]

w	x	y	z	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	X
0	0	1	1	0
0	1	0	0	X
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	X
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

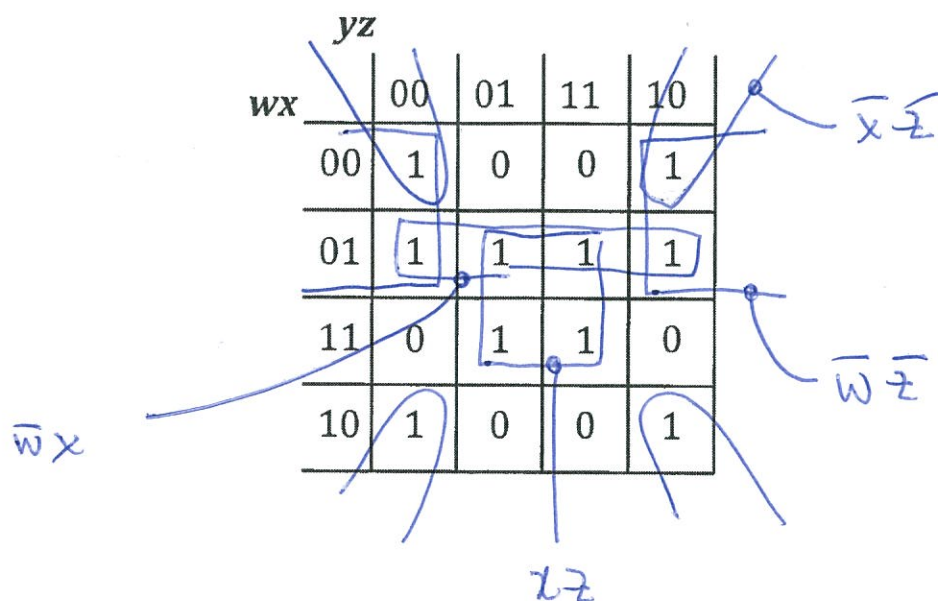
		$\bar{x}\bar{z}$		$yz$	
		00	01	11	10
00		1	0	0	X
01	$w\bar{x}$	X	0	0	1
11		0	1	0	1
10		1	0	0	X
					$y\bar{z}$
					$w\bar{x}\bar{y}z$
		00	01	11	10
00		1	0	0	X
01		X	0	0	1
11	$w\bar{x}$	0	1	0	1
10		1	0	0	X
					$\bar{y}+\bar{z}$
					$x+\bar{z}$
					$w+\bar{z}$

$$f = \bar{x}\bar{z} + y\bar{z} + w\bar{x}\bar{y}z \quad (\text{min SOP})$$

$$f = (\bar{y}+\bar{z})(x+\bar{z})(w+\bar{z})(\bar{x}+y+z) \quad (\text{min POS})$$

Part B)

Shown below is the Karnaugh map for a 4-input logic function  $f = f(w, x, y, z)$ . Find and write down all the prime implicants for the logic function and determine which ones are essential. [6 MARKS]



prime implicants (4 of them)

$xz \leftarrow$  essential

$\bar{w}x$

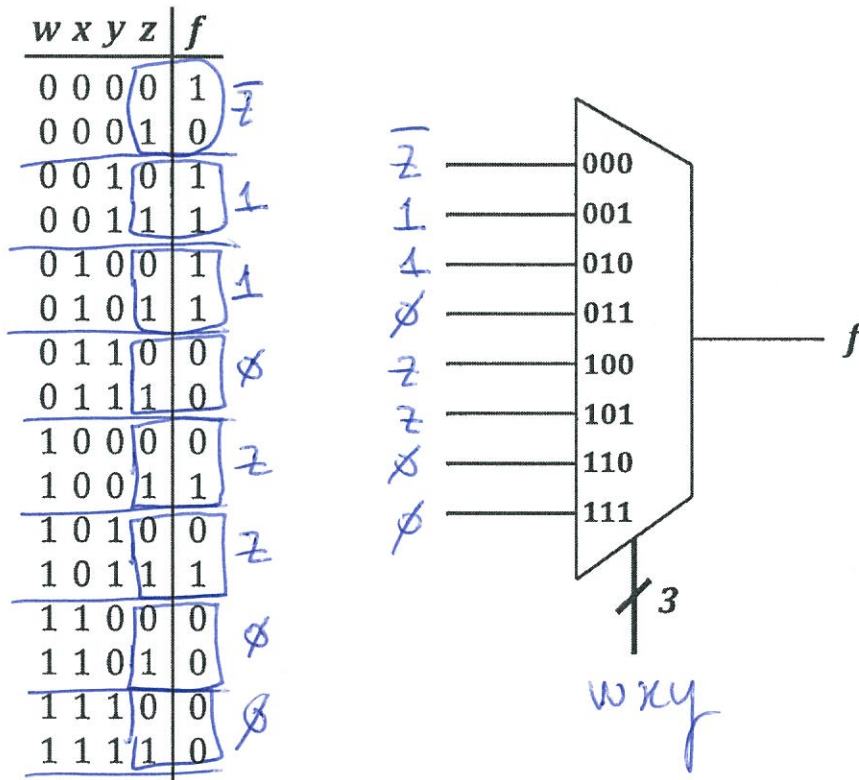
$\bar{x}\bar{z} \leftarrow$  essential

$\bar{w}\bar{z}$

Question 4: Combinational circuit blocks

Part A)

Implement the 4-input logic function  $f = f(w, x, y, z)$  shown in the truth table below using an 8-input multiplexer. [4 marks]

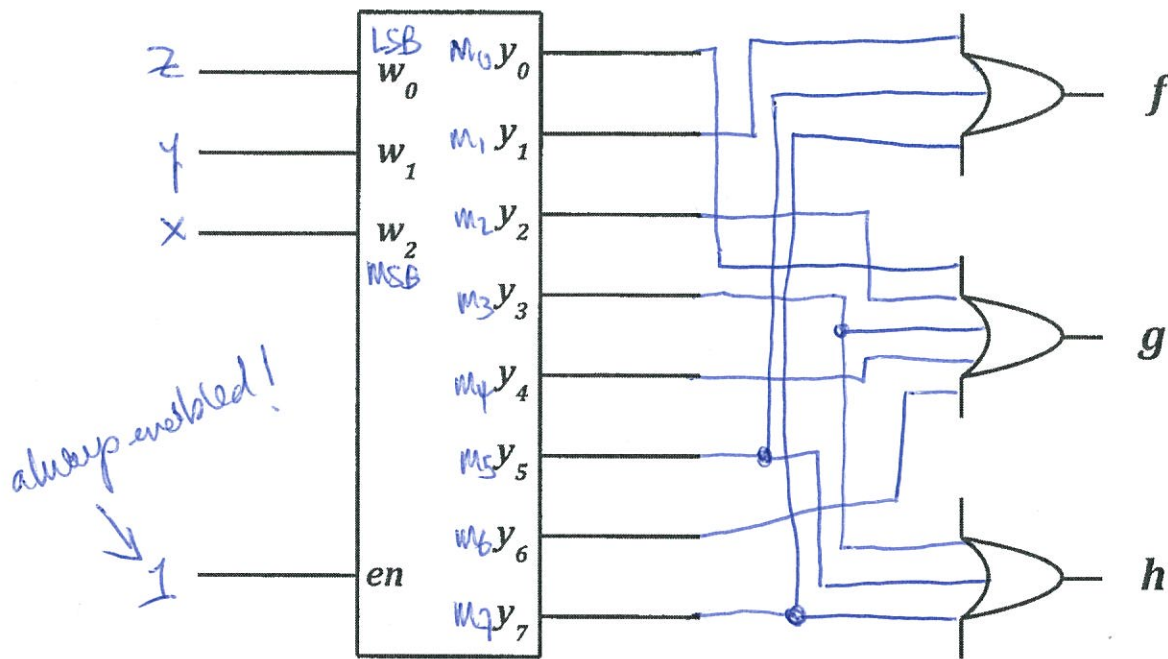


Different solutions possible.



**Part B)**

Complete the diagram below to show how to implement the three logic functions given by  $f = (y' + x)z$ ,  $g = y'z' + x'y + yz'$ , and  $h = (x + y)z$  using only a 3-to-8 decoder and OR gates. [4 marks]



Need min terms for each function

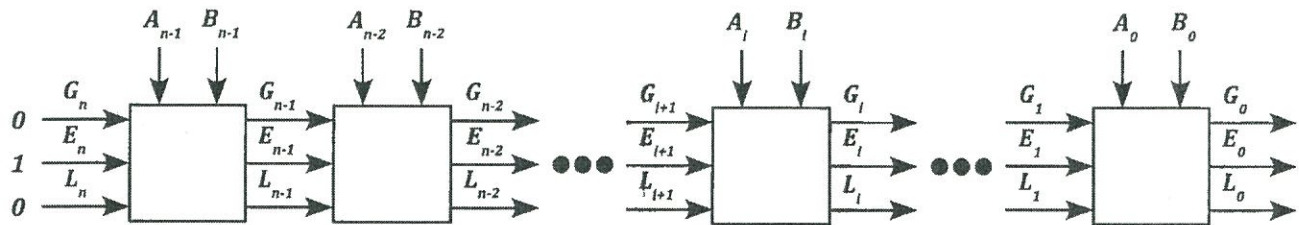
$$f = (\bar{y} + x)z = \bar{y}z + xz = \bar{x}\bar{y}z + x\bar{y}z + xy\bar{z} + x\bar{y}z \\ = \bar{x}\bar{y}z + x\bar{y}z + xy\bar{z} = m_1 + m_5 + m_7$$

$$h = (x + y)z = xz + yz = xyz + x\bar{y}z + xy\bar{z} + \bar{x}yz \\ = x\bar{y}z + \bar{x}yz + xy\bar{z} = m_5 + m_3 + m_7$$

$$g = \bar{y}\bar{z} + \bar{x}y + y\bar{z} = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + \bar{x}y\bar{z} + xy\bar{z} + \bar{x}y\bar{z} \\ = \bar{x}\bar{y}\bar{z} + \bar{x}\bar{y}z + \bar{x}y\bar{z} + xy\bar{z} + xy\bar{z} \\ = m_0 + m_2 + m_3 + m_4 + m_6$$

Part C)

We can compare two  $n$ -bit unsigned numbers  $A = A_{n-1}A_{n-2} \dots A_1A_0$  and  $B = B_{n-1}B_{n-2} \dots B_1B_0$  as shown in the diagram below using  $n$  copies of the same sub-circuit. [4 MARKS]



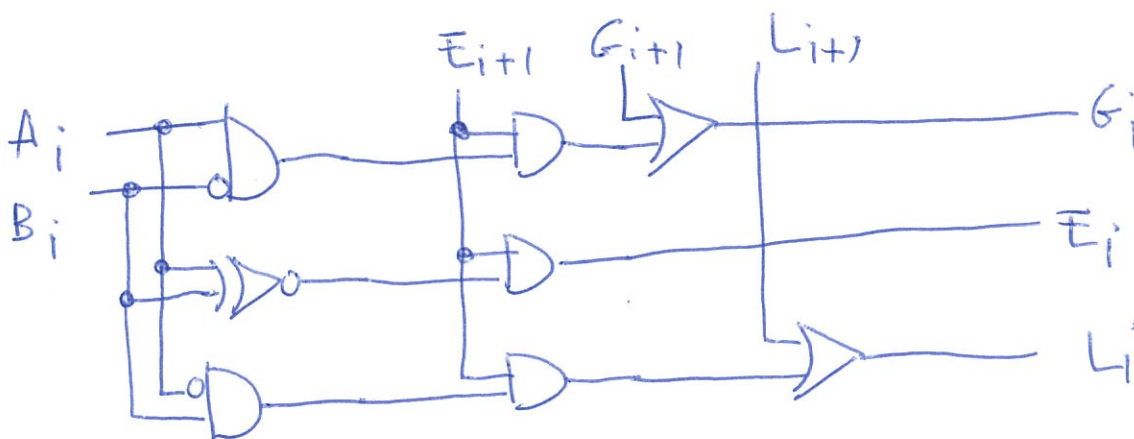
Each sub-circuit has 5 inputs ( $G_{i+1}, E_{i+1}, L_{i+1}, A_i, B_i$ ) and produces 3 outputs ( $G_i, E_i, L_i$ ).  $G_i = 1$  means that  $A > B$  if comparing only the  $i$ -th and larger bits of the numbers.  $E_i = 1$  means that  $A = B$  if comparing only the  $i$ -th and larger bits of the numbers.  $L_i = 1$  means that  $A < B$  if comparing only the  $i$ -th and larger bits of the numbers. Finally, we can tell if  $A > B, A = B, A < B$  by looking at the outputs  $G_0, E_0, L_0$ , respectively.

Draw the required circuitry to implement each sub-circuit. You can use any sort of logic gate you require.

$$G_i = G_{i+1} + E_{i+1} \cdot A_i \cdot \overline{B_i} = \overline{E_i} + L_i$$

$$E_i = E_{i+1} \cdot \overline{A_i \oplus B_i} = \overline{G_i + L_i}$$

$$L_i = L_{i+1} + E_{i+1} \cdot \overline{A_i} \cdot B_i = \overline{G_i + E_i}$$



Question 5: Multi-level circuits and NAND/NOR implementations

Part A)

Implement/draw the logic function  $f = wx' + y'z' + w'yz'$  as a minimized 2-level circuit using only NOR gates. [4 marks]

For 2-level using NOR, need an initial POS (however you get it).

WX

	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	1	0	0	0
10	1	1	1	1

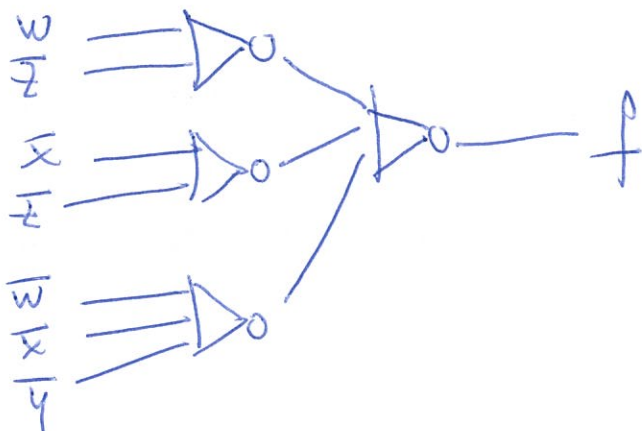
Annotations from image:  
 $w + \bar{z}$  (points to the top row of 0s)  
 $\bar{w} + \bar{x} + \bar{y}$  (points to the third row of 0s)  
 $\bar{x} + \bar{z}$  (points to the second column of 0s)

$$f = w\bar{x} + \bar{y}\bar{z} + \bar{w}y\bar{z}$$

$$= (w + \bar{z})(\bar{x} + \bar{z})(\bar{w} + \bar{x} + \bar{y})$$

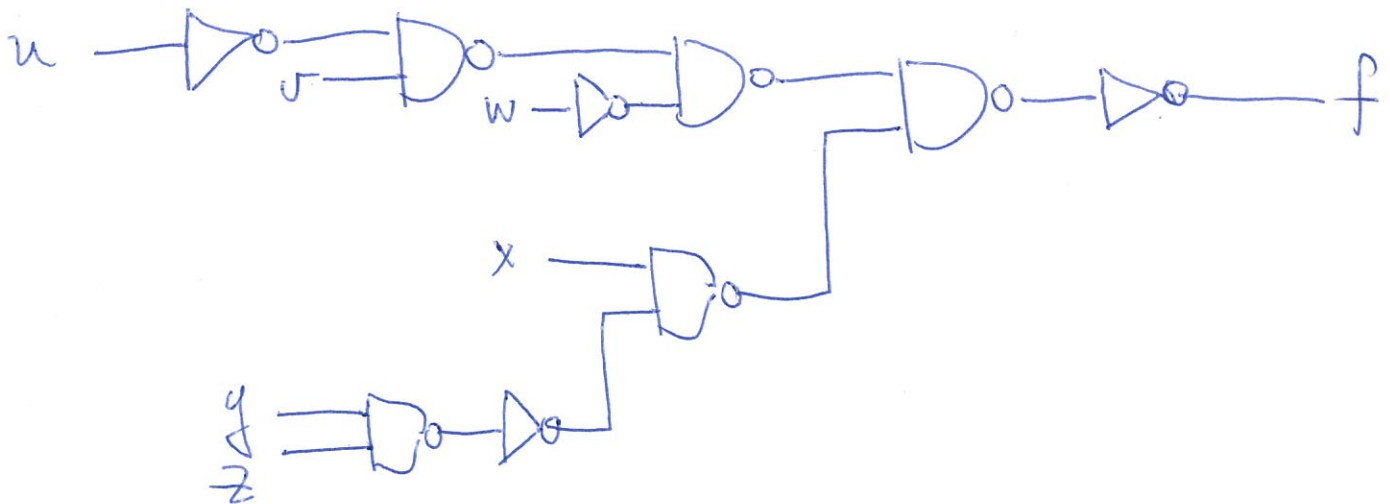
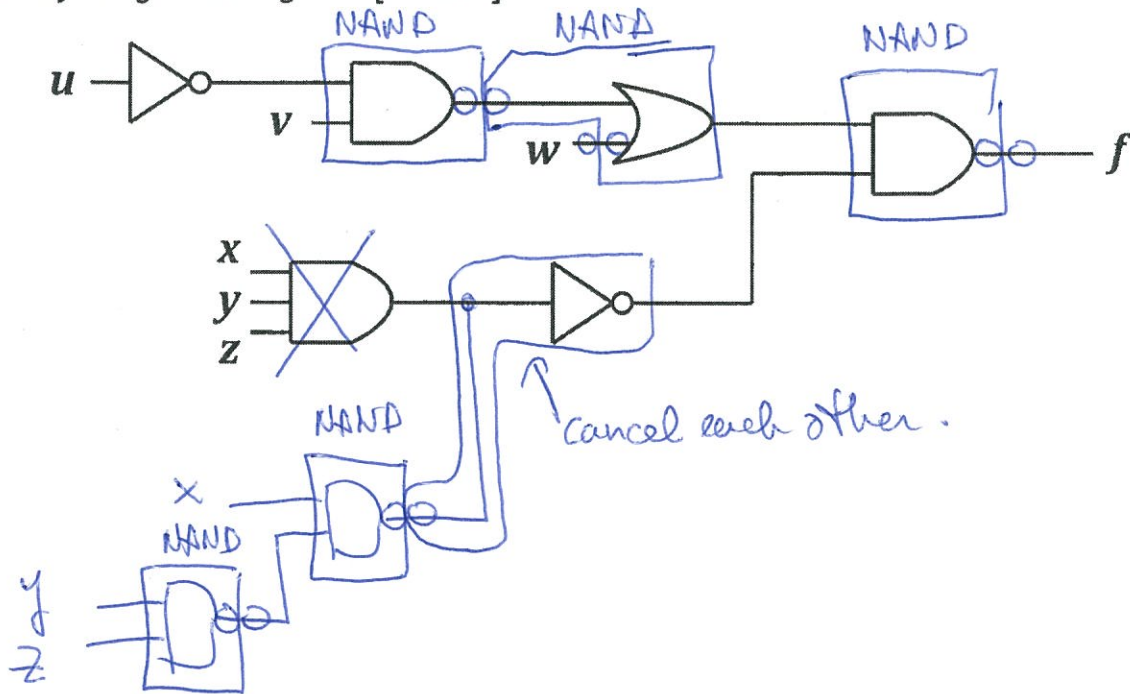
$$= \overline{(w + \bar{z})(\bar{x} + \bar{z})(\bar{w} + \bar{x} + \bar{y})}$$

$$= \overline{(w + \bar{z}) + (\bar{x} + \bar{z}) + (\bar{w} + \bar{x} + \bar{y})}$$



Part B)

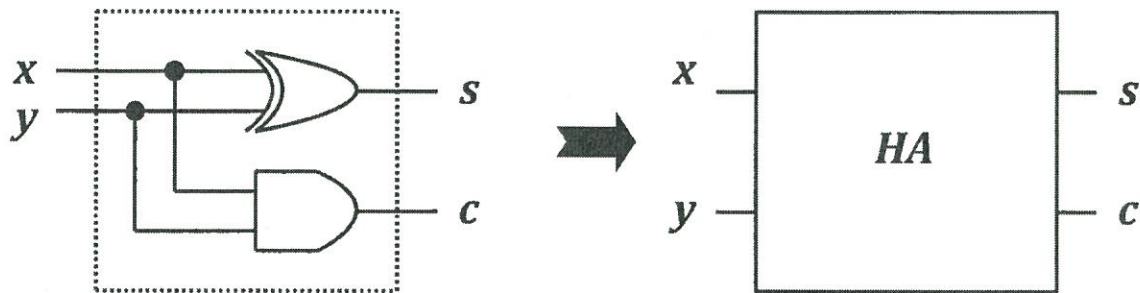
Convert the following circuit to one that uses only 2-input NAND gates and inverters. Inputs are available only in un-complemented form so be sure to show any inversions at inputs explicitly using inverter gates. [4 marks]





Part C)

Shown below is the circuit for a half-adder (HA).



Consider the following 4 logic equations:  $D = A \oplus B \oplus C$ ,  $E = A'BC + AB'C$ ,  $F = ABC' + (A' + B')C$ , and  $G = ABC$ . Show that the 4 logic equations for  $D, E, F$  and  $G$  can be implemented using only 3 half adders. [4 MARKS]

$$D = A \oplus B \oplus C = (A \oplus B) \oplus C \quad (\text{associative})$$

$$E = \bar{A}BC + AB'C$$

$$= C(\bar{A}B + AB') = (A \oplus B) \cdot C$$

$$F = ABC' + (\bar{A} + \bar{B})C$$

$$= ABC' + \bar{A}BC + \bar{B}AC$$

$$= (AB) \oplus C$$

$$G = ABC = (AB) \cdot C \quad (\text{associative})$$

