UNIVERSITY OF WATERLOO

# University of Waterloo
# Midterm Examination

Term: Winter Year: 2017

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| Student Name: | |
| UW Student ID Number: | |

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| Course Abbreviation and Number: | ECE 124 |
| Course Title: | Digital Circuits |
| Instructor(s): | Andrew Kennings |
| Sections(s): | ☐ LEC 001 - ECE (12:30-1:20 lectures) |
| | ☐ LEC 002 - SE (9:30-10:20 lectures) |

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| Date of Exam: | Wednesday, February 15, 2017 |
| Time Period: | Start time: 2:30pm End time: 4:00pm |
| Duration of Exam: | 1.5 hours |
| Location: | RCH 103, RCH 301, RCH 302, STC 0020 |
| Number of Exam Pages: | 13 |
| Exam Type: | Closed Book |
| Additional Materials Allowed: | Electronic calculator (any type) |

| Question | Score | Question | Score |
|---|---|---|---|
| 1) | /12 | 3) | /16 |
| 2) | /14 | 4) | /18 |
| | | Total | /60 |

## Instructions

1. Answer all questions.
2. The examination is a closed book examination.
3. Electronic calculators are allowed.
4. Clearly show all steps used in the solution process unless stated otherwise. No marks will be given for final answers unless accompanied by a correct solution method.
5. You may use the back of the examination pages if you need extra space.

**Question 1:** Each part of this question is multiple choice. Each part has only **one correct answer**. A correct answer will receive full marks while an incorrect answer will receive zero marks.

**Part (a)** (**2 Marks**) On the front page of this midterm examination, I remembered to write my name (first and last), ID number and correctly identify which lecture section I am enrolled in.

(A) True
(B) False

**Your answer is:** [ ]

**Part (b)** (**2 Marks**) The logic function $f = a'b' + a'c + bc$ can be simplified to:

(A) $f = a'b'$
(B) $f = bc$
(C) $f = a'c$
(D) $f = a'c + bc$
(E) $f = a'b' + a'c$
(F) $f = a'b' + bc$

**Your answer is:** [ ]

**Part (c)** (**2 Marks**) Assume that you have any type of logic gate available. Assume that inputs are available **uncomplemented only** (this means that if $x$ is an input, only $x$ is available as an input and if $x'$ is required, you would need an inverter). The fewest number of gates required to implement the 3-input function $f = ((x + y)z' + z + xy)'$ is:

(A) 0
(B) 1
(C) 2
(D) 3
(E) 4

**Your answer is:**

**Part (d)** (**2 Marks**) Assume you are given the 12 bits $110000110101_2$. You are told this represents an unsigned integer. The value of the integer is:

(A) 3125
(B) $-1077$
(C) 971
(D) $-971$

**Your answer is:**

**Part (e)** (**2 Marks**) Assume you are given the 12 bits $110000110101_2$. You are told this represents an signed integer and that negative values are represented using 2s complement. The value of the integer is:

(A) $3125$
(B) $-1077$
(C) $971$
(D) $-971$

**Your answer is:** [ ]

**Part (f)** (**2 Marks**) Assume you have the 3 input logic function $f = f(a, b, c) = \sum(3, 4, 5, 6)$ which is a sum of minterms expression. Let $g = f'$. The proper **product of maxterms** representation for $g$ is:

(A) $\sum(3, 4, 5, 6)$
(B) $\sum(1, 2, 7)$
(C) $\Pi(1, 2, 7)$
(D) $\Pi(3, 4, 5, 6)$

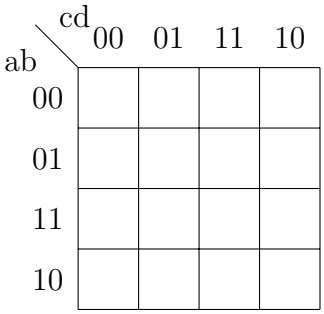
**Your answer is:** [ ]

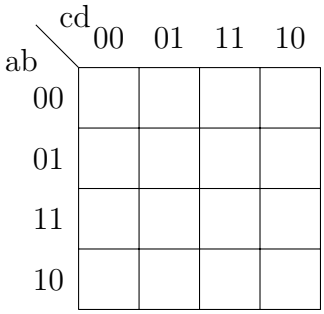
**Question 2:**

**Part (a)** (**6 Marks**) Consider the 3-input logic function $f = (ab)'c + a'c'$. Express $f$ as both a **sum of minterms** and as a **product of maxterms**. You must write out all minterms and all maxterms in full — do **not** use shorthand notation.

**Part (b)** (**8 Marks**) Shown below is a truth table for a 4-input function $f = f(a, b, c, d)$. **Derive** both a **minimized sum of products** expression for $f$ and a **minimized product of sums** expression for $f$. Blank Karnaugh maps are provided if required.

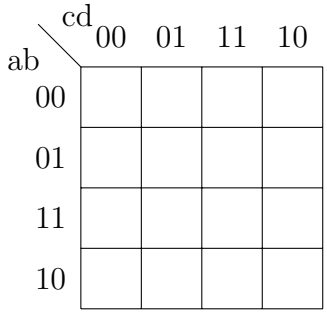
| $a$ | $b$ | $c$ | $d$ | $f$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | $X$ |
| 0 | 0 | 1 | 1 | $X$ |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | $X$ |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |



**Question 3:**

**Part (a)** (**6 Marks**) Assume you are given the 4 input logic function $f = f(a, b, c, d) = b'(a \oplus c) + bd$. **Implement and draw** this function as optimized 2-level circuit using only **NOR** gates. You may assume that the inputs are available **both** complemented and uncomplemented. You may also assume that you have any size of **NOR** gate required. A blank Karnaugh map is shown below if you need it.



**Part (b)** (**10 Marks**) Assume you are given the 5 input logic function $f = f(a, b, c, d, e) = b'd'e' + ace + c'e' + bcde$ which is minimized SOP representation for $f$. **Implement and draw** $f$ as a multi-level circuit using only 2-input **NAND** gates. No **NAND** gate can be used as a **NOT** gate. You may assume that inputs are available both complemented and uncomplemented. **Hint 1:** You might need to consider factoring to eliminate the larger gates. **Hint 2:** The Boolean identify $xb + x'a = (x + a)(x' + b)$ might be useful.

**Question 4:**

**Part (a)** (**6 Marks**) Represent both $(56)_{10}$ and $(79)_{10}$ in base 2 assuming that you have 8 bits available. Subtract $(79)_{10}$ from $(56)_{10}$ by adding the negative of the subtrahend to the minuend. Show all work.

**Part (b)** (**12 Marks**) Assume you require a circuit capable of performing 2-bit division. The four inputs to the circuit are $A = (a_1a_0)$ and $B = (b_1b_0)$. The circuit should perform $A \div B$ and produce as output the quotient $Q = (q_1q_0)$ and the remainder $R = (r_1r_0)$. For example, if $a_1a_0 = 10$ and $b_1b_0 = 11$, then the output should be $q_1q_0 = 00$ and $r_1r_0 = 10$ since $2 \div 3$ is 0 with remainder 2.

When $b_1b_0 = 00$ which means divison by zero, the remainder should always be $r_1r_0 = 11$ but the quotient $q_1q_0$ can have any combination of values.

Based on this description, **design and draw** a circuit capable of performing 2-bit division. Implement all outputs as minimized $SOP$ expressions. Blank Karnaugh maps are provided if you need them.