Introduction to Logic and Computer Design

Final Exam

ID : NAME :

1. Design a synchronous counter that goes through the sequence

   1 3 5 7 4 2 0 6 and repeat

   Using D flip flops.

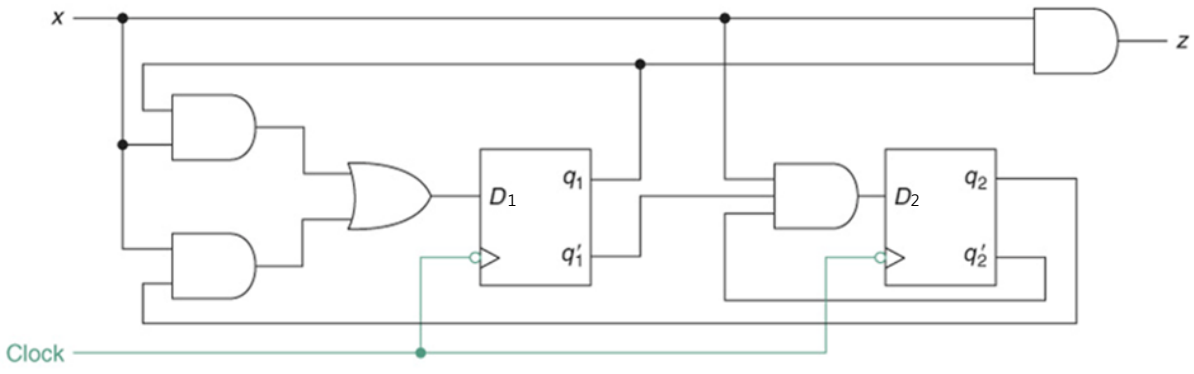
2. Draw a State diagram

   A Moore system, the output of which is 1 iff there have been two or more consecutive 1's or three or more consecutive 0's (five state)

   x 0 0 0 0 1 0 1 1 0 0 1 1 1 0 0 0 1 0

   z ? ? ? 1 1 0 0 0 1 0 0 0 1 1 0 0 1 0 0 0

3. In Following the Block diagram(Mealy model)



   (a) Boolean equation (D_1, D_2, Z)
   (b) Write a State table
   (c) Draw a State diagram

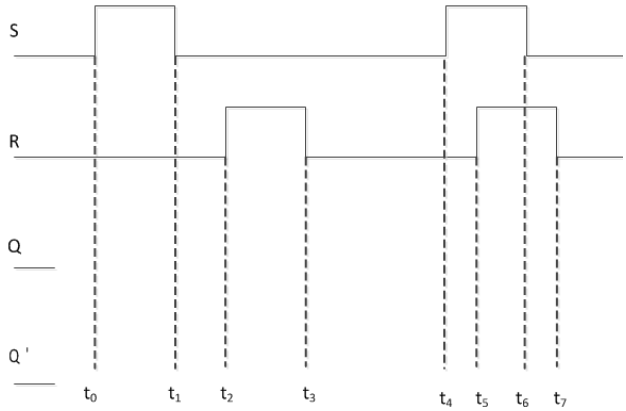
4. Ordered Binary Decision Diagram(OBDD)

(a) Explain the purpose of Ordered Binary Decision Diagram(OBDD)

(b) Draw a OBBD (function f) Sequence b -> c -> a -> d

$$f = abc + b'd + c'd$$

5. SR Latch (a) Draw a Logic Schematic (b) Wirte a Truth table (c) Complete Timing Diagram (Gate unit Delay = 1.4)



6. For each of the following state tables, design the system using JK flip flops

A B	A* B*		z	
	x=0	x=1	x=0	x=1
0 0	1 0	1 1	0	0
0 1	0 0	0 1	0	0
1 0	0 1	1 1	1	0
1 1	0 0	0 0	1	1

Show the equations for each and a block diagram for the JK design (using AND , OR, and NOT gates)