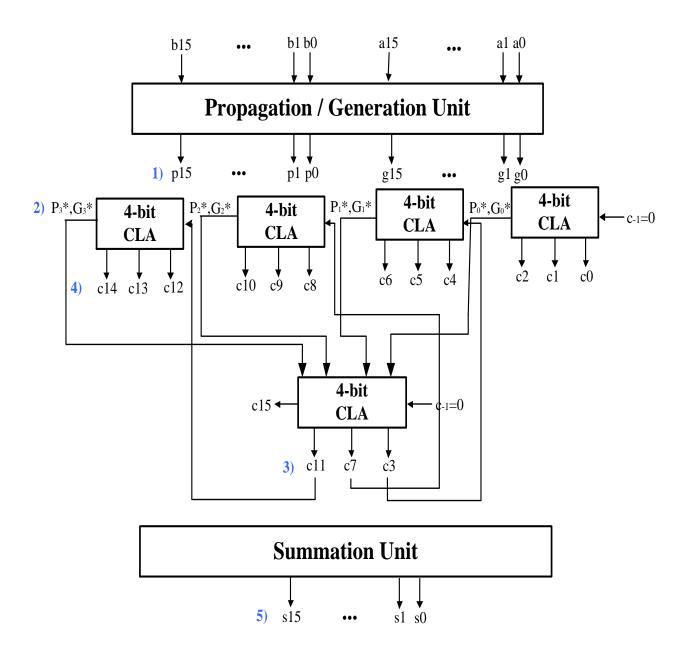
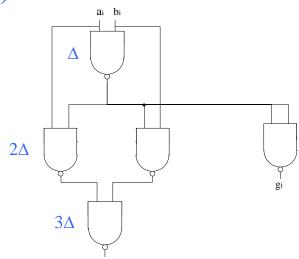
2-Level 16-bit Carry Look-Ahead Adder

Assume that 4-bit Carry Look-Ahead(CLA) units are available for parallel adder construction.

$$\mathbf{A} = a_{15} a_{14} \dots a_0, \qquad \mathbf{B} = \ b_{15} b_{14} \dots b_0, \qquad \mathbf{G} = g_{15} g_{14} \dots g_0, \qquad P = \ p_{15} p_{14} \dots p_0, \qquad \qquad \mathcal{C}_{-1} = \mathbf{0}$$



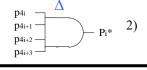
1)



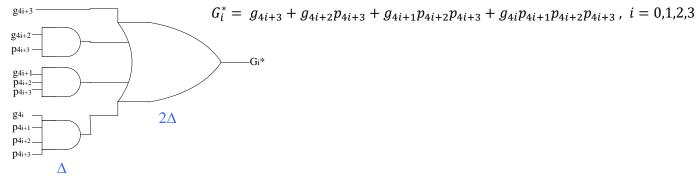
$$g_i = a_i b_i, \quad i = 0,1,2,...,15$$

 $p_i = a_i \bigoplus b_i, \quad i = 0,1,2,...,15$

2)



$$P_i^* = p_{4i}p_{4i+1}p_{4i+2}p_{4i+3}$$
, $i = 0,1,2,3$



3)

$$C_3 = G_0^* + P_0^* C_{-1}$$

$$C_7 = G_1^* + P_1^* C_3 = G_1^* + G_0^* P_1^* + P_0^* P_1^* C_{-1}$$

$$C_{11} = G_2^* + P_2^* C_7 = G_2^* + G_1^* P_2^* + G_0^* P_1^* P_2^* + P_0^* P_1^* P_2^* C_{-1}$$

$$C_{15} = G_3^* + P_3^* C_{11} = G_3^* + G_2^* P_3^* + G_1^* P_2^* P_3^* + G_0^* P_1^* P_2^* P_3^* + P_0^* P_1^* P_2^* P_3^* C_{-1}$$

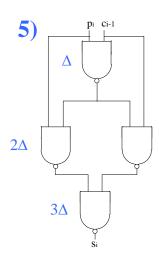
Applying a similar scheme as step 2), the delay of step 3) is also 2Δ .

$$c_{i+1} = g_{i+1} + c_i p_{i+1}, \qquad i = -1,3,7,11$$

$$c_{i+2} = g_{i+2} + g_{i+1} p_{i+2} + c_i p_{i+1} p_{i+2}, \qquad i = -1,3,7,11$$

$$c_{i+3} = g_{i+3} + g_{i+2} p_{i+3} + g_{i+1} p_{i+2} p_{i+3} + c_i p_{i+1} p_{i+2} p_{i+3}, \qquad i = -1,3,7,11$$

Applying a similar scheme as step 2), the delay of step 4) is also 2Δ .



$$s_i = p_i \bigoplus c_{i-1}, \quad i = 0,1,2,...,15$$

Therefore, total time delay of 2-level 16 bit CLA is $3\triangle + 2\triangle + 2\triangle + 2\triangle + 3\triangle = 12\triangle$