CSE3015Introduction to digital circuits, Fall 2018

Midterm Exam

Student Number : Name :

1. (10Pt.) 6-bit two's complement
   For each of the following pairs of integers, subtract the second from the first. Show the operands and the answers in decimal, assuming
   i. The numbers are unsigned
   ii. The numbers are signed (two's complement).
   Indicate overflow where appropriate.
   a. 101010, 100101 b. 110101, 011011

2. (10Pt.) Boolean algebra, simplification of algebraic expression
   Simplify the following functions and show the process
   a. f = wy' + wz + xy' + xz + yz
   b. g =ab + ac + a'd + a'e

3. (10Pt.) manipulation of algebraic functions, karnaugh map
   For the following function, find the minimum SOP expression and the minimum POS expression.
   a. $f(w, x, y, z) = \sum m(0, 2, 5, 7, 8, 10, 11, 13, 15)$
   b. $f(w, x, y, z) = \sum m(1, 3, 5, 8, 9, 15) + \sum d(2, 7, 12, 13)$

4. (20Pt.) 4-bit carry look-ahead adder
   Show the Boolean algebra of Carry-propagate function and Carry-generate function, and draw a logic gate of 4-bit carry look-ahead adder. (Use only gate like AND, OR, NOT, XOR, not block)

5. (10Pt.) Decoder
   a. Show a 4x16 decoder by using 2x4 decoders.
   b. Using a decoder, Show logic diagram for a function of problem 3.a.

6. (10Pt.) Function implementation using MUX
   Implement the function
   $$f(w, x, y) = \sum m(0, 2, 5, 6, 7)$$
   using 2x1 multiplexers

7. (10Pt.)
   Show TR-level circuit of OR gate using PMOS, NMOS

8. (10Pt.) Converter
Design a converter. This converter has 3 digit BCD code input from 0 to 5 and 5 digit output which has (input variable)^2 + 1 (input variable : BCD code with X, Y, Z). Complete the table below and design the B and D circuits of converter.

Digit	X	Y	Z	A	B	C	D	E
0	0	0	0	0	0	0	0	1
1	0	0	1					
2	0	1	0					
3	0	1	1					
4	1	0	0					
5	1	0	1					

9. (10Pt.) delay
Suppose that each component in the following logic circuit has each gate delay. If the state of input A and B is like the following timing diagram, show timing diagram of Q.