CSE3015 Introduction to digital circuits, Fall 2017

Midterm Exam

Student ID number : Name :

1. (10Pt.) 6-bit subtraction
   For the following pair of integers, subtract the second number from the first number. Show the sequence and result. Indicate overflow if it occurs.
   1A. If the numbers are unsigned, 101100, 011100
   1B. If the numbers are signed(2's complement), 010001, 011000

   Ans)

2. (10Pt.) Transistor-level circuit description
   Show Transistor-level circuit of three input (a, b, c) NAND gate and one output F using PMOS, NMOS transistors.

   Ans)

3. (10Pt.) Simplification of Boolean algebraic expression
   Simplify the following functions and show the process briefly.
   3A. f = (a + c)'(b + c') + a + c
   3B. g = (a + b + c)(b' + c + d)(a + c + d)

   Ans)

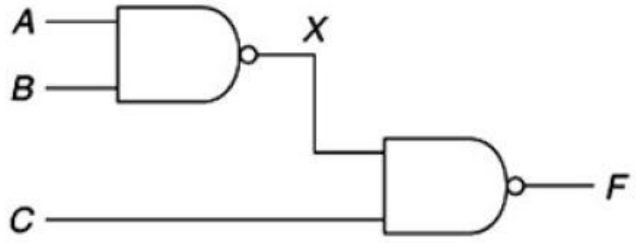
4. (20Pt.) Boolean function
   This is the truth table of function f and g with three inputs (a, b, c).

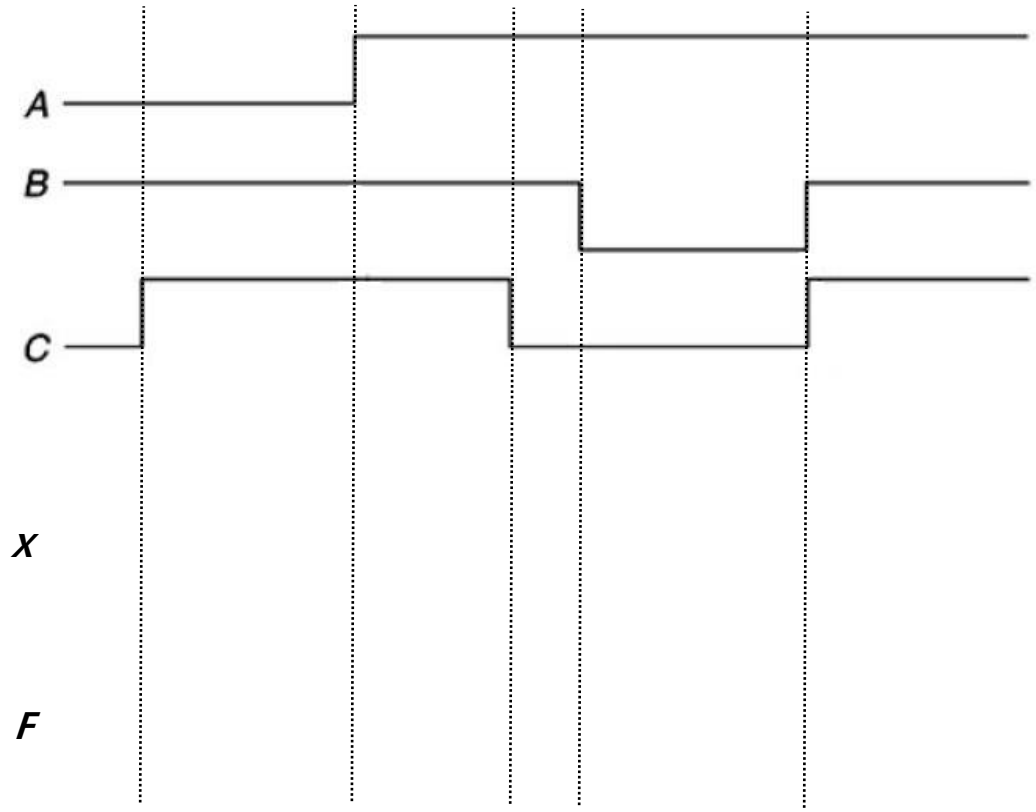
a	b	c	f	g
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

   4A. Obtain minimum SOP of each function using Karnaugh map.
   4B. Obtain minimum POS of each function using Karnaugh map.

   Ans)

5. (10Pt.) Gate delay
The following logic diagram has three inputs and one output F. the internal node is denoted as X. complete the logic and timing transition of X and F for the given transition sequence of A, B, C. (input A starts with 0, input B starts with 1, input C starts with 0.)





6. (20Pt.) Karnaugh map
Obtain Karnaugh map of each function f, g. Then obtain every possible minimum SOP using Karnaugh map. Suppose that d means don't care.

A. $f(a,b,c) = \sum m(0,1,2,5,6,7)$

B. $g(a,b,c,d) = \sum m(5,7,9,11,13,14) + \sum d(2,6,10,12,15)$

Ans)

7. (20Pt.) 4-bit Carry look-ahead adder
The following figure is logic circuit of 4-bit Carry look-ahead adder. Draw logic gates in the box.