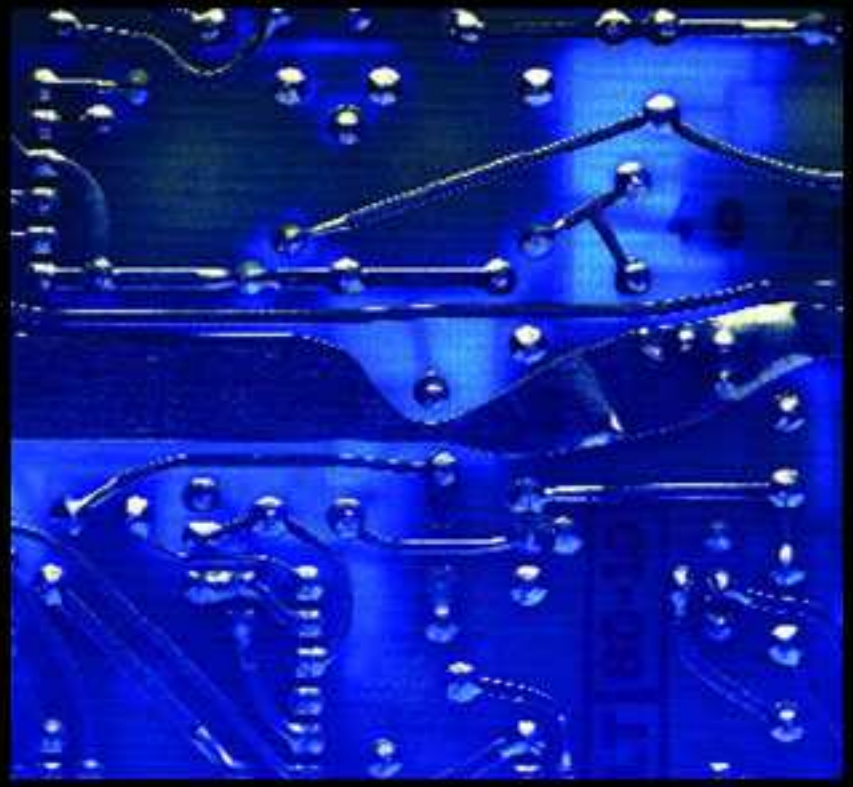
ELECTRONIC DEVICES AND CIRCUIT THEORY

TENTH EDITION



BOYLESTAD

PEARSON

Chapter 3 & 4:
Bipolar Junction Transistors and Applications

Transistor Construction

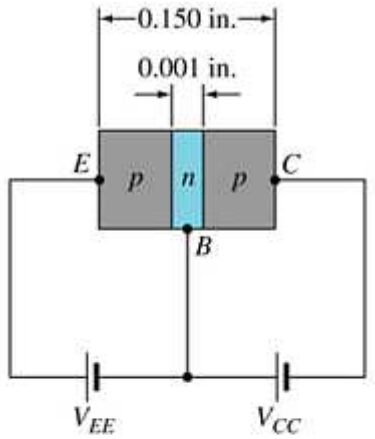
There are two types of transistors:

- *pnp*
- *npn*

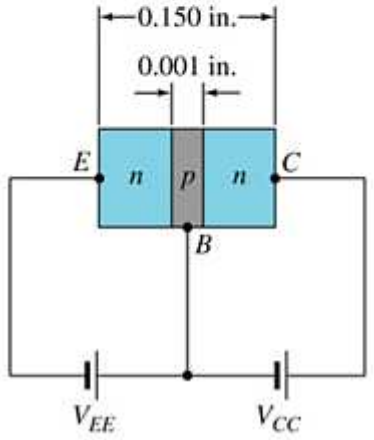
The terminals are labeled:

- **E - Emitter**
- **B - Base**
- **C - Collector**

pnp



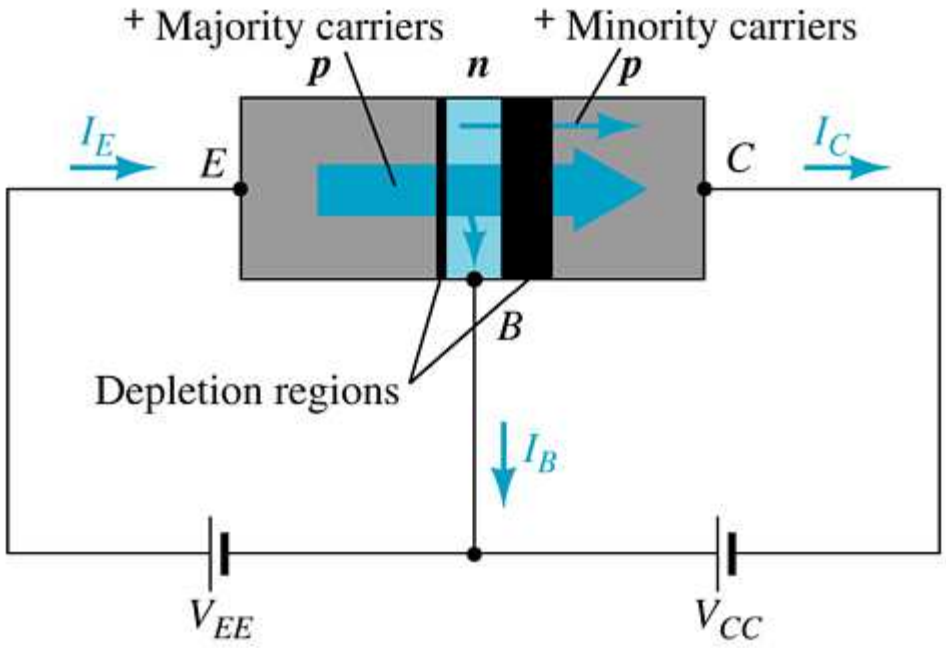
npn



Transistor Operation

With the external sources, V_{EE} and V_{CC}, connected as shown:

- **The emitter-base junction is forward biased**
- **The base-collector junction is reverse biased**



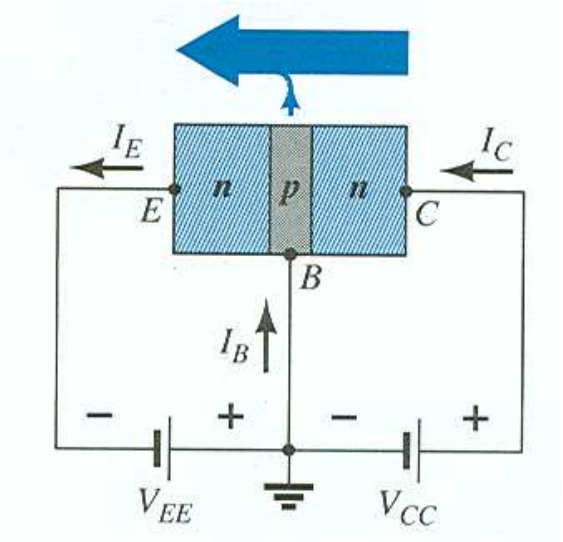
Currents in a Transistor

Emitter current is the sum of the collector and base currents:

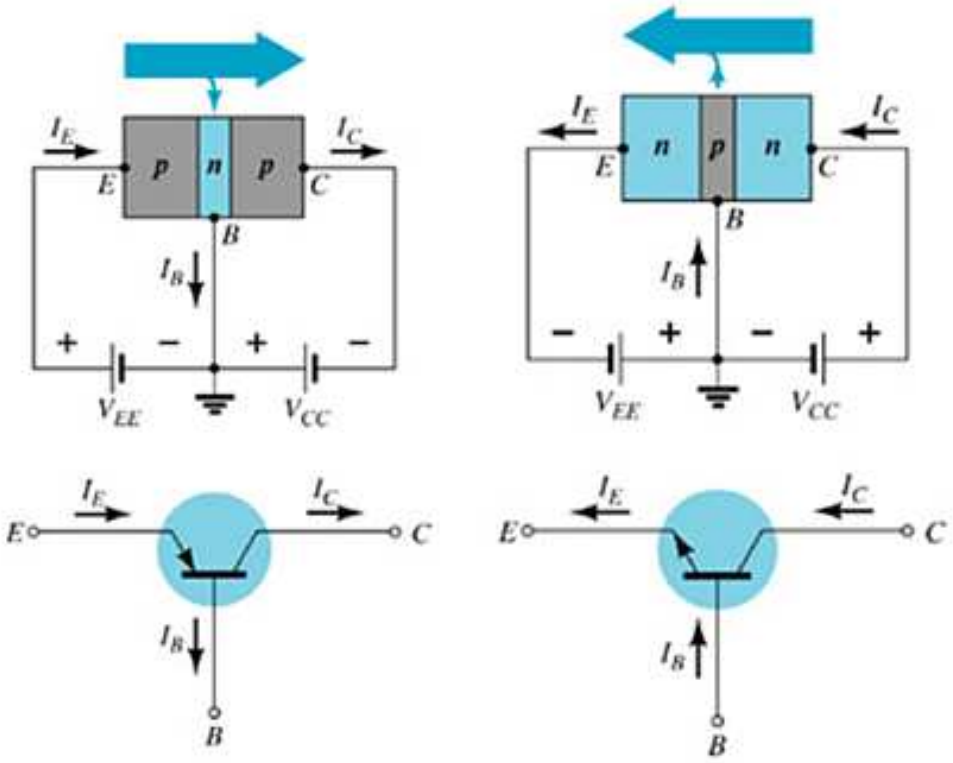
$$I_E = I_C + I_B$$

The collector current is comprised of two currents:

$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$



Common-Base Configuration

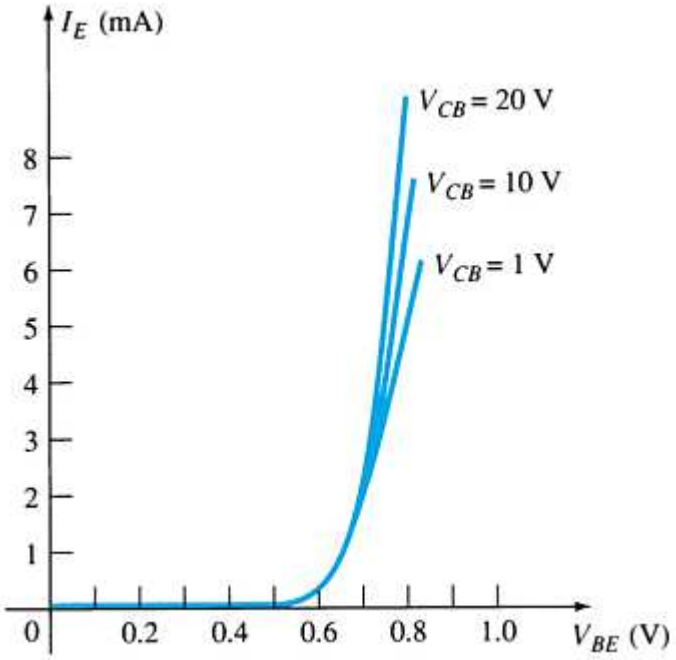


The base is common to both input (emitter–base) and output (collector–base) of the transistor.

Common-Base Amplifier

Input Characteristics

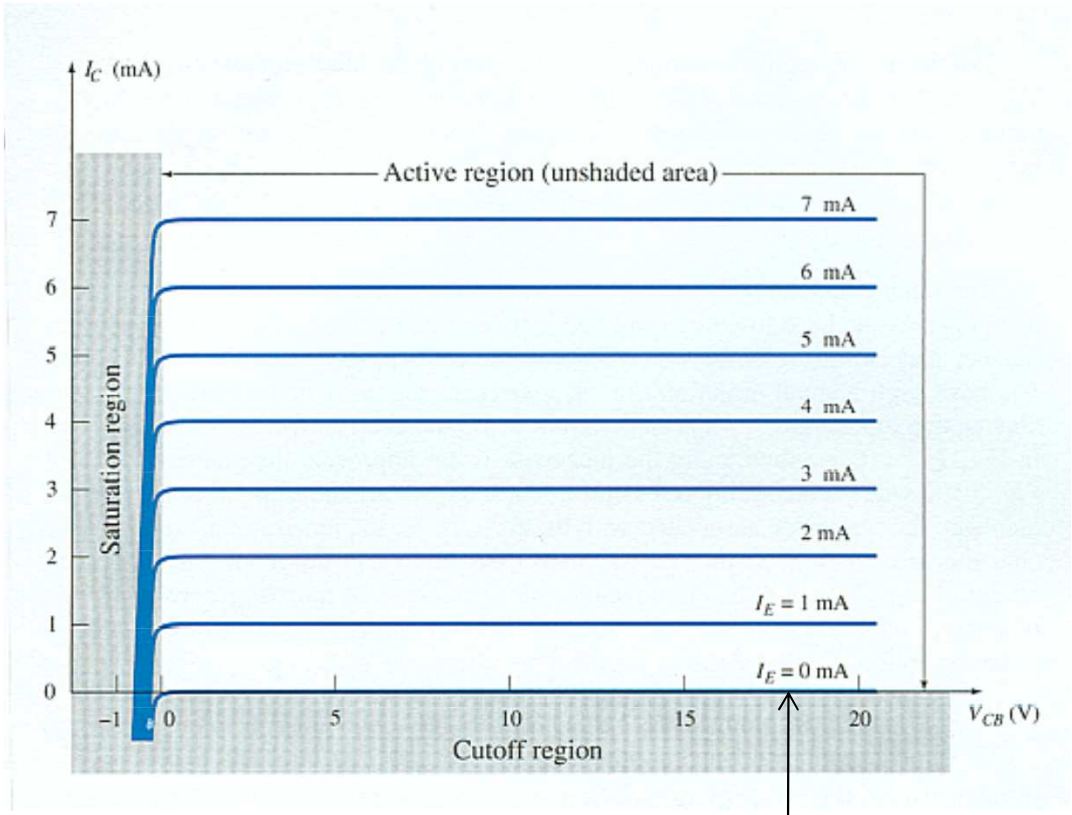
This curve shows the relationship between of input current (I_E) to input voltage (V_{BE}) for three output voltage (V_{CB}) levels.



Common-Base Amplifier

Output Characteristics

This graph demonstrates the output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E).



$$I_{CO} = I_{CBO}$$

Operating Regions

- **Active – Operating range of the amplifier.**
- **Cutoff – The amplifier is basically off. There is voltage, but little current.**
- **Saturation – The amplifier is full on. There is current, but little voltage.**

Regions	Base-Emitter	Collector-Base
Active	Forward-biased	Reverse-biased
Cutoff	Reverse-biased	Reverse-biased
Saturation	Forward-biased	Forward-biased

Approximations

Emitter and collector currents:

$$I_C \cong I_E$$

Base-emitter voltage:

$$V_{BE} = 0.7\ V \quad \text{(for Silicon)}$$

Alpha (α)

Alpha (α) is the ratio of I_C to I_E :

$$\alpha_{\text{dc}} = \frac{I_C}{I_E}$$

Ideally: α = 1
In reality: α is between 0.9 and 0.998

$$I_C = \alpha I_E + I_{CBO}$$

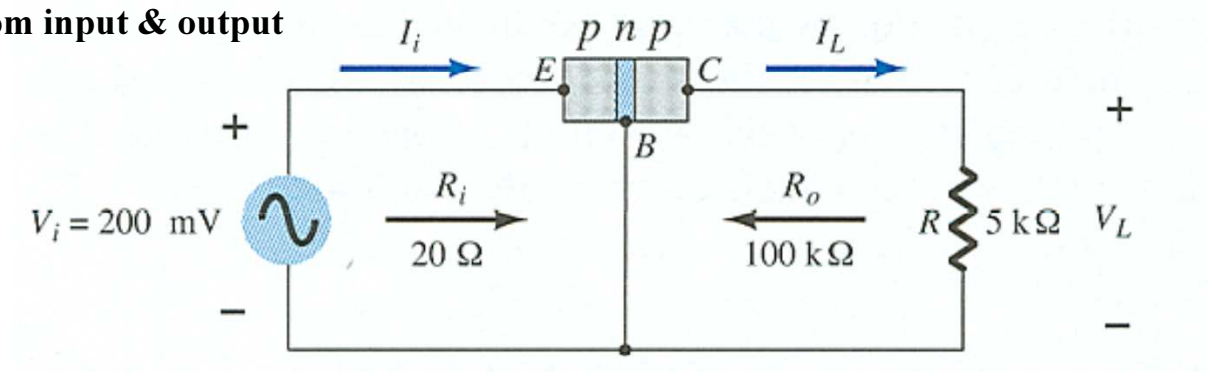
Alpha (α) in the AC mode:

$$\alpha_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}} = \text{constant}$$

Transistor Amplification

Omit DC biasing to demonstrate AC response

Assume R_i and R_o from input & output characteristic curves



Currents and Voltages:

$$I_E = I_i = \frac{V_i}{R_i} = \frac{200\text{mV}}{20\Omega} = 10\text{mA}$$

$$I_C \cong I_E$$

$$I_L \cong I_i = 10\,\text{mA}$$

$$V_L = I_L R = (10\,\text{ma})(5\,\text{k}\Omega) = 50\,\text{V}$$

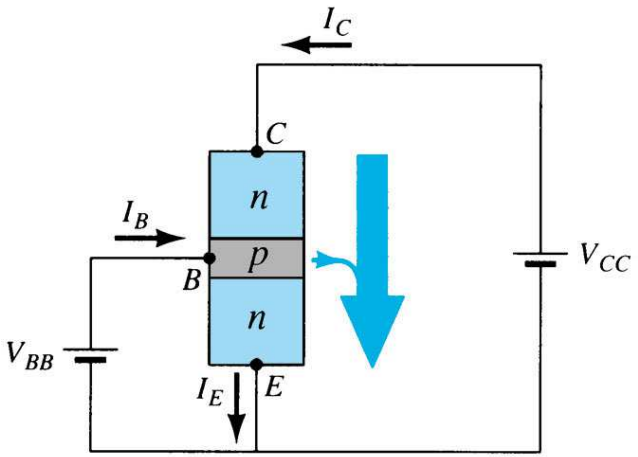
Voltage Gain:

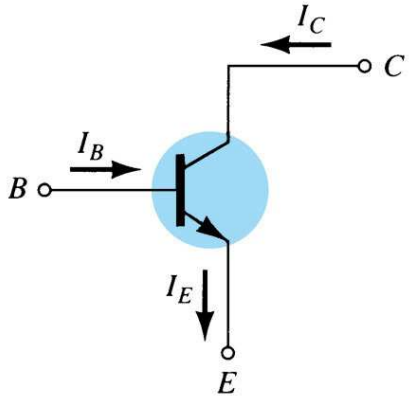
$$A_v = \frac{V_L}{V_i} = \frac{50\text{V}}{200\text{mV}} = 250$$

Common–Emitter Configuration

The emitter is common to both input (base-emitter) and output (collector-emitter).

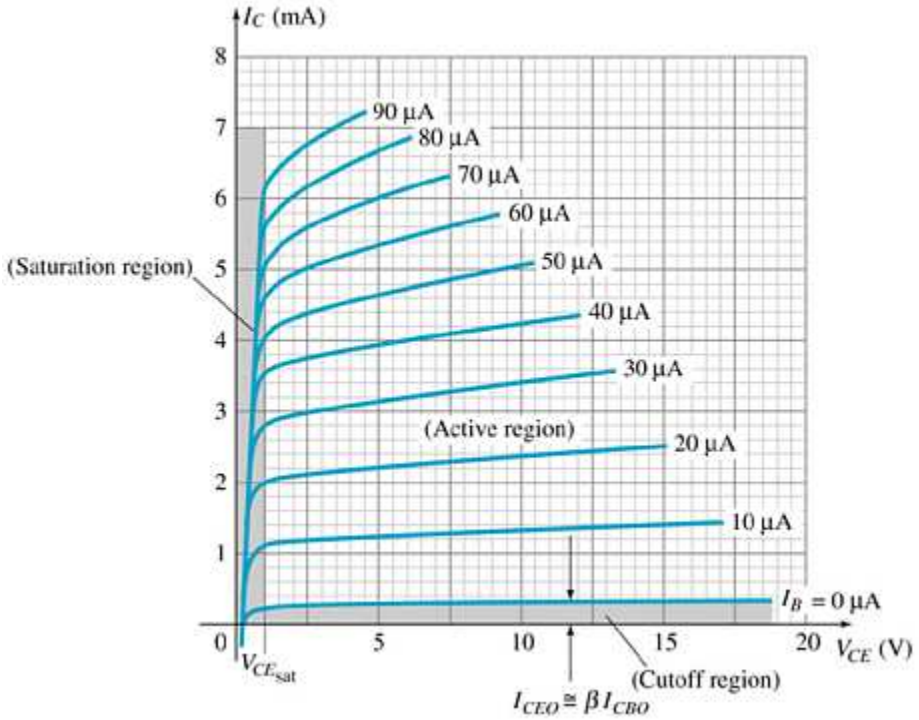
The input is on the base and the output is on the collector.



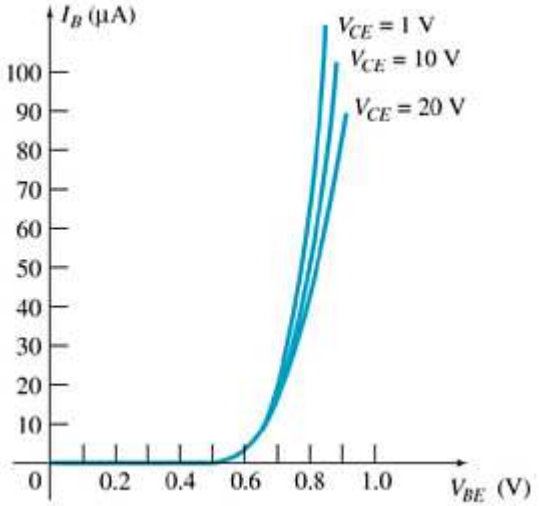


(a)

Common-Emitter Characteristics



Collector Characteristics



Base Characteristics

Common-Emitter Amplifier Currents

Ideal Currents

$$I_E = I_C + I_B \qquad I_C = \alpha I_E$$

Actual Currents

$$I_C = \alpha I_E + I_{CBO}$$ **where I_{CBO} = minority collector current**

I_{CBO} is usually so small that it can be ignored, except in high power transistors and in high temperature environments.

When $I_B = 0\ \mu A$ the transistor is in cutoff, but there is some minority current flowing called I_{CEO}.

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha}\bigg|_{I_B = 0\,\mu A}$$

Beta (β)

β represents the amplification factor of a transistor. (β is sometimes referred to as h_{fe}, a term used in transistor modeling calculations)

In DC mode:

$$\beta_{\text{dc}} = \frac{I_C}{I_B}$$

In AC mode:

$$\beta_{\text{ac}} = \frac{\Delta I_C}{\Delta I_B}\bigg|_{V_{CE}=\text{constant}}$$

Beta (β)

Determining β from a Graph

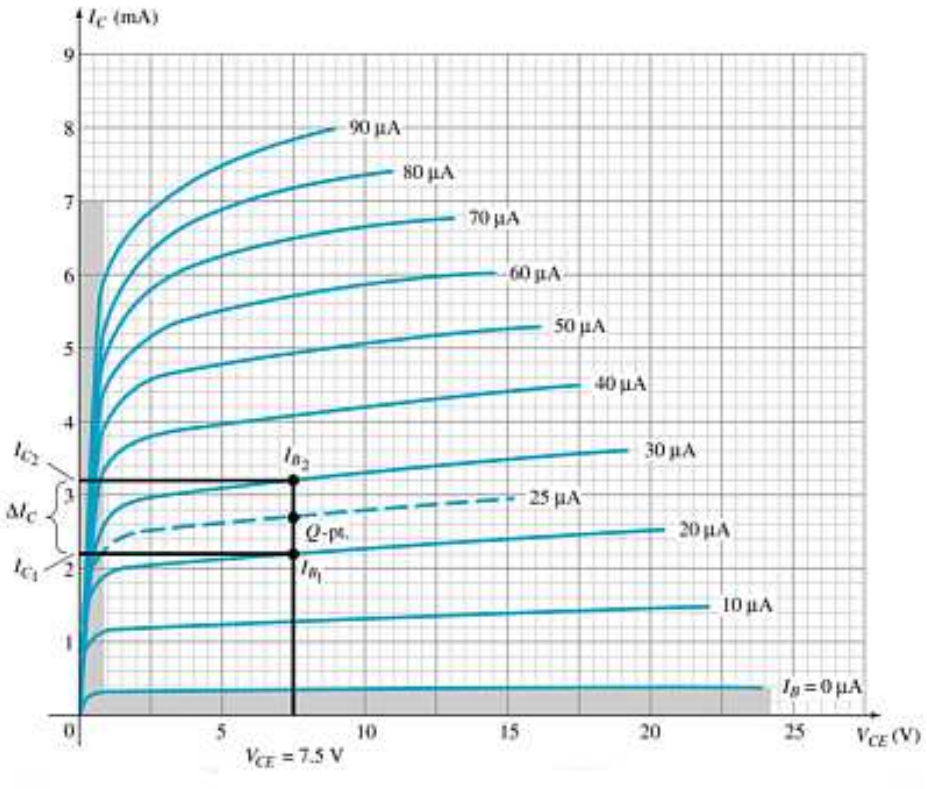
$$\beta_{AC} = \frac{(3.2\,\text{mA} - 2.2\,\text{mA})}{(30\,\mu\text{A} - 20\,\mu\text{A})}$$

$$= \frac{1\,\text{mA}}{10\,\mu\text{A}}\bigg|_{V_{CE}=7.5}$$

$$= 100$$

$$\beta_{DC} = \frac{2.7\ \text{mA}}{25\ \mu\text{A}}\bigg|_{V_{CE}=7.5}$$

$$= 108$$



Both β values are usually reasonably close and are often used interchangeably

Beta (β)

Relationship between amplification factors β and α

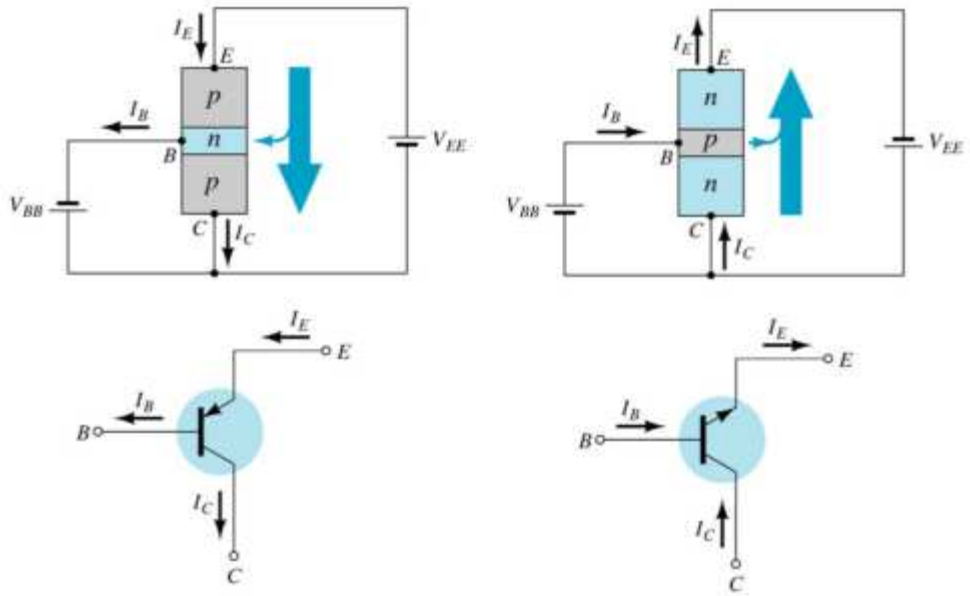
$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{\alpha - 1}$$

Relationship Between Currents

$$I_C = \beta I_B \qquad I_E = (\beta + 1) I_B$$

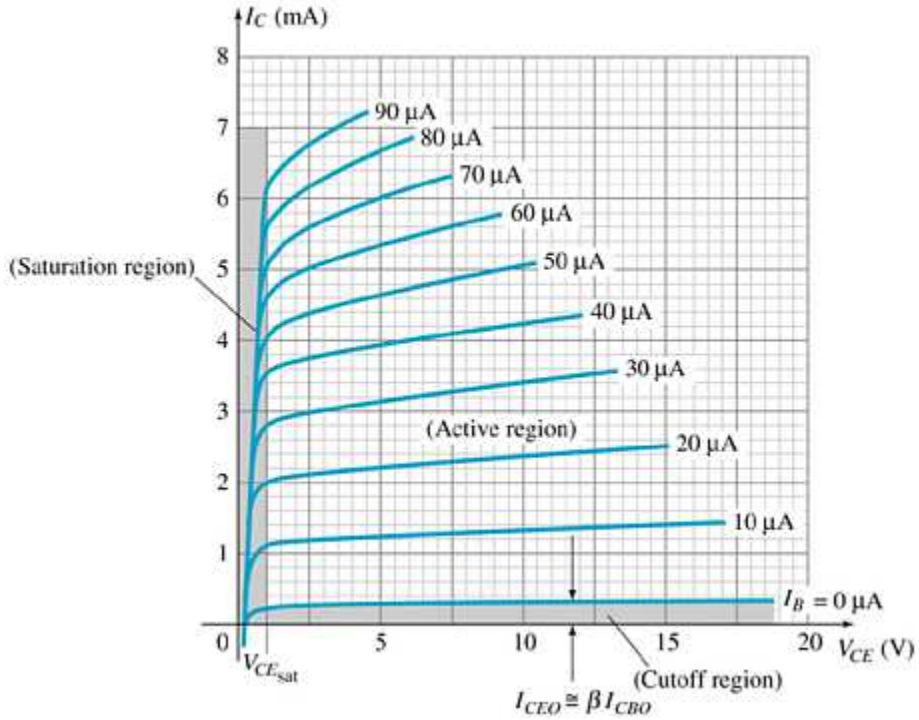
Common–Collector Configuration

The input is on the base and the output is on the emitter.



Common–Collector Configuration

The characteristics are similar to those of the common-emitter configuration, except the vertical axis is I_E.

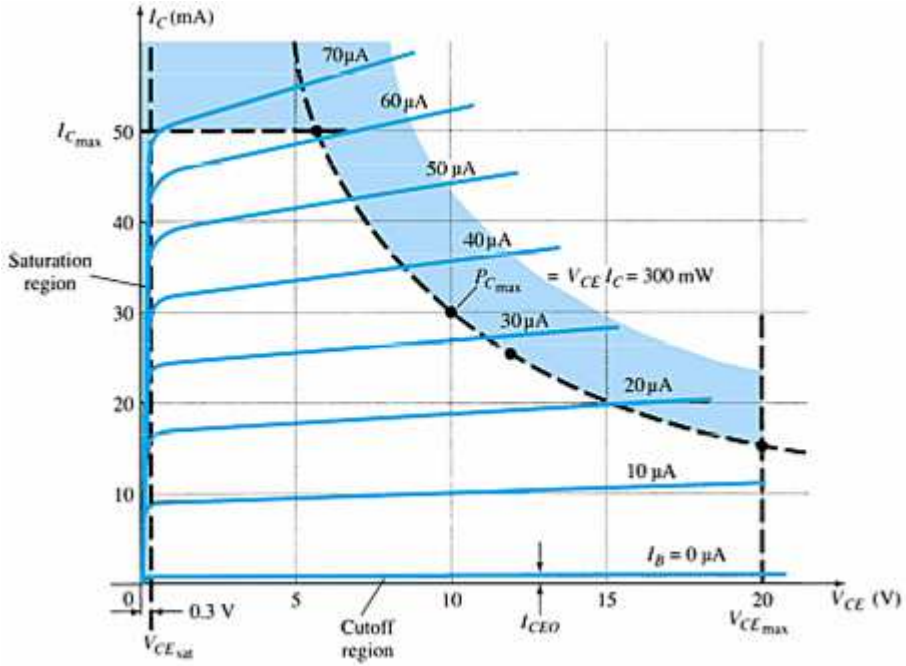


Operating Limits for Each Configuration

V_{CE} is at maximum and I_C is at minimum ($I_{Cmax} = I_{CEO}$) in the cutoff region.

I_C is at maximum and V_{CE} is at minimum ($V_{CE\ max} = V_{CEsat} = V_{CEO}$) in the saturation region.

The transistor operates in the active region between saturation and cutoff.



Power Dissipation

Common-base:

$$P_{Cmax} = V_{CB}I_C$$

Common-emitter:

$$P_{Cmax} = V_{CE}I_C$$

Common-collector:

$$P_{Cmax} = V_{CE}I_E$$

Transistor Specification Sheet

MAXIMUM RATINGS

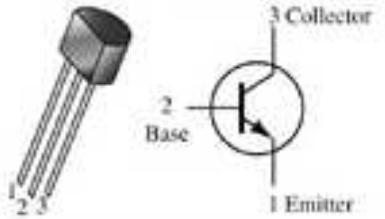
Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25^\circ C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

2N4123

CASE 29-04, STYLE 1
TO-92 (TO-226AA)



GENERAL PURPOSE
TRANSISTOR
NPN SILICON

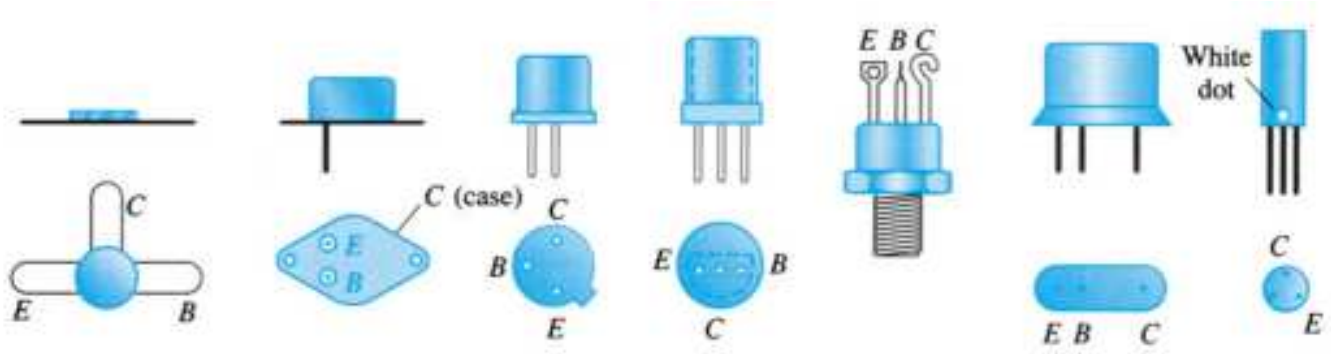
Transistor Specification Sheet

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_E = 0)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) (I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	50 25	150 –	–
Collector-Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{BE(sat)}$	–	0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	250		MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 100 MHz)	C_{obo}	–	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	C_{ibo}	–	8.0	pF
Collector-Base Capacitance (I_E = 0, V_{CB} = 5.0 V, f = 100 kHz)	C_{cb}	–	4.0	pF
Small-Signal Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	50	200	–
Current Gain – High Frequency (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz) (I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	h_{fe}	2.5 50	– 200	–
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k ohm, f = 1.0 kHz)	NF	–	6.0	dB

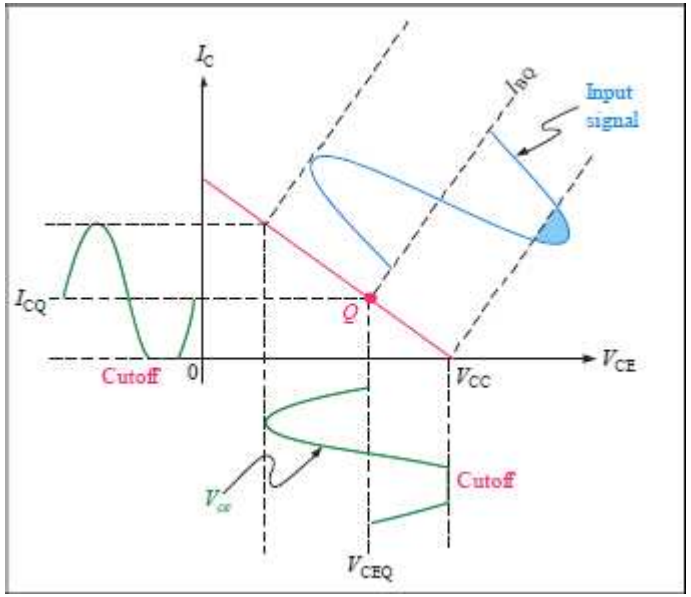
(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%

Transistor Terminal Identification



Biasing

Biasing: **The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.**



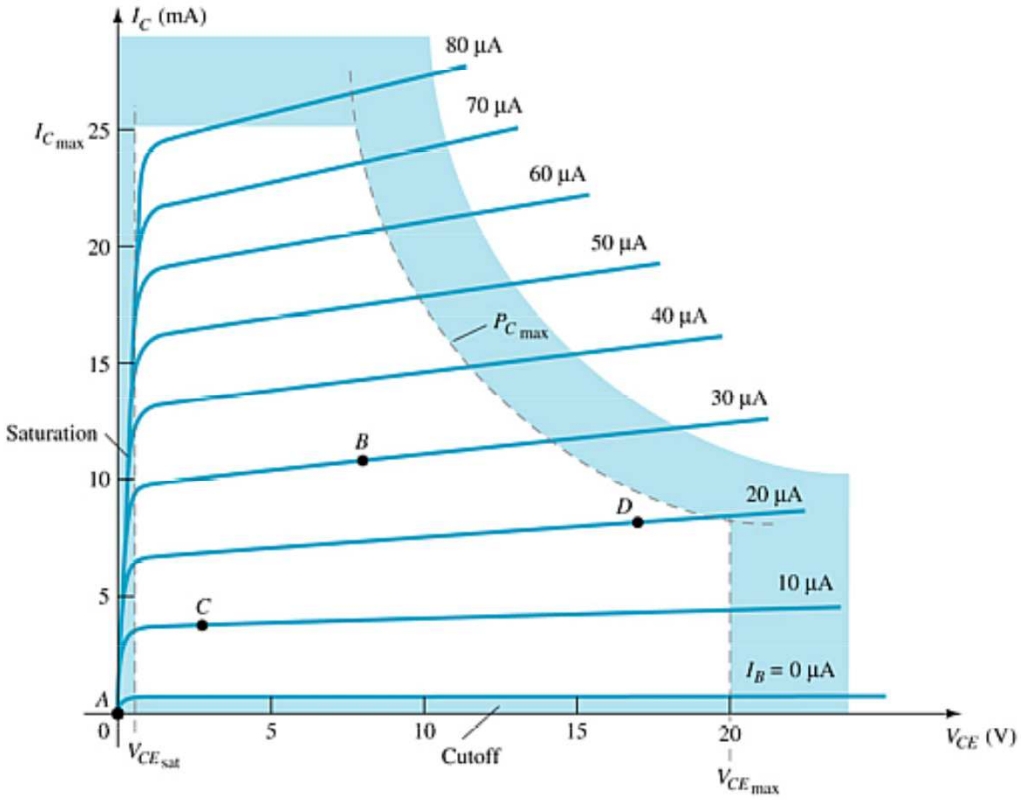
$$V_{BE} = 0.7\,V$$

$$I_E = (\beta + 1)I_B \cong I_C$$

$$I_C = \beta I_B$$

Operating Point

The DC input establishes an operating or *quiescent point* called the *Q-point*.



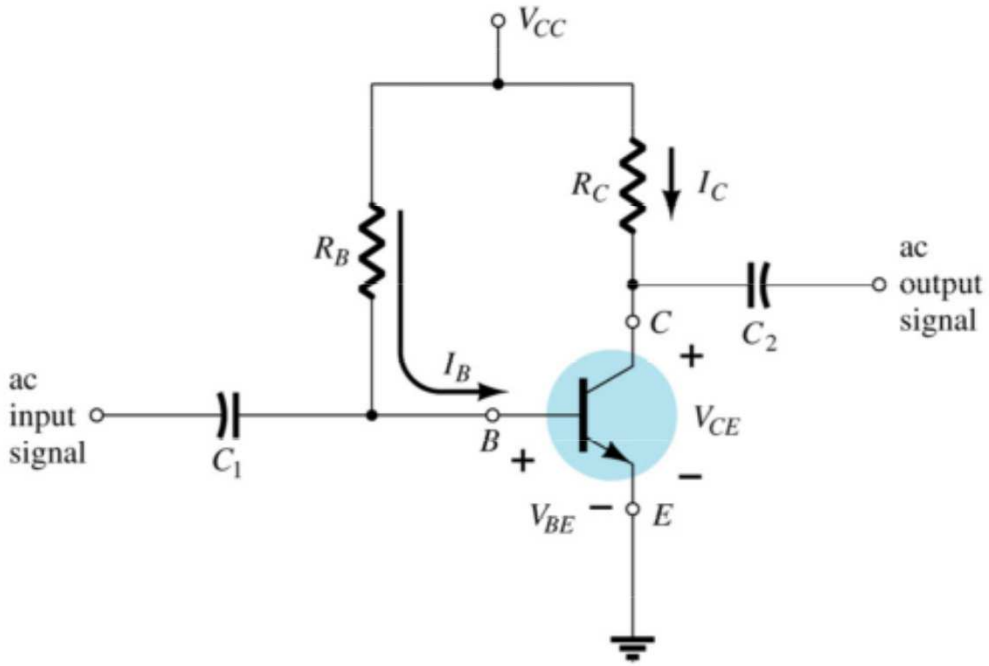
The Three States of Operation

- **Active or Linear Region Operation**
  - Base–Emitter junction is forward biased
  - Base–Collector junction is reverse biased
- **Cutoff Region Operation**
  - Base–Emitter junction is reverse biased
- **Saturation Region Operation**
  - Base–Emitter junction is forward biased
  - Base–Collector junction is forward biased

DC Biasing Circuits

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback

Fixed Bias



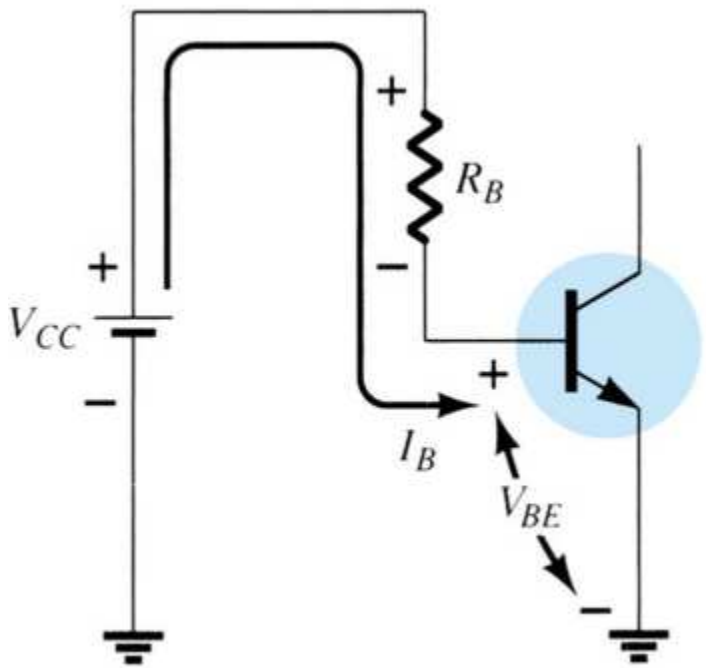
The Base-Emitter Loop

From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



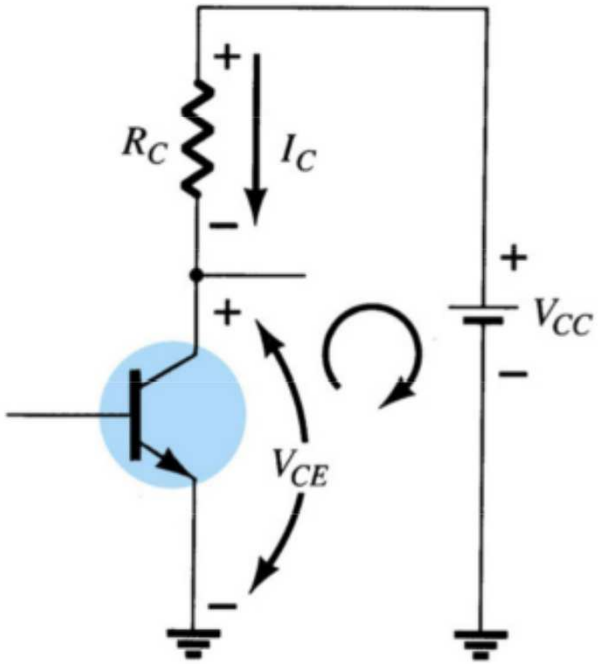
Collector-Emitter Loop

Collector current:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$



Saturation

When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

$$V_{CE} \cong 0\,V$$

This approximation is equivalent to move the region below V_{CEsat} of the output curves to align on the output current axis.

Load Line Analysis

The end points of the load line are:

I_{Csat}

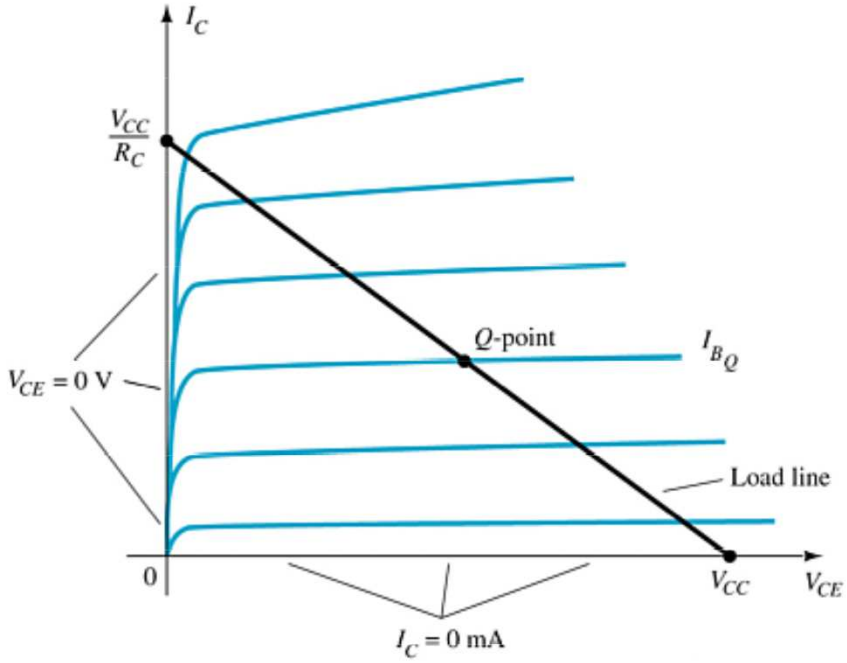
$I_C = V_{CC} / R_C$

$V_{CE} = 0$ V

$V_{CEcutoff}$

$V_{CE} = V_{CC}$

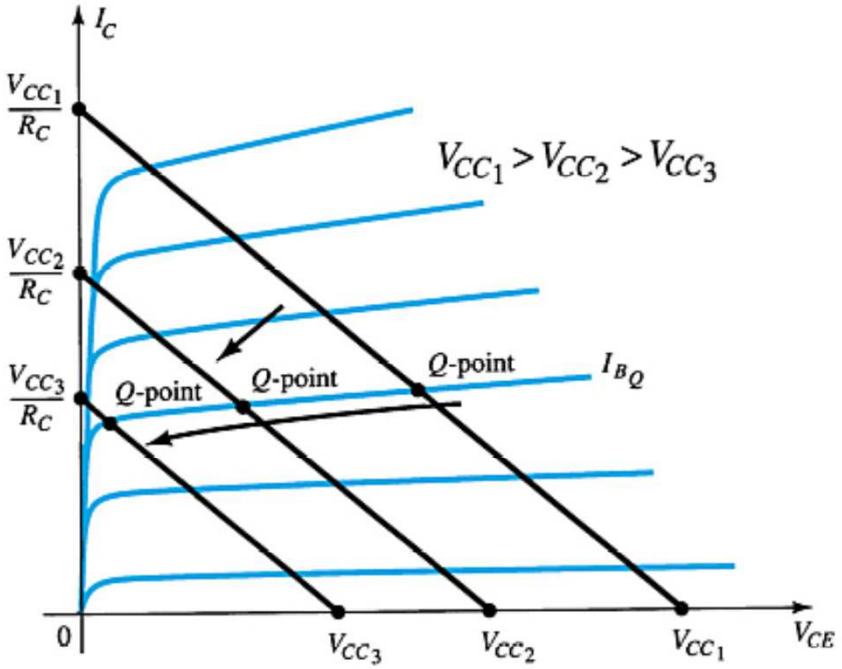
$I_C = 0$ mA



The *Q*-point is the operating point:

- **where the value of R_B sets the value of I_B**
- **that sets the values of V_{CE} and I_C**

Circuit Values Affect the Q-Point



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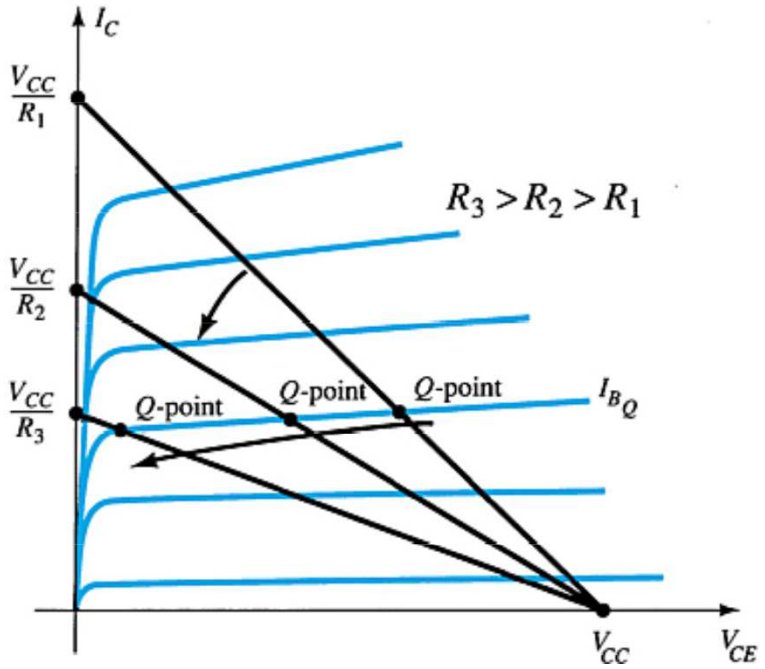
Circuit Values Affect the Q-Point



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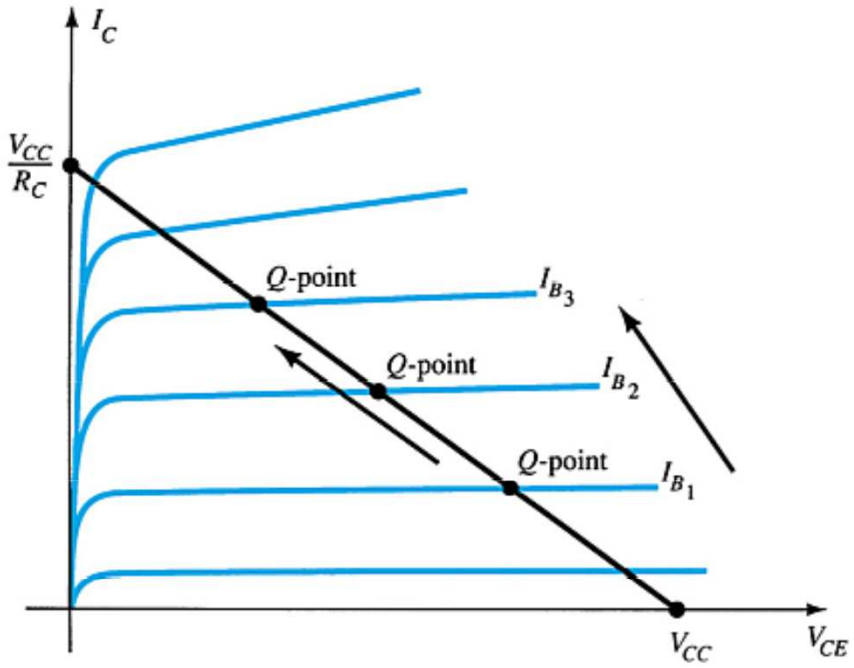
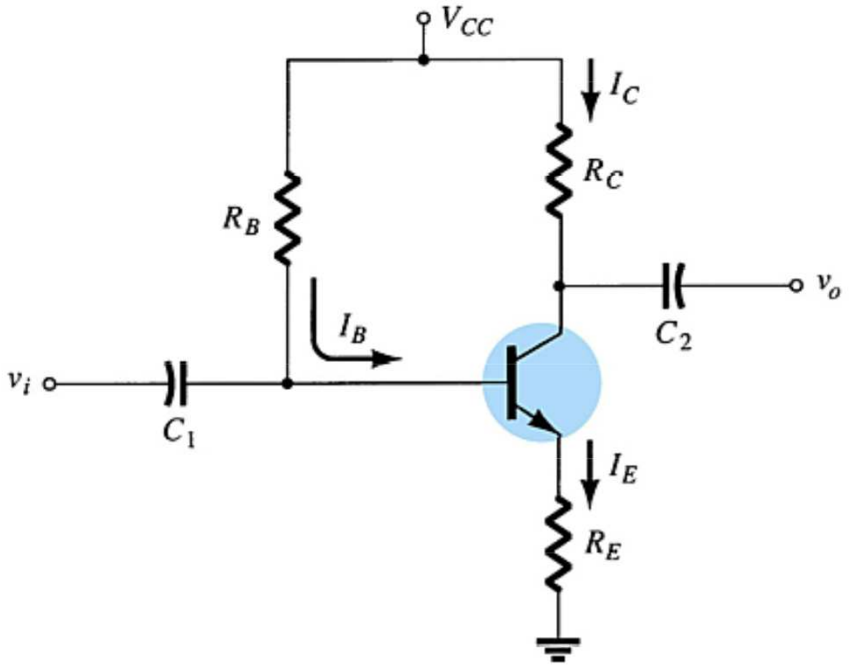
Circuit Values Affect the Q-Point



Emitter-Stabilized Bias Circuit

Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit.



Base-Emitter Loop

From Kirchhoff's voltage law:

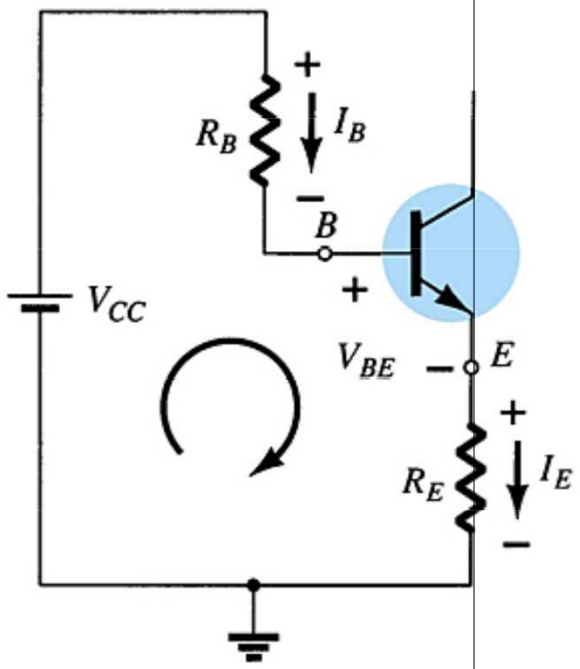
$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



Collector-Emitter Loop

From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

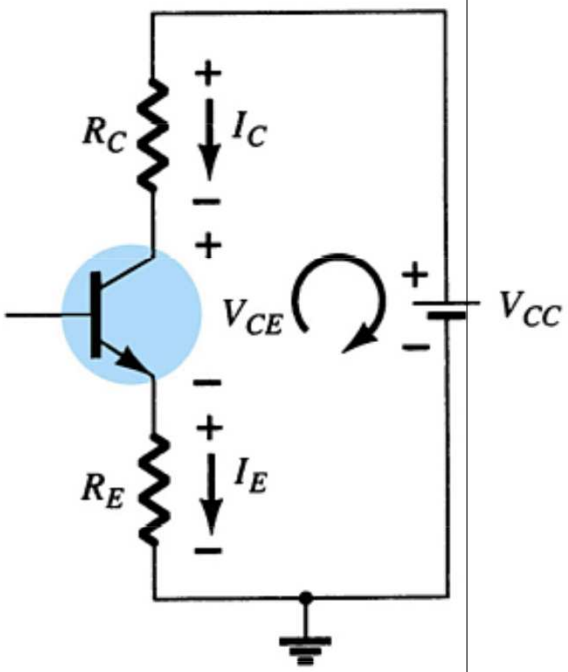
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$



Improved Biased Stability

Stability **refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.**

Adding RE to the emitter improves the stability of a transistor.

Fixed-bias circuit

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

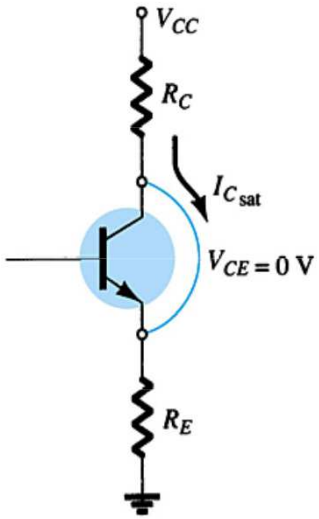
Emitter-stabilized bias circuit

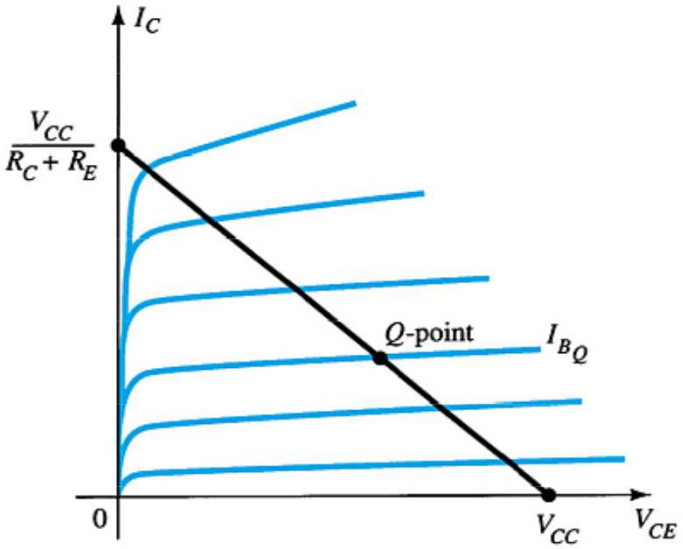
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$I_C = \beta I_B$$

I_B in fixed-bias circuit cannot change, so change in β results in large change in output current and voltage.

Saturation Level





The endpoints can be determined from the load line.

$\mathbf{V_{CEcutoff}}$:

$$\mathbf{V_{CE} = V_{CC}}$$
$$\mathbf{I_C = 0\ mA}$$

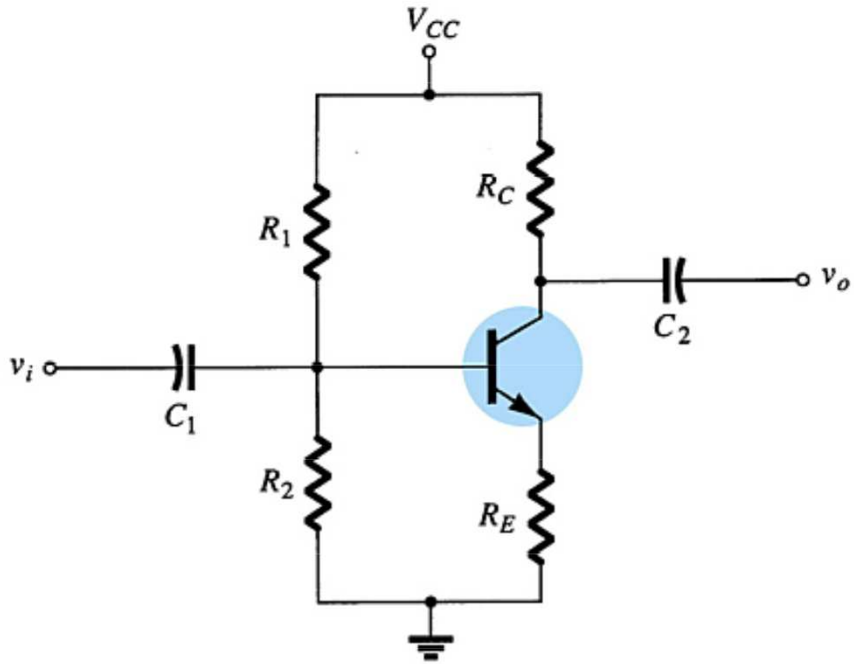
$\mathbf{I_{Csat}}$:

$$\mathbf{V_{CE} = 0\ V}$$
$$\mathbf{I_C = \frac{V_{CC}}{R_C + R_E}}$$

Voltage Divider Bias

This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in β.



Approximate Analysis

Where $I_B << I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E}$$

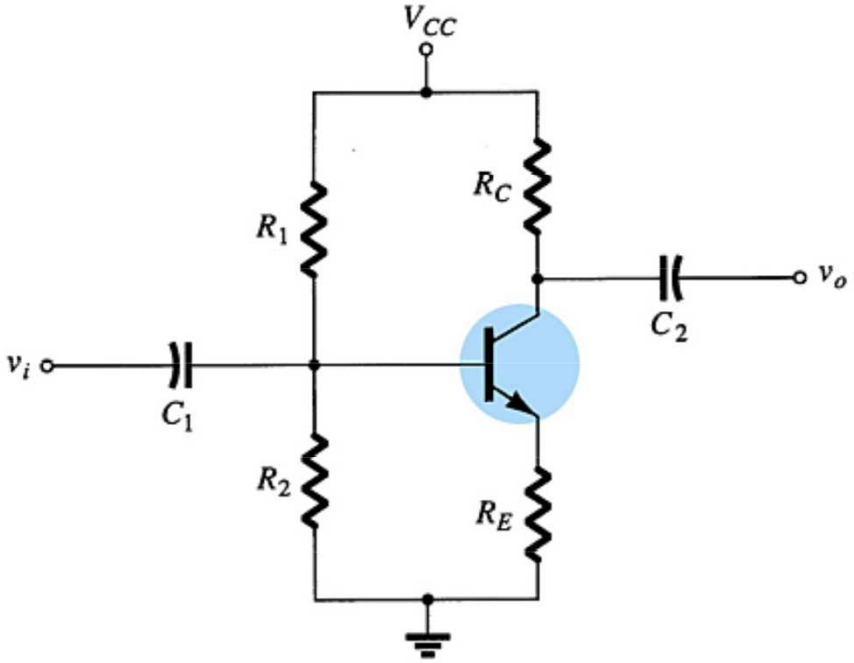
$$V_E = V_B - V_{BE}$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \cong I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Voltage Divider Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$
$$I_C = 0mA$$

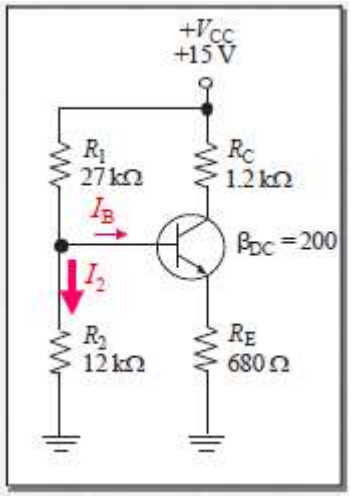
Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$
$$V_{CE} = 0V$$

Voltage Divider Bias

$$V_B = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

$$= \left(\frac{12\ \text{k}\Omega}{27\ \text{k}\Omega + 12\ \text{k}\Omega}\right)(+15\ \text{V}) = 4.62\ \text{V}$$

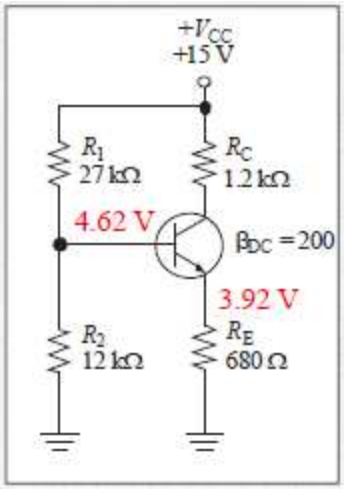


V_E is one diode drop less than V_B:

$$V_E = 4.62\ \text{V} - 0.7\ \text{V} = 3.92\ \text{V}$$

Applying Ohm's law:

$$I_E = \frac{V_E}{R_E} = \frac{3.92\ \text{V}}{680\ \Omega} = 5.76\ \text{mA}$$



Voltage Divider Bias (Exact)

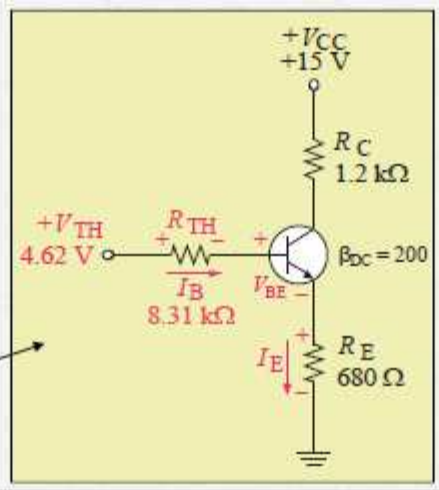
$V_{TH} = V_{B(\text{no load})}$

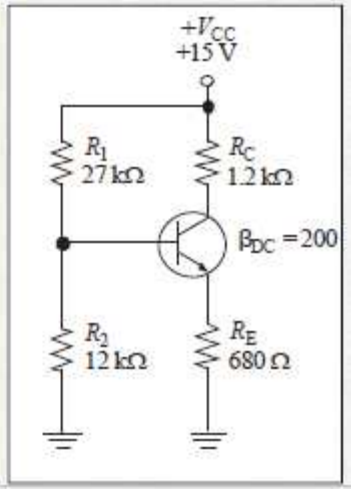
$= 4.62\ \text{V}$

$R_{TH} = R_1 \| R_2 =$

$= 8.31\ \text{k}\Omega$

The Thevenin input circuit can be drawn





$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

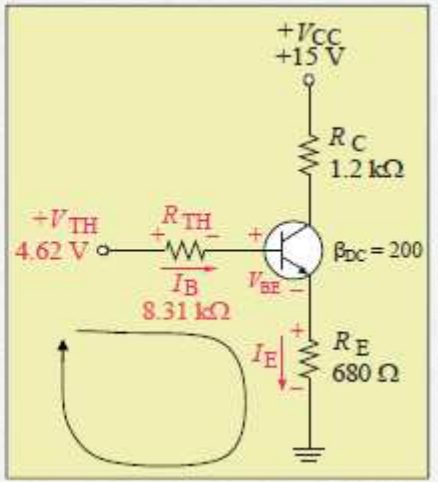
$$I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$$

Substituting and solving,

$$I_E = \frac{4.62\ \text{V} - 0.7\ \text{V}}{680\ \Omega + 8.31\ \text{k}\Omega/200} = 5.43\ \text{mA}$$

and $V_E = I_E R_E = (5.43\ \text{mA})(0.68\ \text{k}\Omega)$

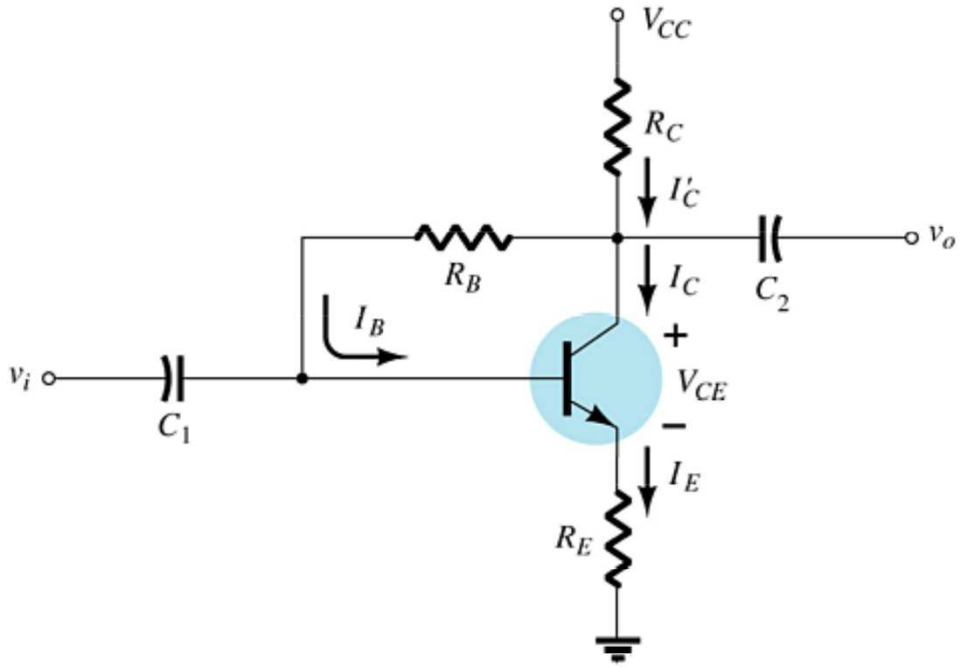
$= 3.69\ \text{V}$



DC Bias with Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



Base-Emitter Loop

From Kirchhoff's voltage law:

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Where $I_B << I_C$:

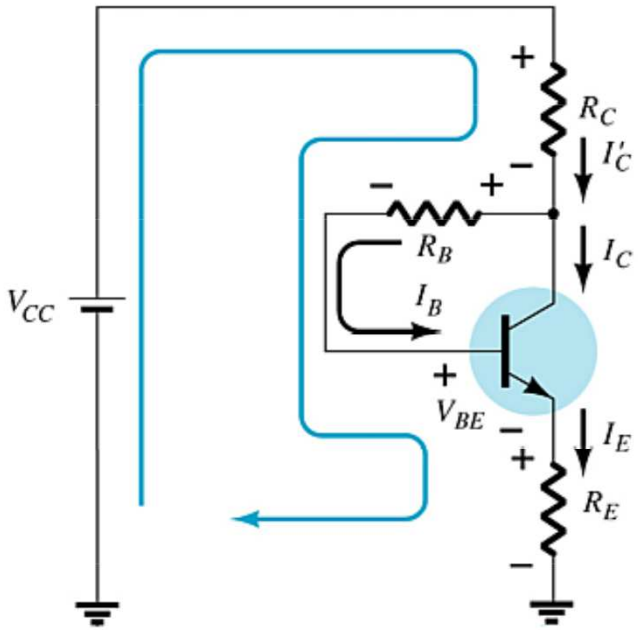
$$I'_C = I_C + I_B \cong I_C$$

Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$



Collector-Emitter Loop

Applying Kirchoff's voltage law:

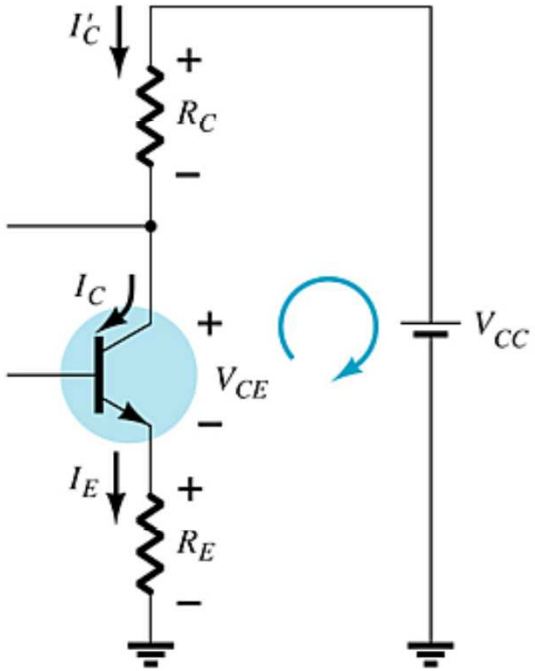
$$I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

Solving for V_{CE}:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Base-Emitter Bias Analysis

Transistor Saturation Level

$$I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$$

Load Line Analysis

Cutoff:

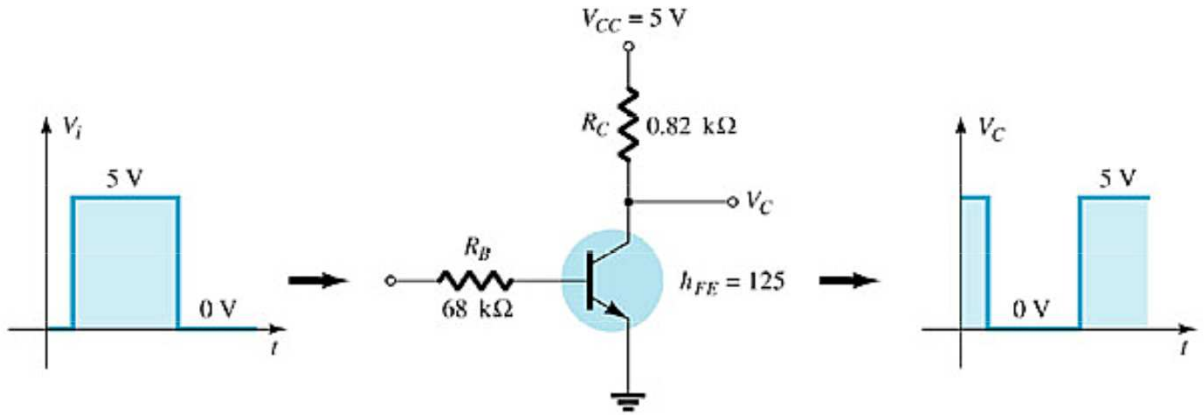
$$V_{CE} = V_{CC}$$
$$I_C = 0\,mA$$

Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$
$$V_{CE} = 0\,V$$

Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.



Switching Circuit Calculations

Saturation current:

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

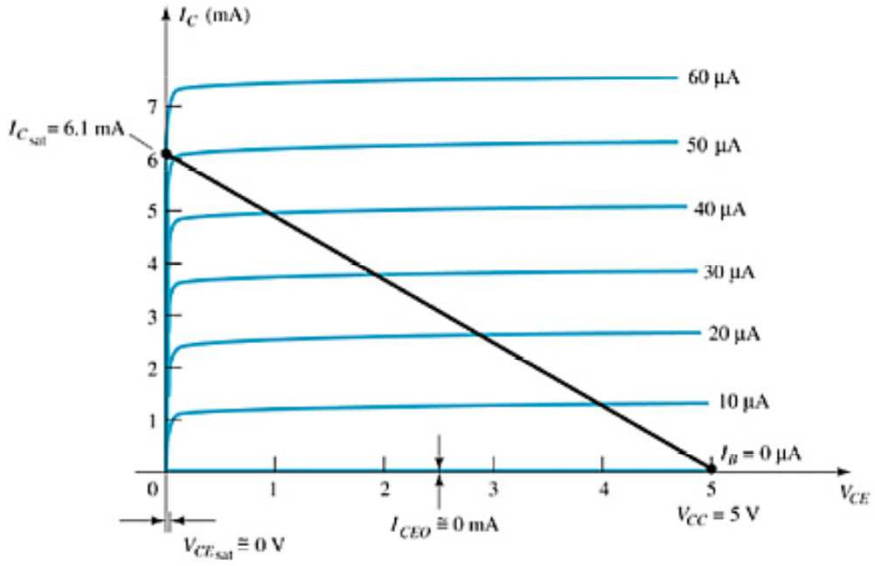
To ensure saturation:

$$I_B > \frac{I_{Csat}}{\beta_{dc}}$$

Emitter-collector resistance at saturation and cutoff:

$$R_{sat} = \frac{V_{CEsat}}{I_{Csat}}$$

$$R_{cutoff} = \frac{V_{CC}}{I_{CEO}}$$

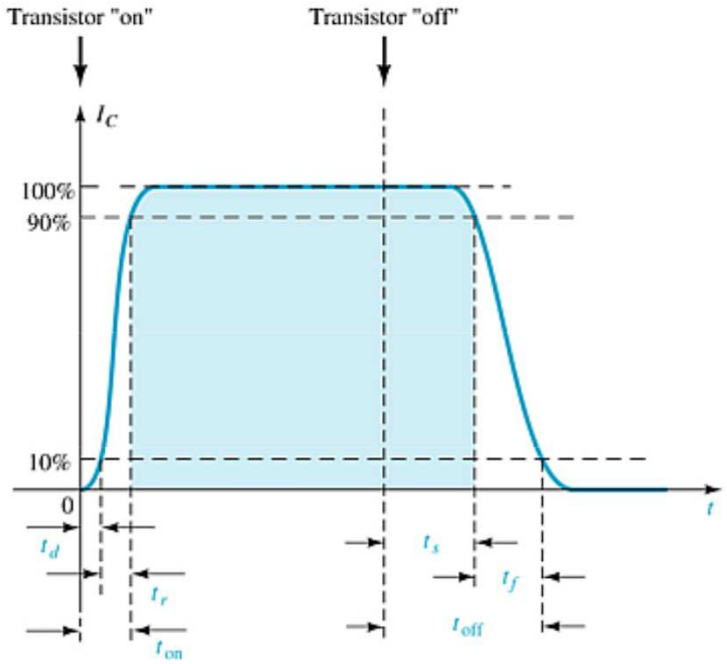


Switching Time

Transistor switching times:

$$t_{on} = t_r + t_d$$

$$t_{off} = t_s + t_f$$



Troubleshooting Hints

- Approximate voltages
  - $V_{BE} \cong .7$ V for silicon transistors
  - $V_{CE} \cong 25\%$ to 75% of V_{CC}
- Test for opens and shorts with an ohmmeter.
- Test the solder joints.
- Test the transistor with a transistor tester or a curve tracer.
- Note that the load or the next stage affects the transistor operation.

PNP Transistors

The analysis for *pnp* transistor biasing circuits is the same as that for *npn* transistor circuits. The only difference is that the currents are flowing in the opposite direction.

Homework 3 (Chapter 3)

- **Common-Base Configuration**
  - **3.4 (13)**
- **Transistor Amplifying Action**
  - **3.5 (18)**
- **Common-Emitter Configuration**
  - **3.6 (23)**

Homework 3 (Chapter 4)

- **Fixed-Bias Configuration**
  - **4.3 (1)**
- **Emitter-Bias Configuration**
  - **4.4 (8)**
- **Voltage Divider Configuration**
  - **4.5 (13)**
- **Collector-Feedback Configuration**
  - **4.6 (23)**
- **Miscellaneous Bias Configuration**
  - **4.59 (30)**