EE457-U: Digital IC Design
Fall Semester 2020
Final Report Cover Sheet

Submit on Blackboard by Friday 11:50PM, 12/18/2020

Final Presentation on Thursday 12/17/2020 from 7:00PM to 10:30PM.

PROJECT TITLE: <u>16-to-1 Multiplexer using Transmission Gates, Static CMOS, and Dynamic CMOS</u>

Group Name:_____Team MUX_____

Student Names:_____Gregory Delpé_&_Handell Vigniero_____

Put Check marks for completion in this column	Topics ***DO NOT alter the order and shape of this table***	GRADES
Required	✔Section1: Executive Summary (1/2 page to 1 page)	
	✔Section 2: Introduction and Background	/5
	✔Section 3: Electric Circuit Schematics (only transistors)	/10
	✔Section 4: Detailed Electric Layouts (*<u>The entire layout should be on single page landscape form.</u>*) Provide detailed layouts of subcircuits with simulations.	/30
	✔Section 5: LTSPICE code and parasitic extractions with calculation analysis. Put only samples of code. Do Not provide multiple pages of LTSPICE code. (-2 points for more than 2 pages of code)	/15
	✔Section 6: IRSIM Logic Simulations and Measurements for Layout and Schematic <u>(must provide comparisons between the two using tables)</u>	/10
	✔Section 7: Measurements in LTSPICE for delays for Layout and Schematic <u>(must provide comparisons between the two using tables)</u>	/15
	✔Section 8: Measurements of <u>power, delay, chip area, timing, number of transistors</u> for the layout. (If you are using TG, static or dynamic CMOS, compare here using tables.)	/10
Required	✔Section 9: Conclusions and References	
Required	✔Presentation (Thursday 7:00PM – 10:30PM, 12/17/2020)	/5
	Late Report (-5pts per day until day 12/21/2020)	
Answer	✔Does the project work? (-20pts for not functioning design)	Yes
	TOTAL	**/100**

2) *Design of 16-to-1 Multiplexer using both of (1) transmission gates (TG), (2) Static CMOS, and (3) dynamic CMOS circuit. Compare the TG design with conventional CMOS gate designs (dynamic and static) by performance, power, chip size, number of transistors, etc.*

1. Executive Summary

Hereafter, I will detail the steps and procedures that were employed in the design and simulation of a 16:1 multiplexer. The 16:1 multiplexers that will be evaluated in this exercise have been implemented using transmission gate, static CMOS, and dynamic CMOS logic. Subsequent to the construction of the three 16:1 multiplexer designs presently alluded to herein, further observations are presented with reference to the relative performance of each design.

In general, complementary static CMOS network designs consisting of PMOS and NMOS transistor configurations that form pull-up and pull-down networks are inherently more complex than dynamic and transmission gate network designs. The parallel nature of transmission gate logic yields a more performant network implementation with a reduced transistor count. Similarly, dynamic CMOS designs offer performance enhancements with comparison to networks implemented using static CMOS logic patterns.

Using the Electric VLSI Design System EDA we have constructed tree 16:1 multiplexers. Schematic and layout designs have been implemented for the 16:1 multiplexer static CMOS, dynamic CMOS, and transmission gate logic design. Each design implementation has been tested for common errors and simulated using LTSpice and IRSIM simulation tools made available in Electric VLSI. We have drafted SPICE decks to simulate and measure the performance of each layout and schematic design. Additional steps have been taken to configure Electric for parasitic extraction.

2. Introduction and Background

The multiplexer is a fundamental component of modern computer architecture. In essence, a multiplexer operates as a binary selector. Given an input representing a binary number, a multiplexer will return the data associated with the selected binary input supplied to the component. A multiplexer with 2^n inputs has n ($\log_2(n)$) *select* lines that control which input lines will be returned as the output of the multiplexer circuit.

To demonstrate the utility of the multiplexer circuit, we will implement a 16:1 multiplexer in three formats and compare the performance and implementation characteristics of each design to better understand the implication of each implementation in the context of discrete design patterns.

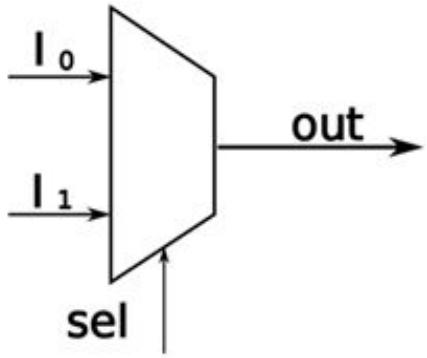

Figure 1: *2:1 Multiplexer*

The 16:1 multiplexer is a digital selector circuit comprising sixteen inputs and four selectors; it returns a single output that is determined by the combination of the data supplied as inputs to the 16:1 multiplexer and the selector designation. The output of the 16:1 multiplexer will be one of the sixteen inputs supplied to the 16:1 multiplexer as depicted in *Figure 2*.

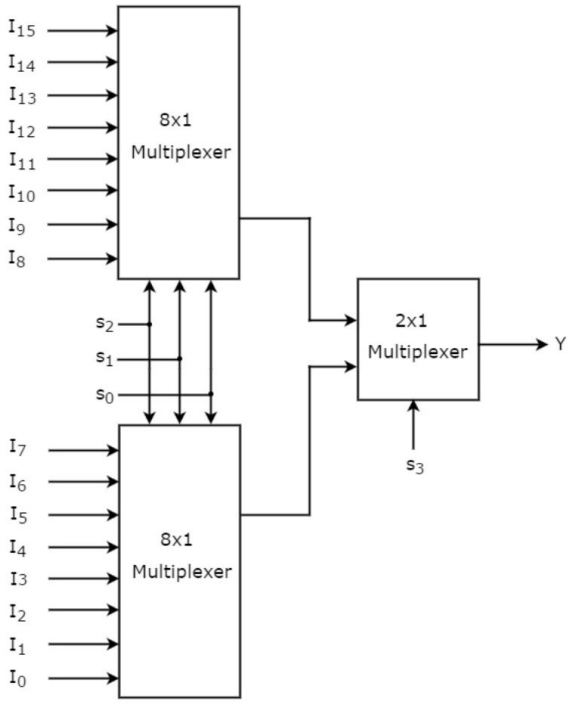

Figure 2: *16:1 Multiplexer*

Multiplexers have many practical applications in the implementation of modern integrated circuits used in computers and digital hardware components. Multiplexers allow several electronic signals to share one device or resource. Thus, there is an economically compelling argument for the integration of multiplexer circuits in electronic circuit design.

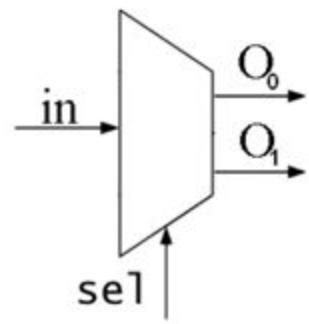

Figure 3: 2:1 Demultiplexer

Data that is transmitted via multiplexed media can be decoded on the receiving end of the transmission line using a demultiplexer. Where a multiplexer can be described as a multiple-input, single-output device, we can characterize demultiplexers as single-input, multiple-output devices. Receiving a single input, a demultiplexer will pipe the signal to the appropriate output line associated with the designated selector.

For the purposes of this exploratory exorcise, we will focus our efforts on the design characteristics of the 16:1 multiplexer. The 16:1 digital multiplexer responds to electronic signals with a binary representation of the value 0 and 1. In the case of a 16:1 multiplexer, if the signals supplied to the selector lines of the multiplexer circuit have a binary representation of the value 0 [0000], the 16:1 multiplexer would return the data associated with I_0 (input 0) as detailed in the 16:1 Multiplexer Truth Table below. A selector designation with a binary representation of the value 1 [0001] would result in an output of the data associated with I_1 (input 1).

A 16:1 multiplexer where I_0, I_1, I_2, …, I_{15} are the given inputs, S_0, S_1, S_2, and S_3 are the selector inputs, and Y is the output; can be express as the Boolean function detailed in *Figure 4* hereafter.

$$
\begin{aligned}
Y = {} & (S_0'S_1'S_2'S_3'I_0) + (S_0'S_1'S_2'S_3I_1) + (S_0'S_1'S_2S_3'I_2) \\
& + (S_0'S_1'S_2S_3I_3) + (S_0'S_1S_2'S_3'I_4) + (S_0'S_1S_2'S_3I_5) \\
& + (S_0'S_1S_2S_3'I_6) + (S_0'S_1S_2S_3I_7) + (S_0S_1'S_2'S_3'I_8) \\
& + (S_0S_1'S_2'S_3I_9) + (S_0S_1'S_2S_3'I_{10}) + (S_0S_1'S_2S_3I_{11}) \\
& + (S_0S_1S_2'S_3'I_{12}) + (S_0S_1S_2'S_3I_{13}) + (S_0S_1S_2S_3'I_{14}) \\
& + (S_0S_1S_2S_3I_{15})
\end{aligned}
$$

Figure 4: *Boolean Function for 16:1 Multiplexer Output "Y"*

We can expand this expression into a truth table detailing all the potential permutation of the multiplexer inputs and the associated output we expect to be returned:

16:1 Multiplexer Truth Table

Selection Inputs				*Output*
S3	***S2***	***S1***	***S0***	***Y***
0	0	0	0	I0
0	0	0	1	I1
0	0	1	0	I2
0	0	1	1	I3
0	1	0	0	I4
0	1	0	1	I5
0	1	1	0	I6
0	1	1	1	I7
1	0	0	0	I8
1	0	0	1	I9
1	0	1	0	I10
1	0	1	1	I11
1	1	0	0	I12
1	1	0	1	I13
1	1	1	0	I14
1	1	1	1	I15

The traditional implementation of a 4:1 multiplexer is comprised of a combination of subcomponents. *Figure 6* depicts a traditional model for the implementation of a 4:1 multiplexer consisting of two inverters, four 3-input AND gates, and a 4-input OR gate.

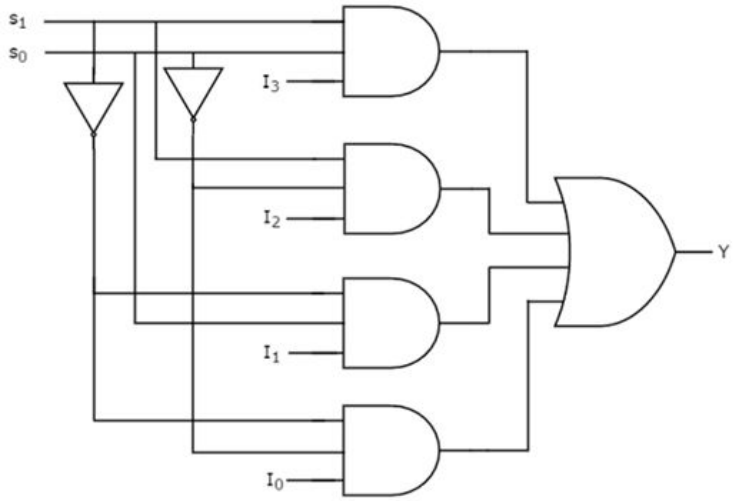

Figure 5: *Circuit Diagram for Digital 16:1 Multiplexer*

A 4:1 multiplexer where I0, I1, I2, and I3 are the given inputs, S0 and S1 are the selector inputs, and Y is the output; can be expressed as the Boolean function detailed in *Figure 6*.

$$Y = S_1{}'S_0{}'I_0 + S_1{}'S_0I_1 + S_1S_0{}'I_2 + S_1S_0I_3$$

Figure 6: *Boolean Function for 4:1 Multiplexer Output "Y"*

We can expand this expression into a truth table detailing all the potential permutation of the multiplexer inputs and the associated output we expect to be returned:

4:1 Multiplexer Truth Table

Selection Inputs		*Output*
S1	***S0***	***Y***
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Using two 4:1 multiplexers in concert with a 2:1 multiplexer similar to the model depicted in *Figure 1,* we can construct an 8:1 multiplexer capable of selecting 8 distinct signal values.

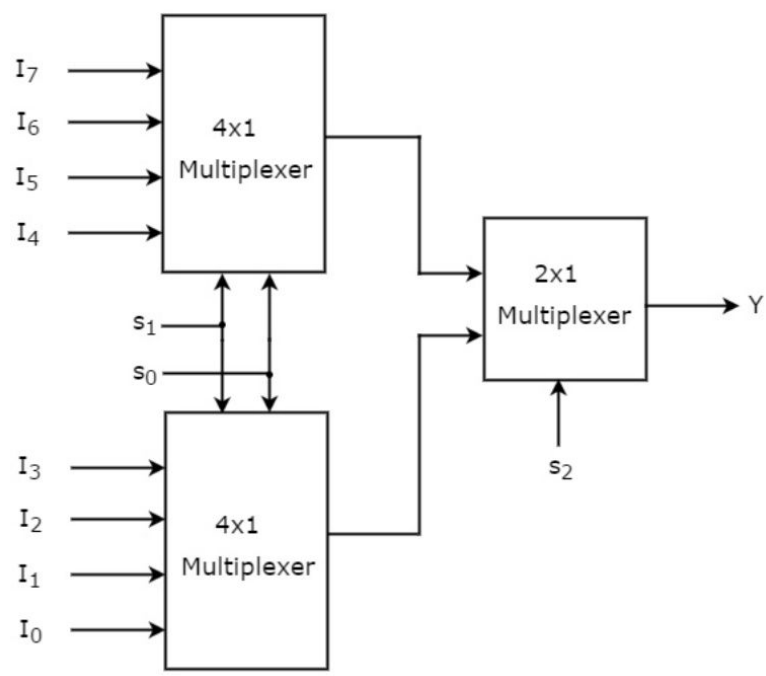

Figure 7: *8:1 Multiplexer*

8:1 Multiplexer Truth Table

Selection Inputs			*Output*
S2	***S1***	***S0***	***Y***
0	0	0	I0
0	0	1	I1
0	1	0	I2
0	1	1	I3
1	0	0	I4
1	0	1	I5
1	1	0	I6
1	1	1	I7

Furthermore, we can compose 8:1 multiplexers in conjunction with a 2:1 multiplexer to construct the 16:1 multiplexer (*Figure 2*) that we will implement in the interest of evaluating the performance characteristic of discrete CMOS design patterns.

This report details the implementation of a traditional 16:1 multiplexer design using static CMOS logic that is akin to the conventional digital circuit illustrated in *Figure 5*, but digital logic design is not absolute; there are many cleaver implementation patterns and practices that we can leverage to optimize the performance of a standard multiplexer. Among these optimization techniques is the integration or use of transmission gates in the implementation of a circuit design.

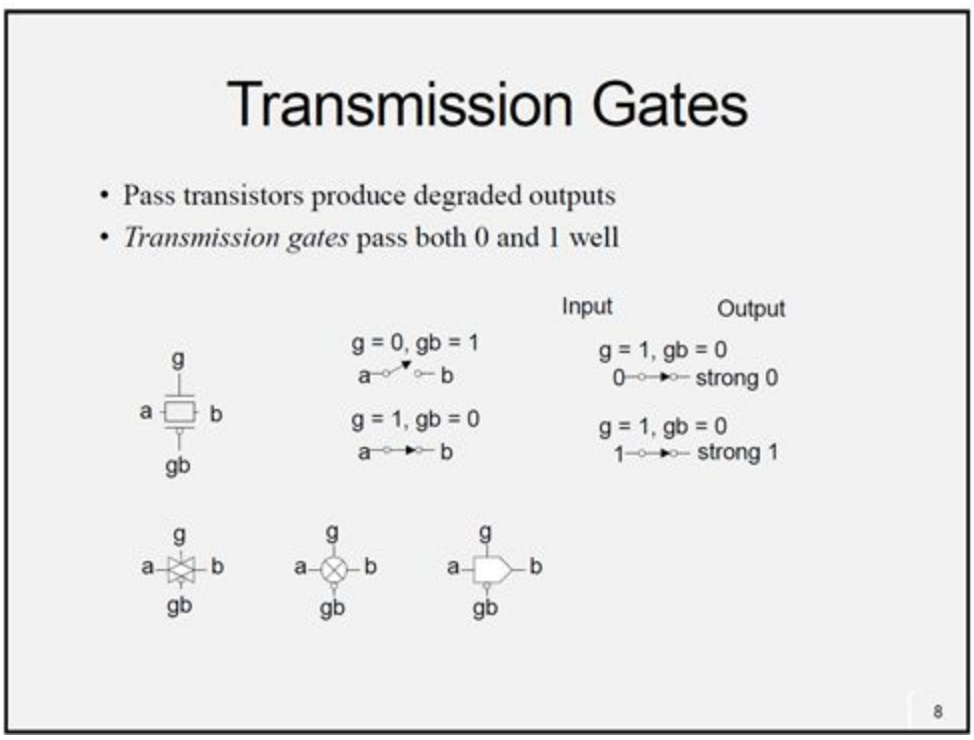

Figure 8: *Lecture_4_Final Slide 8*

Transmission gates can be constructed by pairing a p-type and n-type MOSFET in parallel such that their respective source and drain terminals are shared. CMOS transistors can be abstracted as opened and closed switches that operate as a function of the supplied voltage applied to the gate terminal of the transistor. When the voltage applied to the gate terminal of a PMOS transistor is low it will operate as a closed switch. When the supplied voltage applied to the gate terminal of a PMOS transistor ($V_{GS} > V_{TH}$) is high, the PMOS transistor acts as an open circuit. NMOS transistors have an inverse response with comparison to that of a PMOS transistor. When the supplied voltage applied to the gate terminal of the NMOS transistor is high ($V_{GS} > V_{TH}$) it acts as a closed circuit. When the supply voltage is low, the NMOS transistor behaves as an open switch. Thus, we can leverage the complementary nature of PMOS and NMOS transistors to construct a transmission gate that will return the input as determined by the a control signal as depicted in *Figure 6*; where the input will be returned as output if the control signal A is high and suppressed if the control signal A is low.

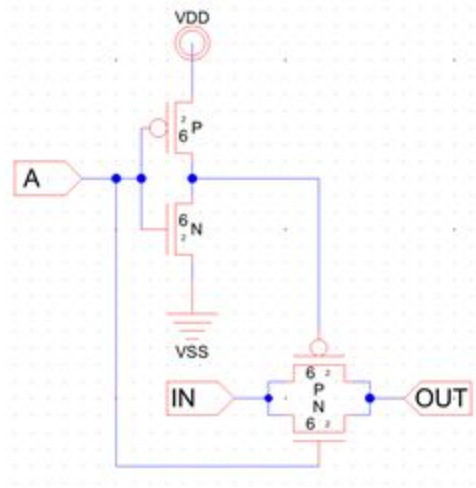

Figure 6: Transmission Gate

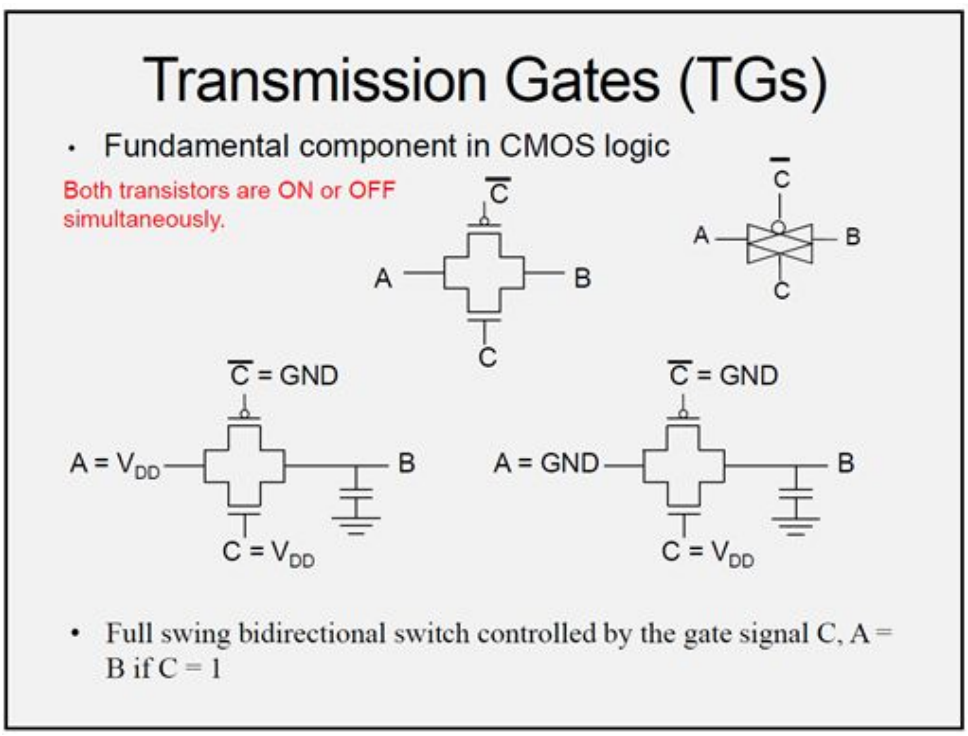

Figure 9: *Lecture_4_Final Slide 9*

In addition to the implementation of the 16:1 multiplexer implemented using static CMOS logic, we have also constructed a 16:1 multiplexer using transmission gates consistent with the model detailed in *Figure 8* above.

Where circuit delay and total silicon chip area are a major concern in the implementation of digital integrated circuits, we can leverage the advantages inherent in dynamic CMOS logic design patterns. Dynamic CMOS logic designs implement clocked pull-up transistors in place of static PMOS transistors that are always on. Here, we will implement a 16:1 multiplexer using dynamic CMOS logic patterns to demonstrate these performance advantages.

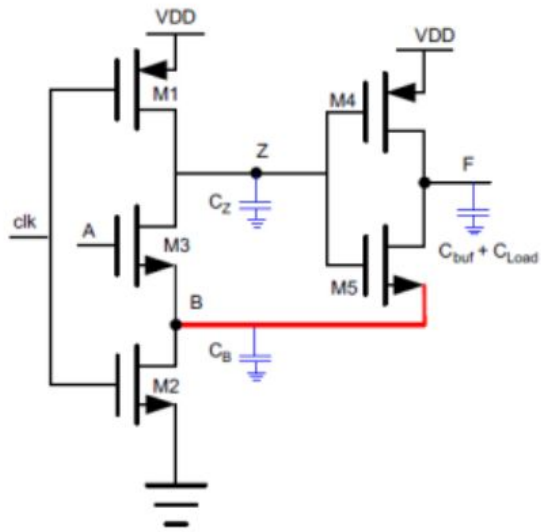

Figure 10: *Generalized Dynamic Circuit*

3. Electric Circuit Schematics

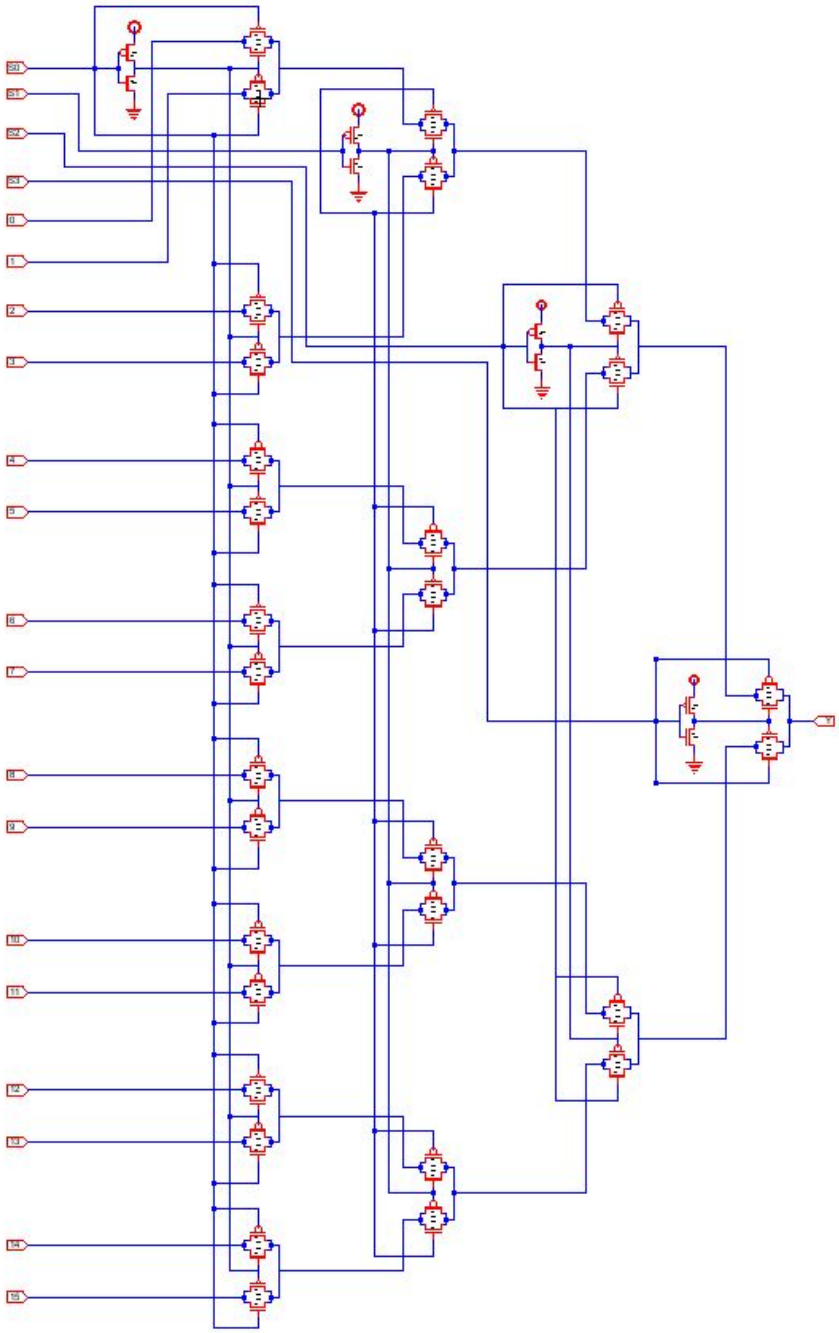

Figure 11: *Electric Schematic for 16:1 Multiplexer ~ Transmission Gates*

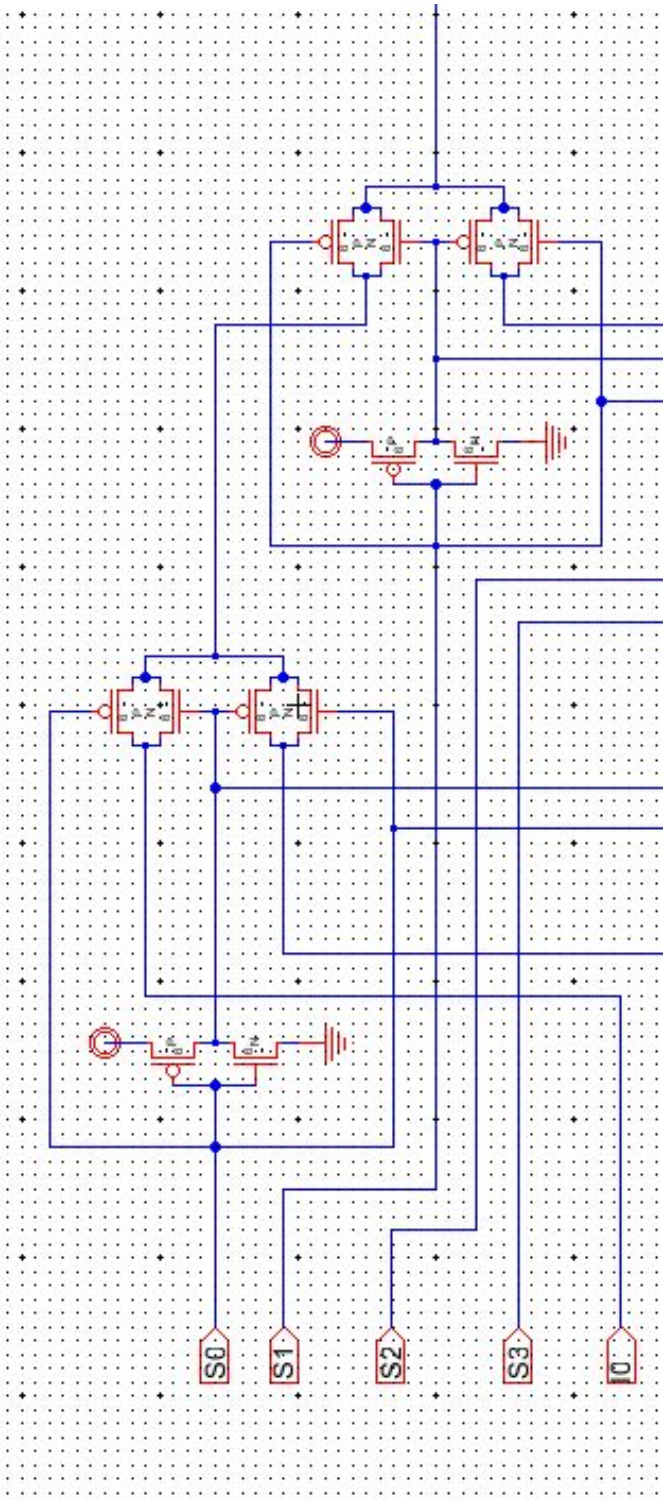

Figure 12: *Electric Layout for 16:1 Multiplexer Input ~ Transmission Gates*

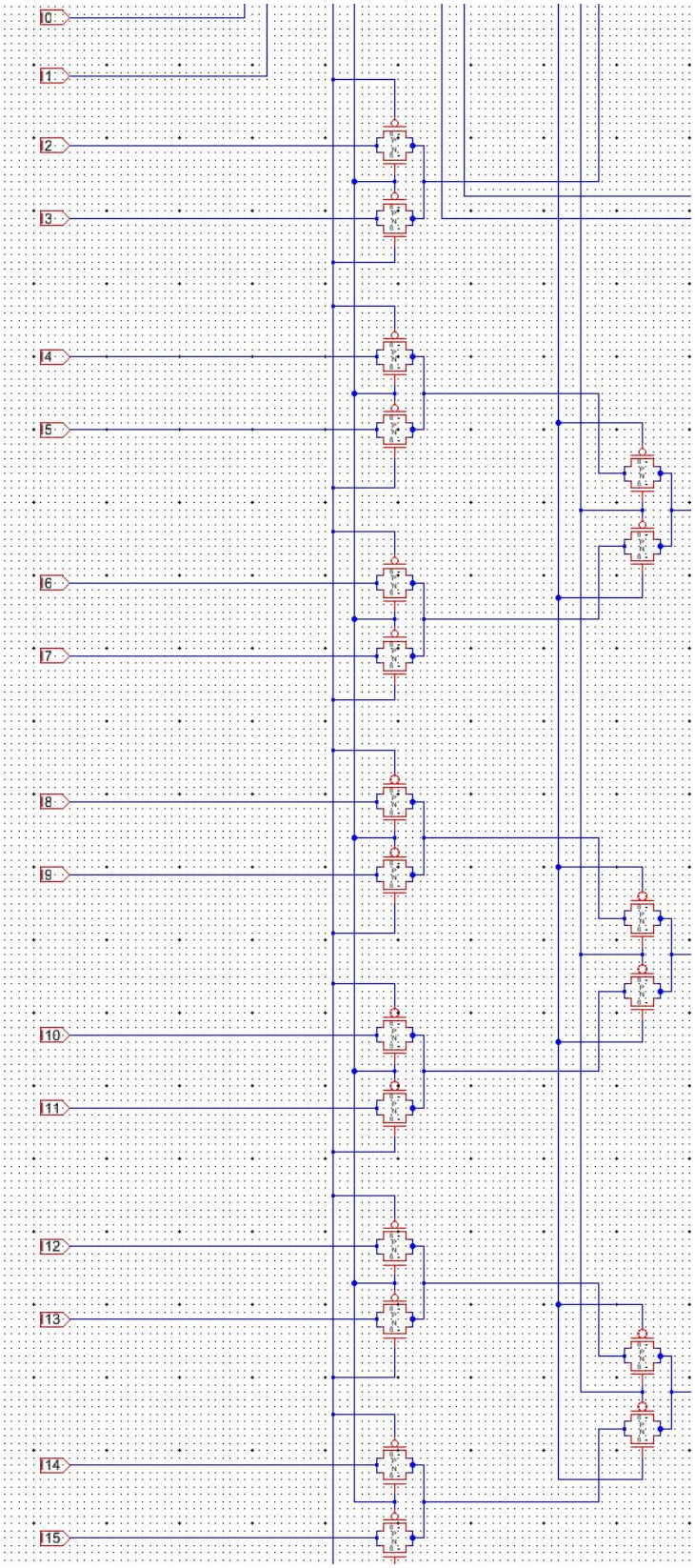

Figure 13: *Electric Layout for 16:1 Multiplexer Input ~ Transmission Gates*

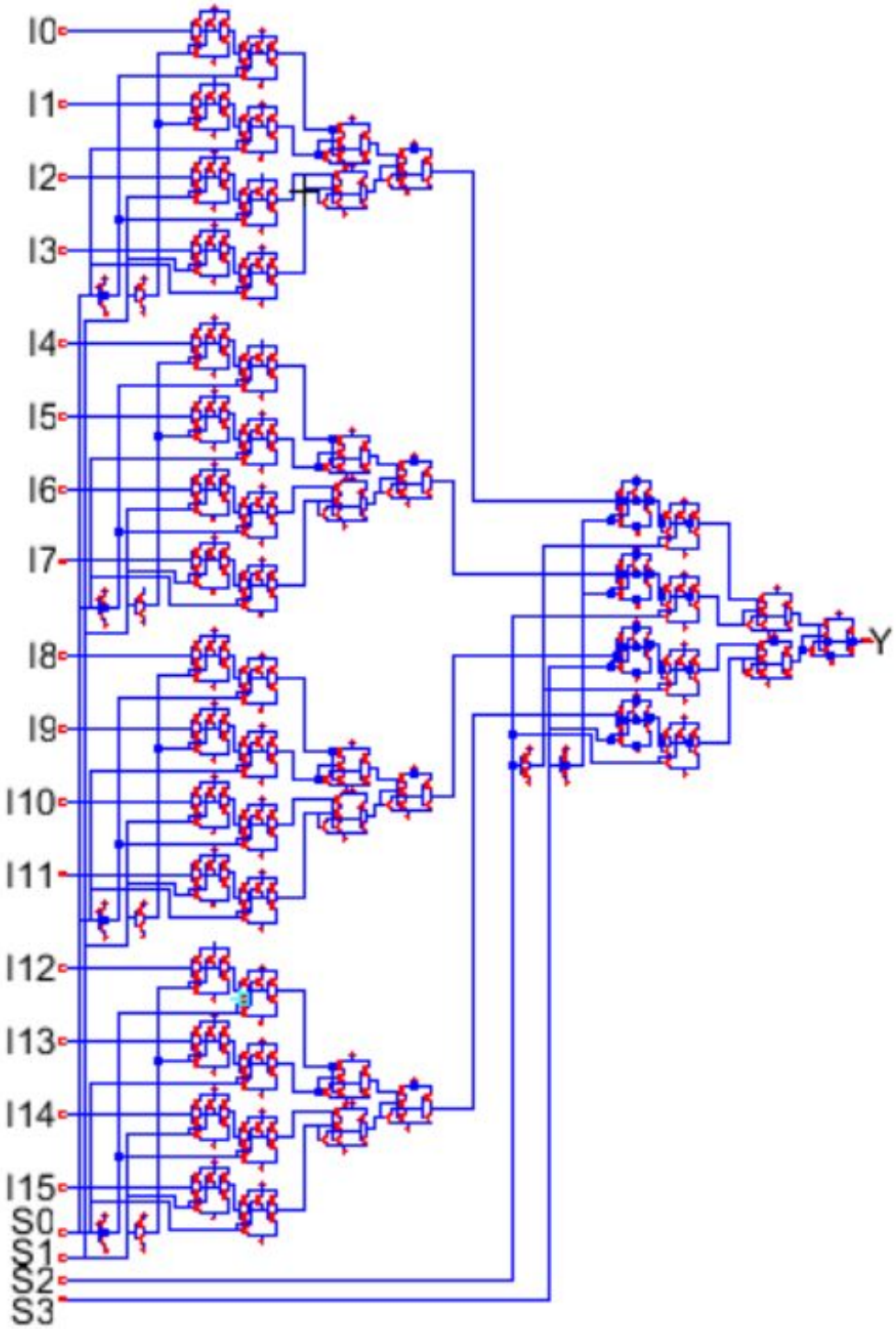

Figure 14: *Electric Schematic for 16:1 Multiplexer ~ Static CMOS Gates*

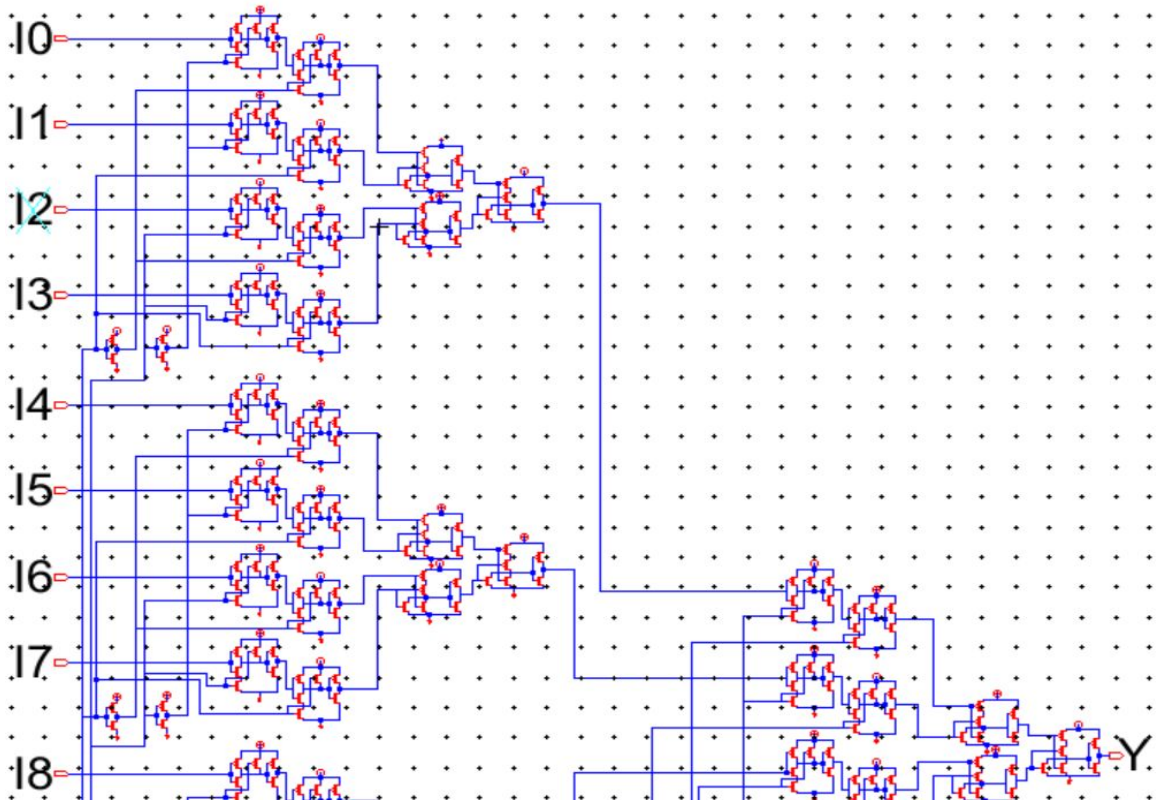

Figure 15: *Electric Schematic for 16:1 Multiplexer ~ Static CMOS Gates*

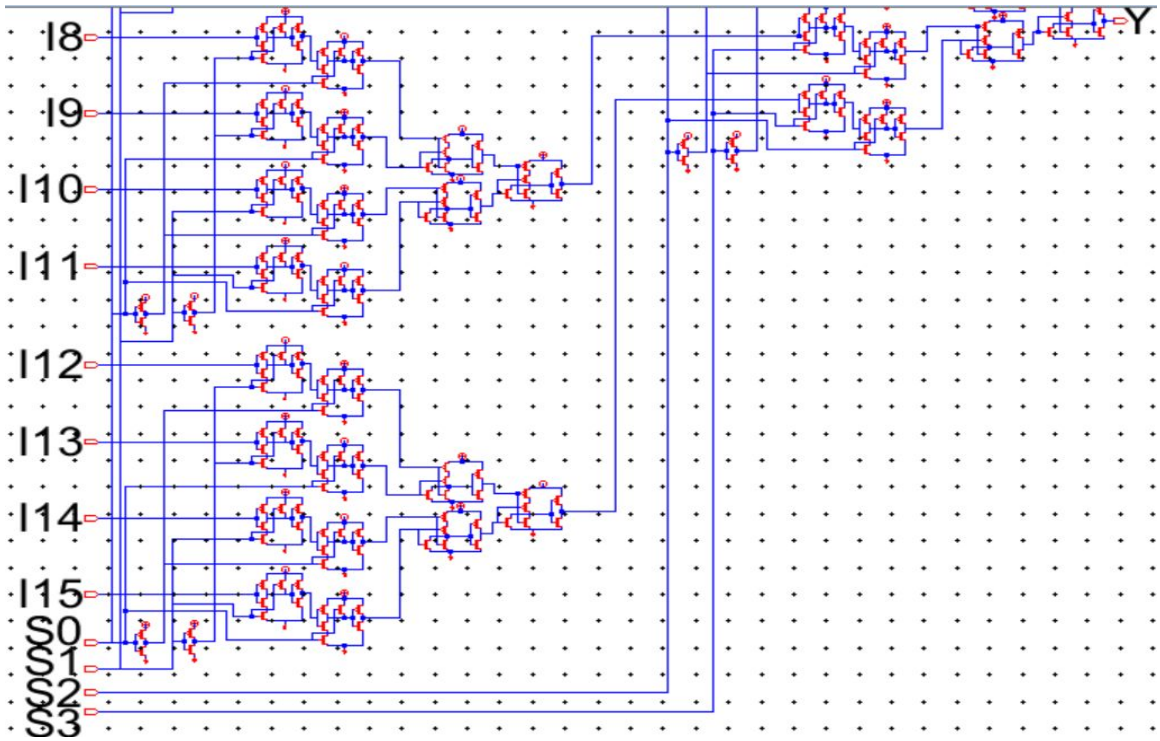

Figure 16: *Electric Schematic for 16:1 Multiplexer ~ Static CMOS Gates*

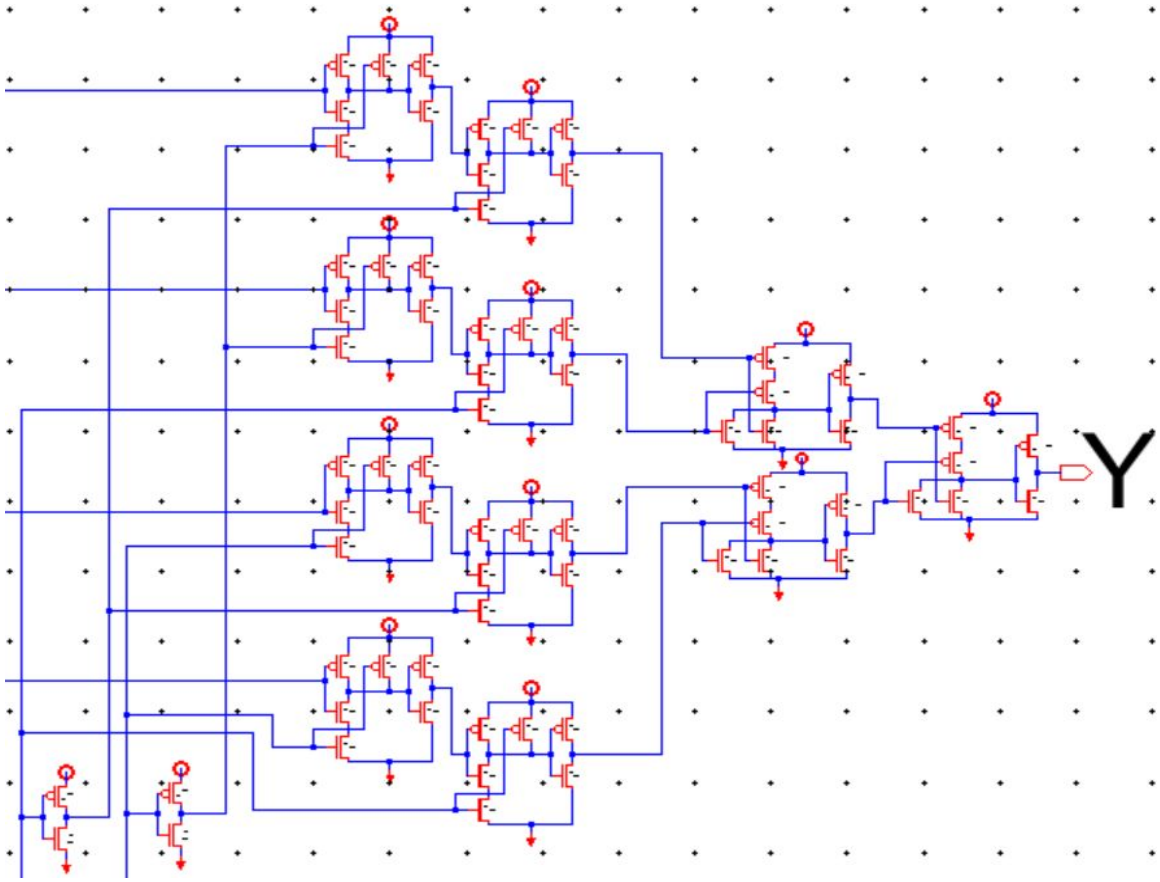

Figure 17: *Electric Schematic for 16:1 Multiplexer ~ Static CMOS Gates*

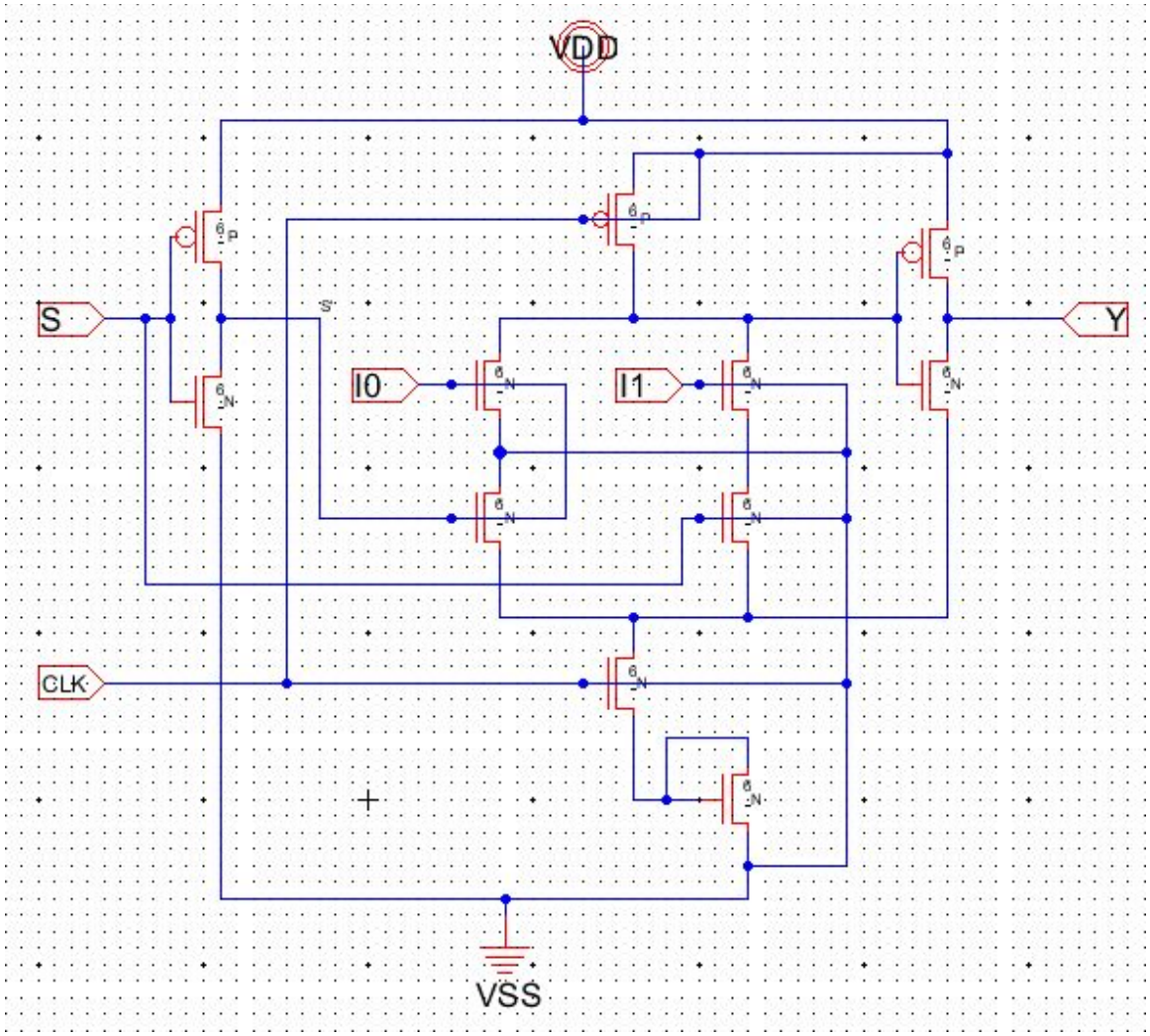

Figure 18: *2:1 Multiplexer ~ Dynamic CMOS*

"Domino circuits are widely used in high-speed applications for the implementation of high fan-in circuits. However, domino circuits are vulnerable to noise. In order to improve performance, the transistor threshold voltage has to be commensurately scaled to maintain a high drive current. However, the threshold voltage scaling results in the substantial increase of the sub-threshold leakage current. The main source of noise in deep-submicron circuits is mainly due to the high leakage current, crosstalk noise, supply noise, and charge-sharing. Performance degraded in a domino circuit is due to propagation of pre-charge pulse from dynamic node to the output node. The Pseudo Domino Buffer based design for domino logic compensates this problem up to some extent. In the Footed Diode Domino logic an NMOS transistor which is working as a diode in between GND and M2 clock transistors. This transistor reduces the discharging time furthermore which in turn reduces the delay. ***Figure 18*** *shows a generalised CMOS* ***footed diode domino*** *logic and multiplexer using the same logic. [http://data.conferenceworld.in/IETEAUGUST2017/55.pdf]"*

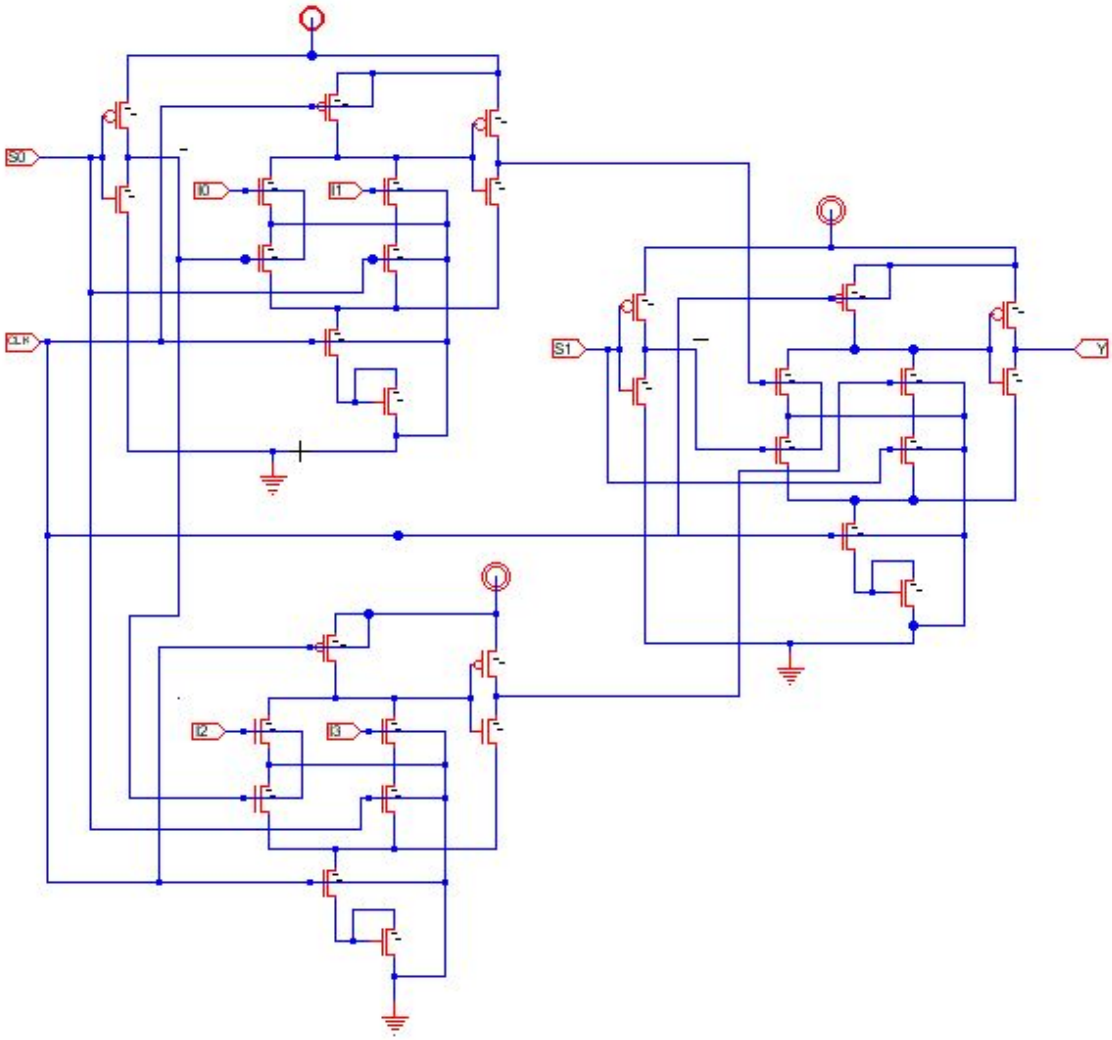

Figure 19: *4:1 Multiplexer ~ Dynamic CMOS*

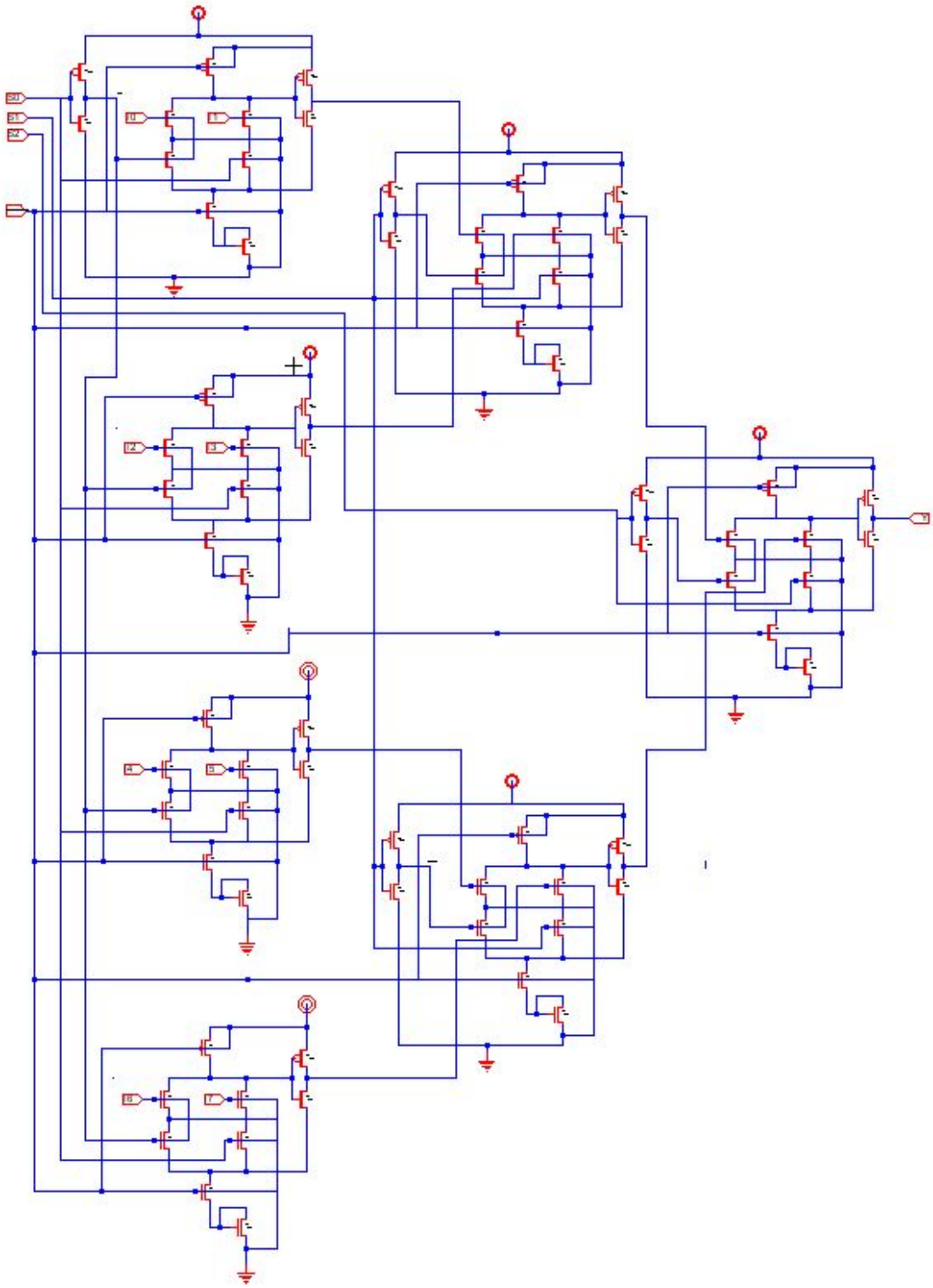

Figure 20: *8:1 Multiplexer (8-Bit) ~ Dynamic CMOS*

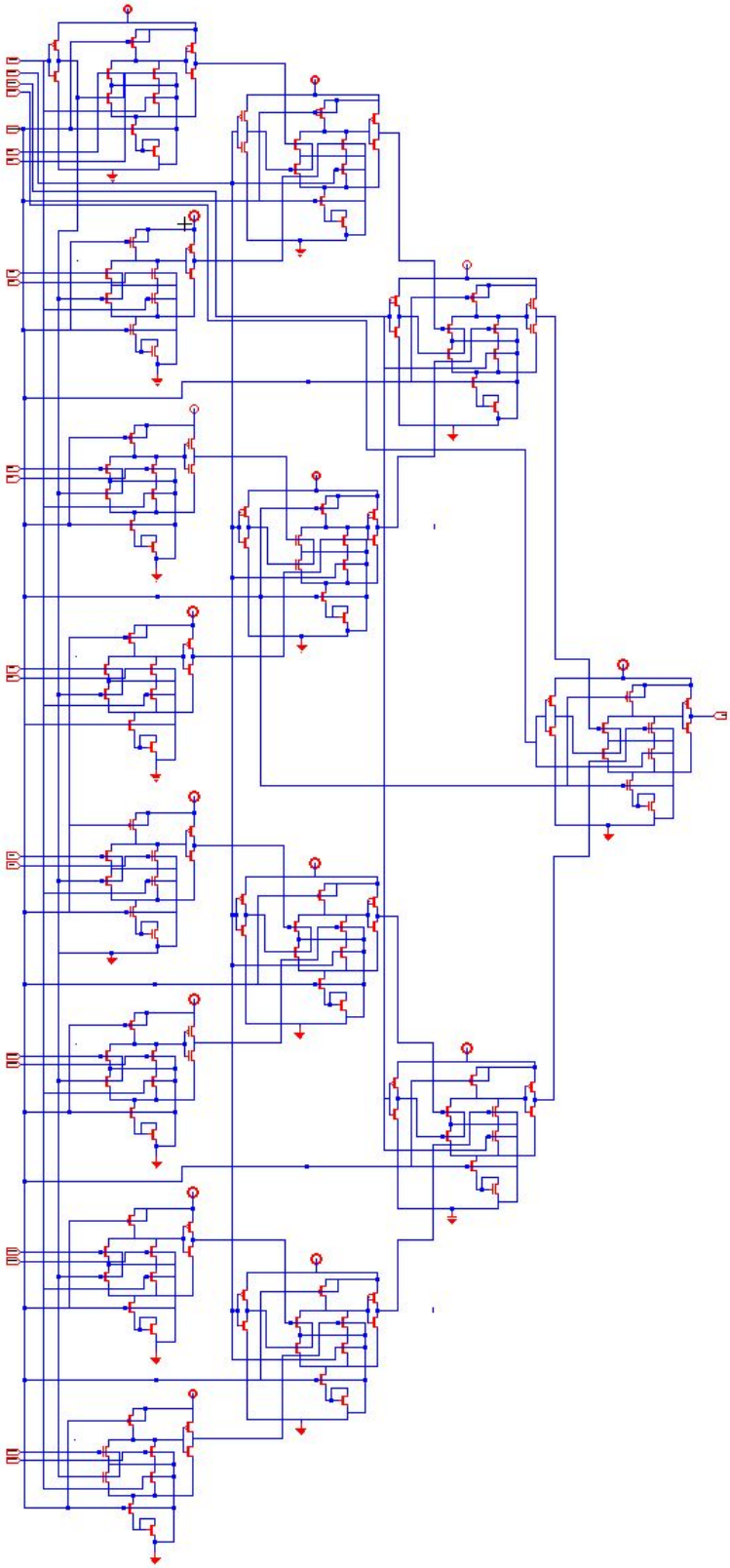

Figure 21: *16:1 Multiplexer ~ Dynamic CMOS*

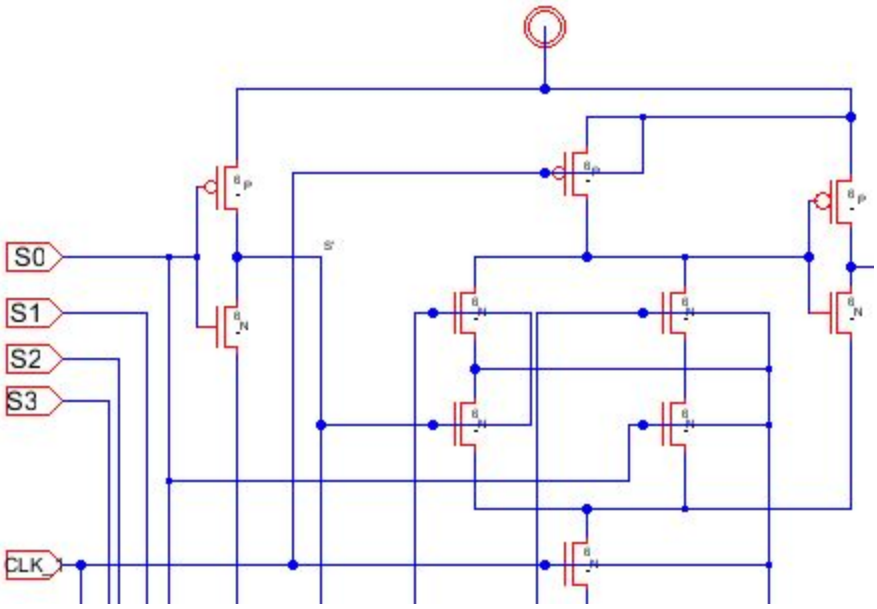

Figure 22: *Electric Layout for 16:1 Multiplexer Input ~ Dynamic CMOS*

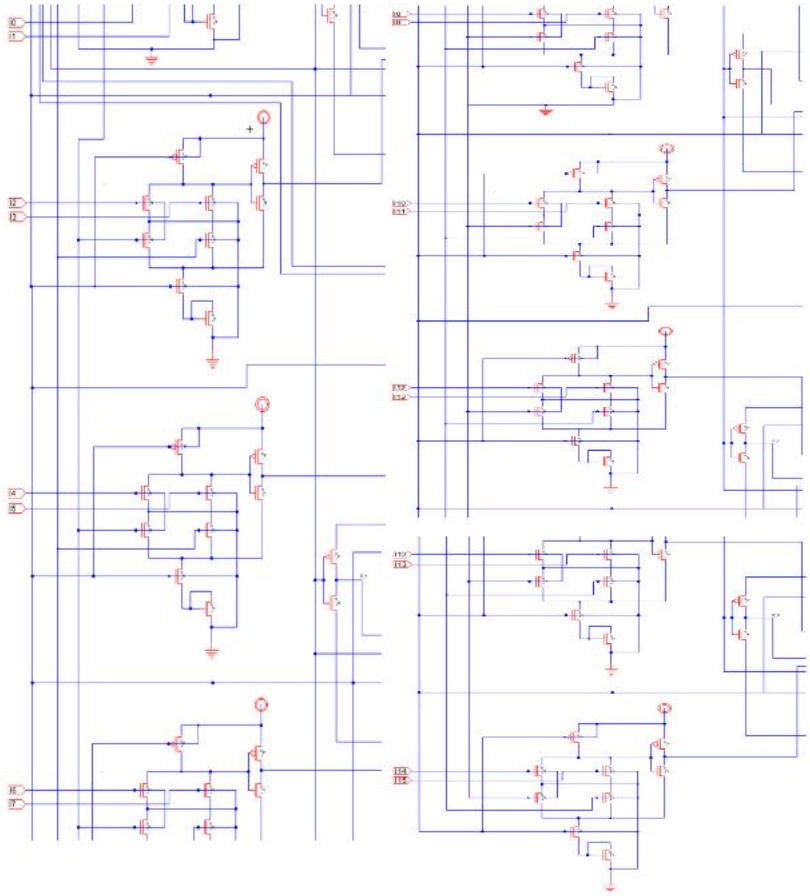

Figure 23: *Electric Layout for 16:1 Multiplexer Input ~ Dynamic CMOS*

4. Detailed Electric Layouts

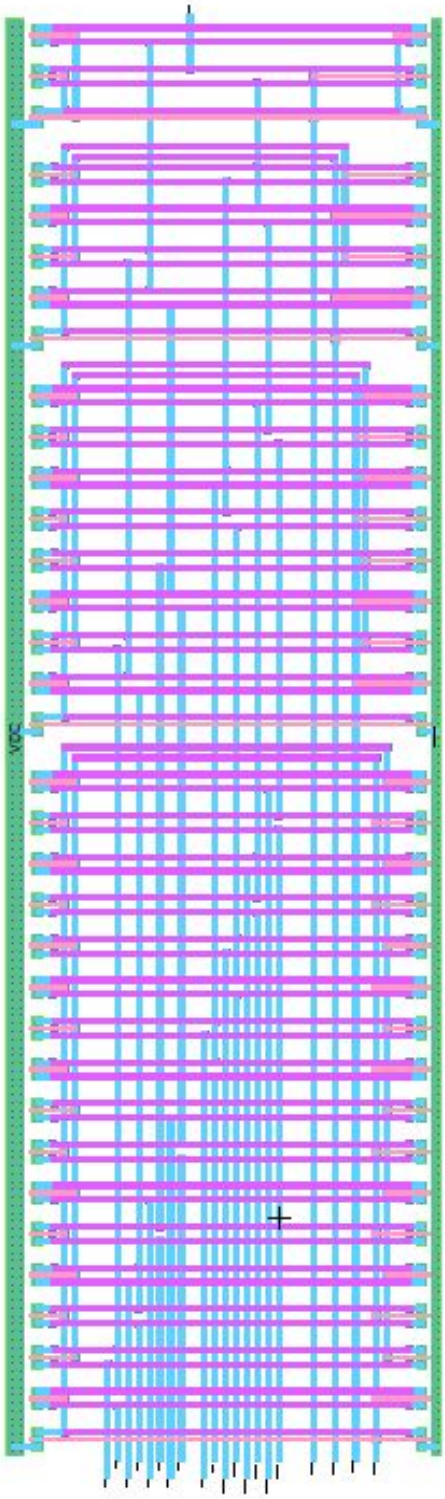

Figure 24: *Electric Layout for 16:1 Multiplexer ~ Transmission Gates*

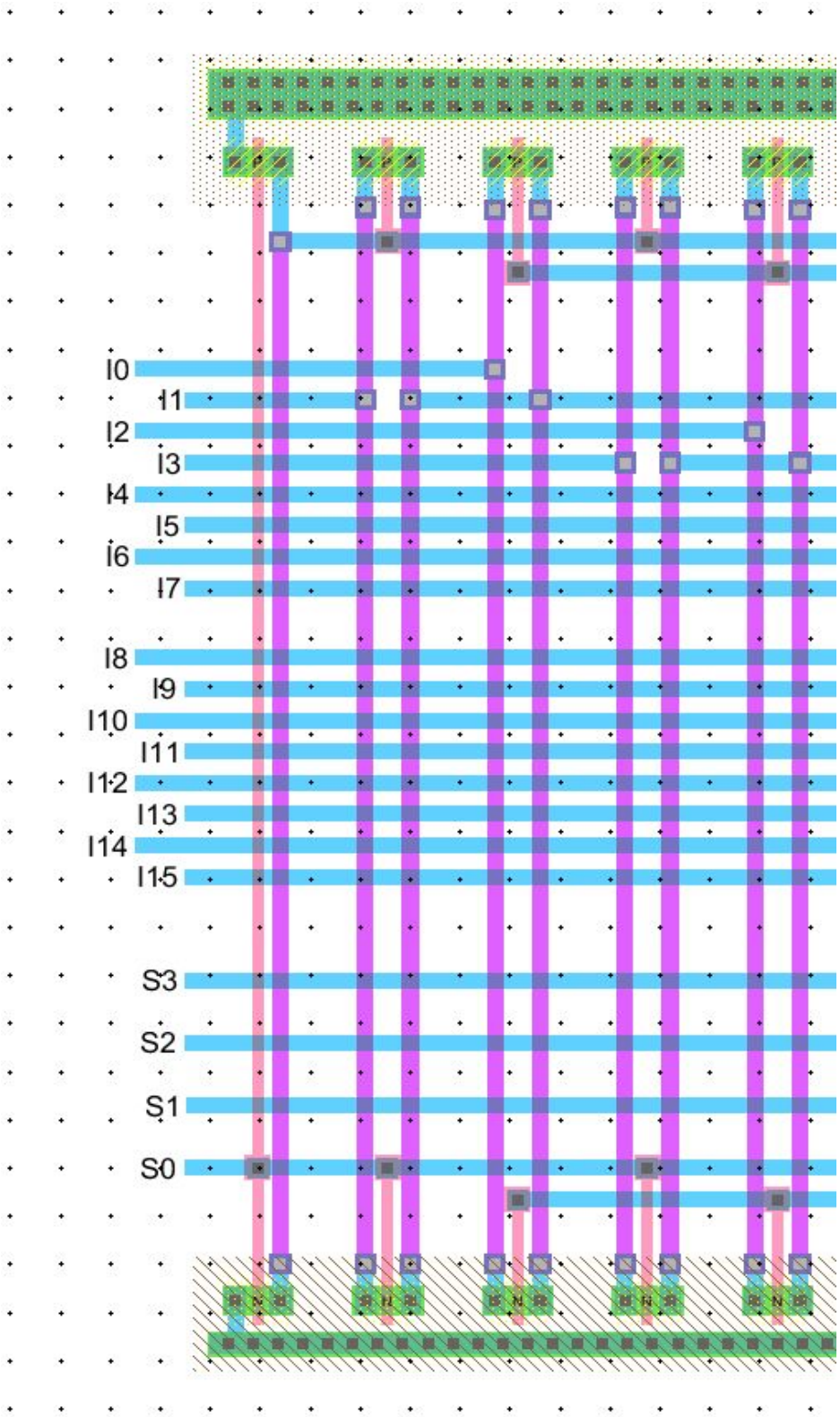

Figure 25: *Electric Layout for 16:1 Multiplexer Input ~ Transmission Gates*

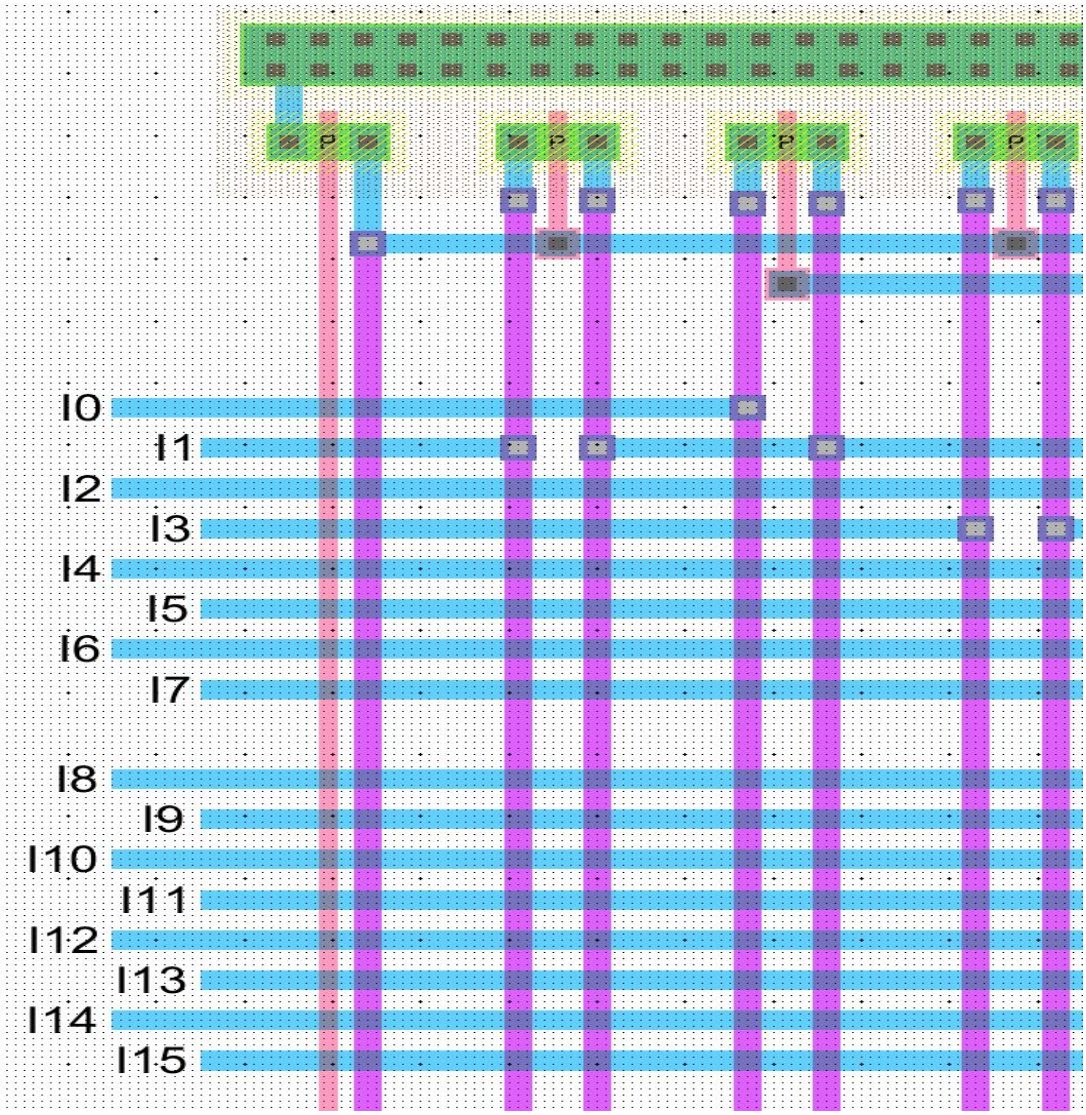

Figure 26: *Electric Layout for 16:1 Multiplexer Input ~ Transmission Gates*

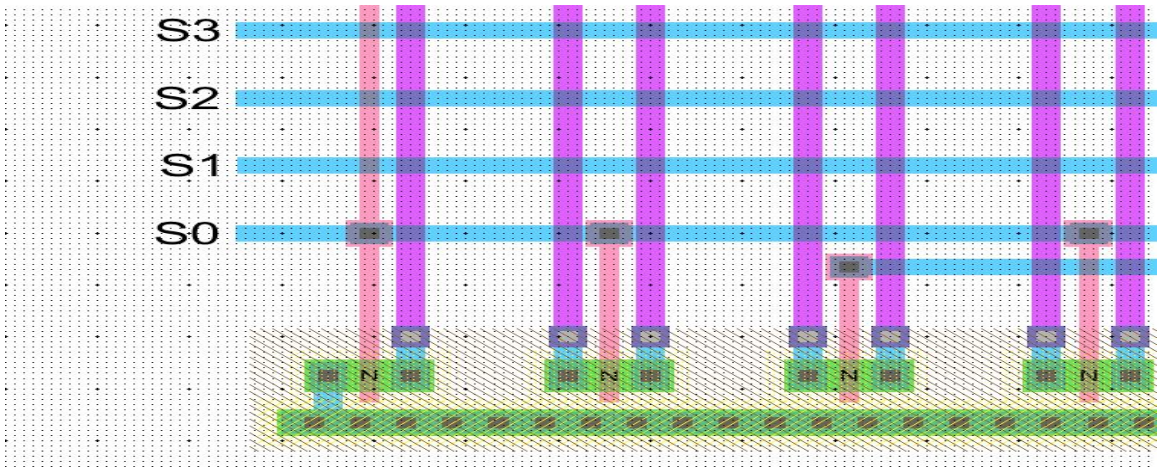

Figure 27: *Electric Layout for 16:1 Multiplexer Input ~ Transmission Gates*

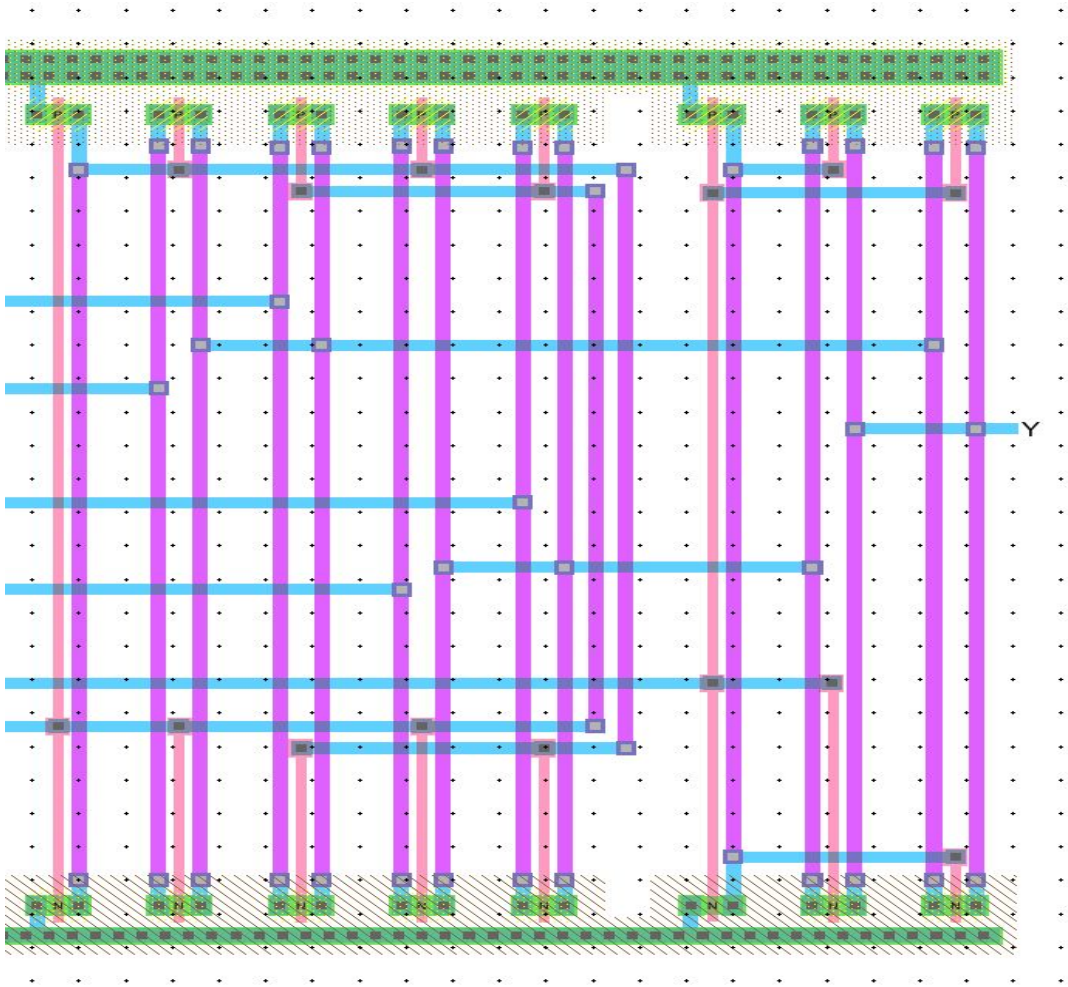

Figure 28: *Electric Layout for 4:1 Multiplexer Output ~ Transmission Gates*

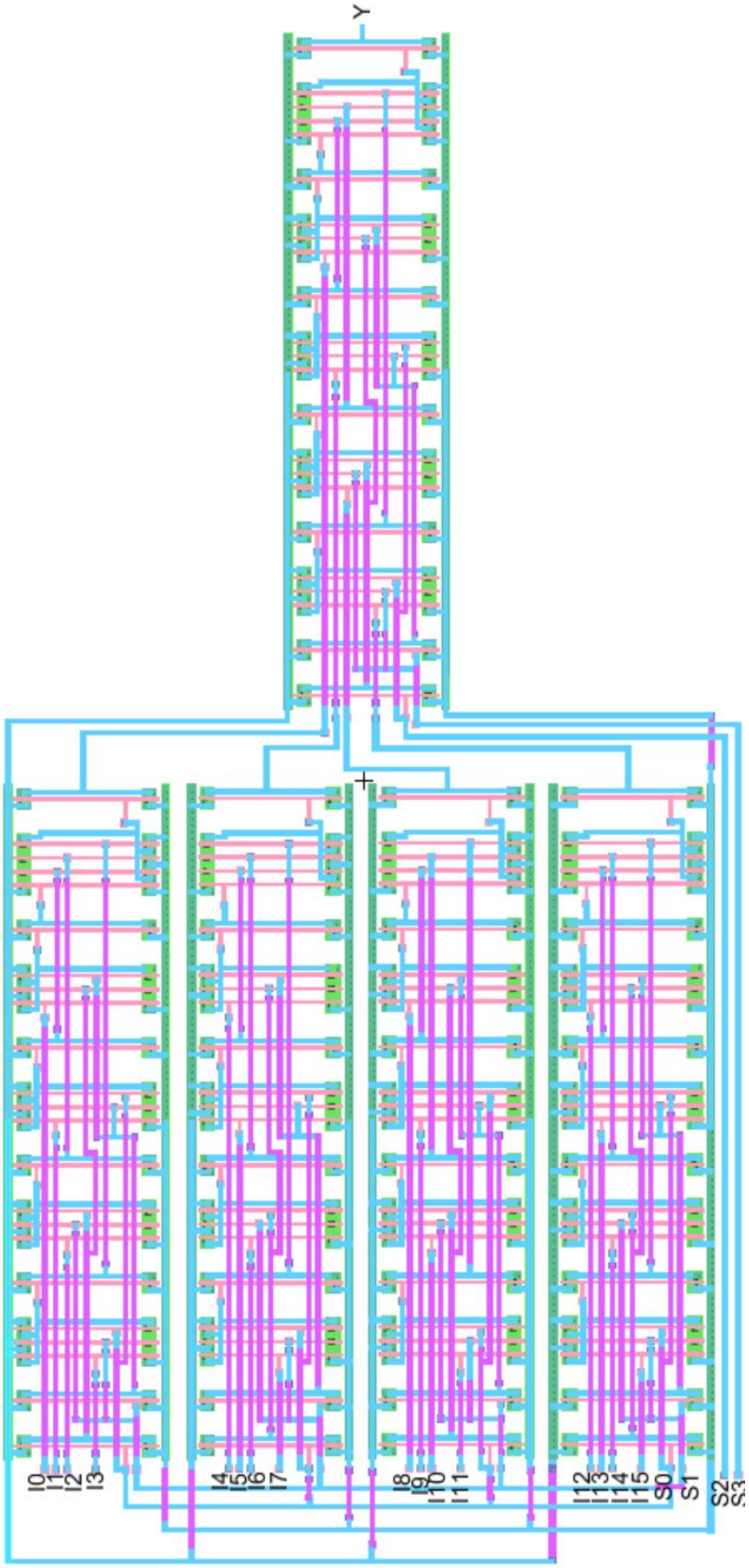

Figure 29: *Electric Layout for 16:1 Multiplexer Input ~ Static CMOS*

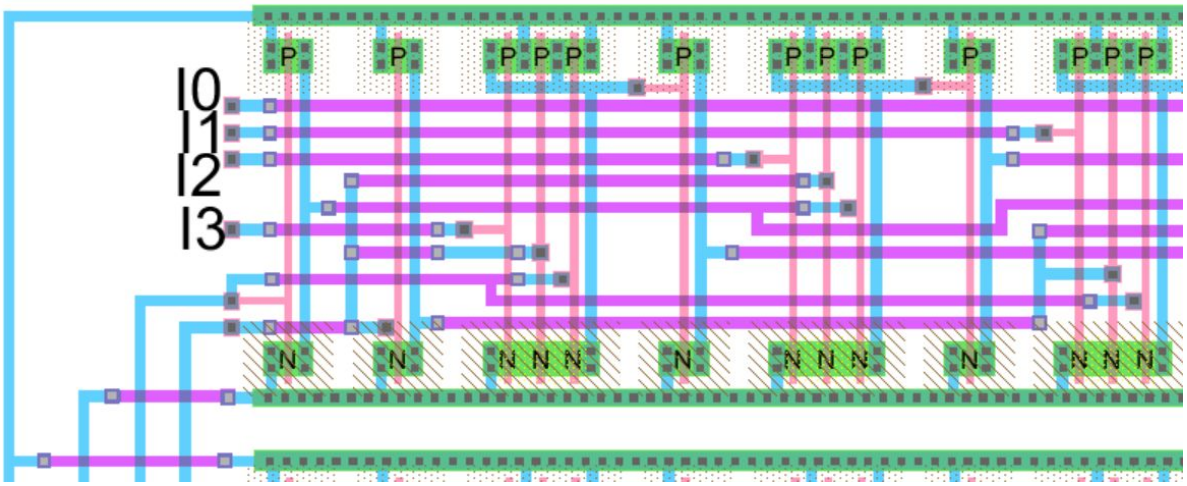

Figure 30: *Electric Layout for 16:1 Multiplexer Input ~ Static CMOS*

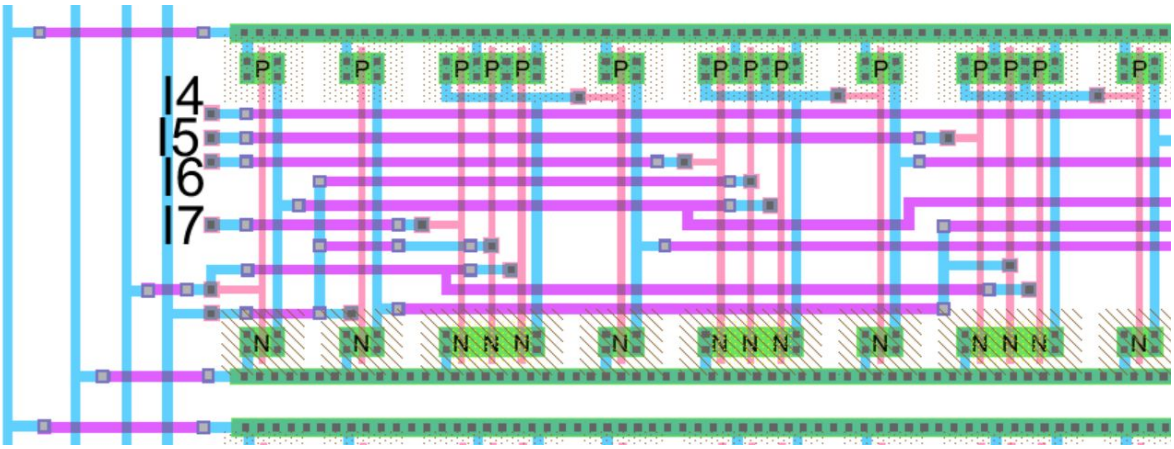

Figure 31: *Electric Layout for 16:1 Multiplexer Input ~ Static CMOS*

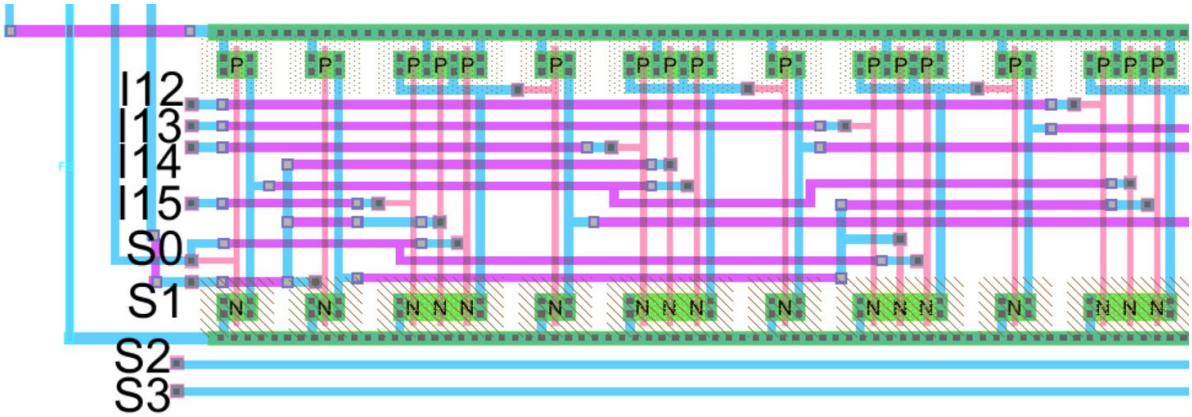

Figure 32: *Electric Layout for 16:1 Multiplexer Input ~ Static CMOS*

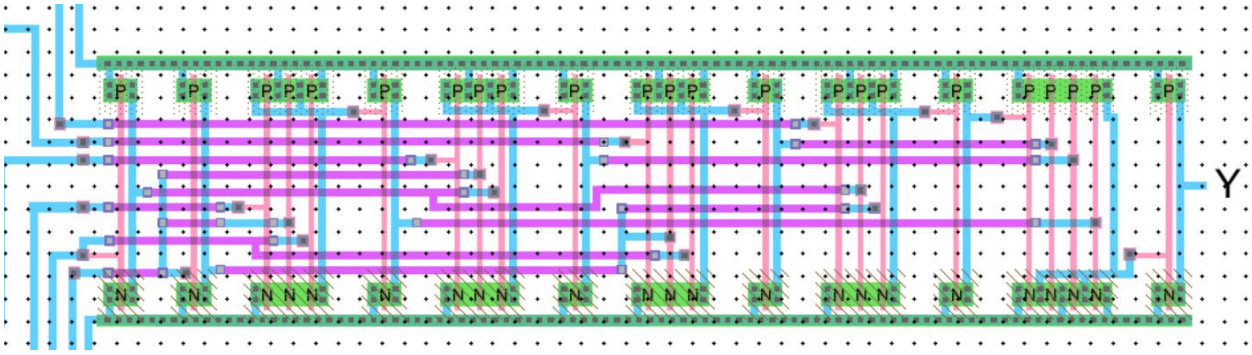

Figure 33: *Electric Layout for 16:1 Multiplexer Input ~ Static CMOS*

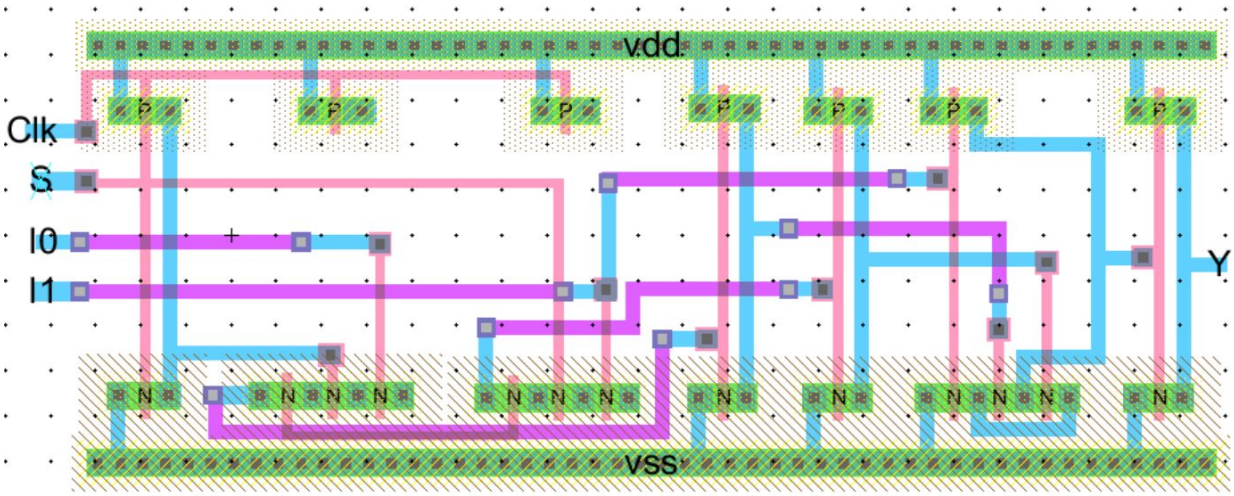

Figure 34: *Electric Layout for 2:1 Multiplexer ~ Dynamic CMOS*

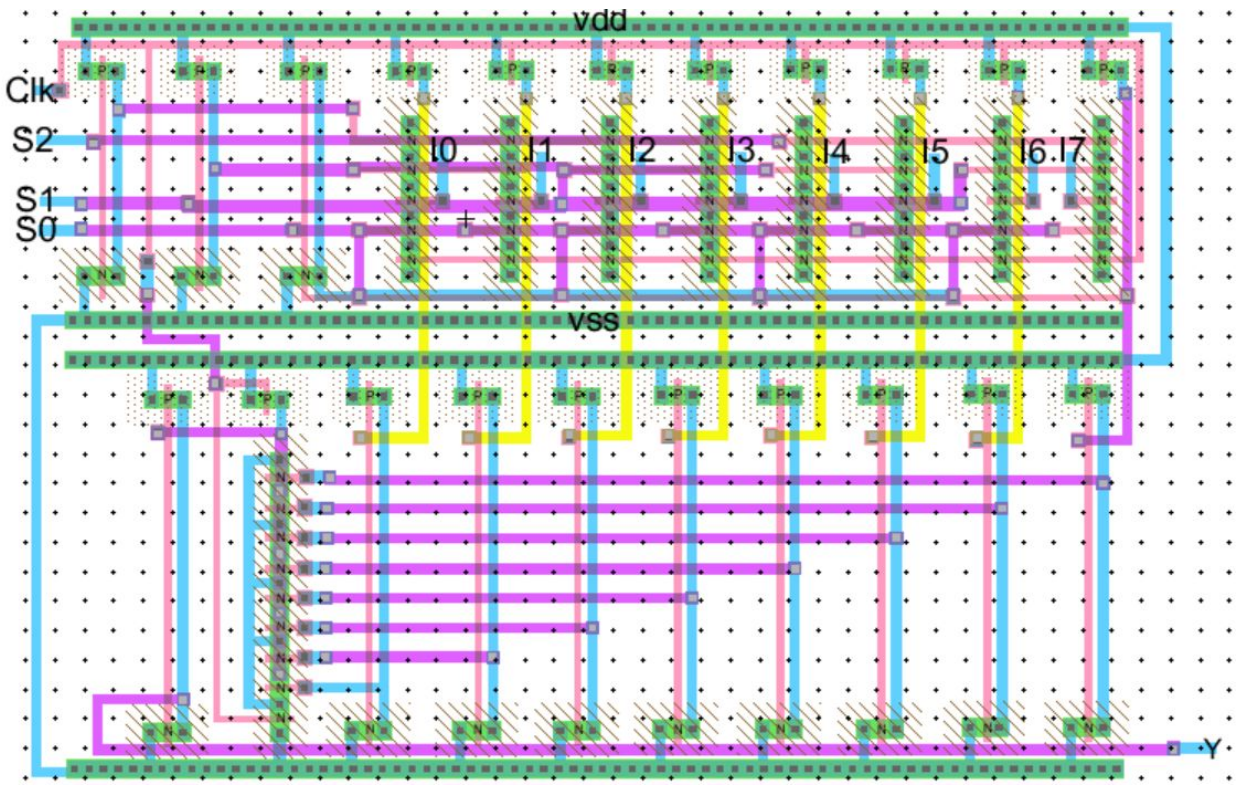

Figure 35: *Electric Layout for 8:1 Multiplexer ~ Dynamic CMOS*

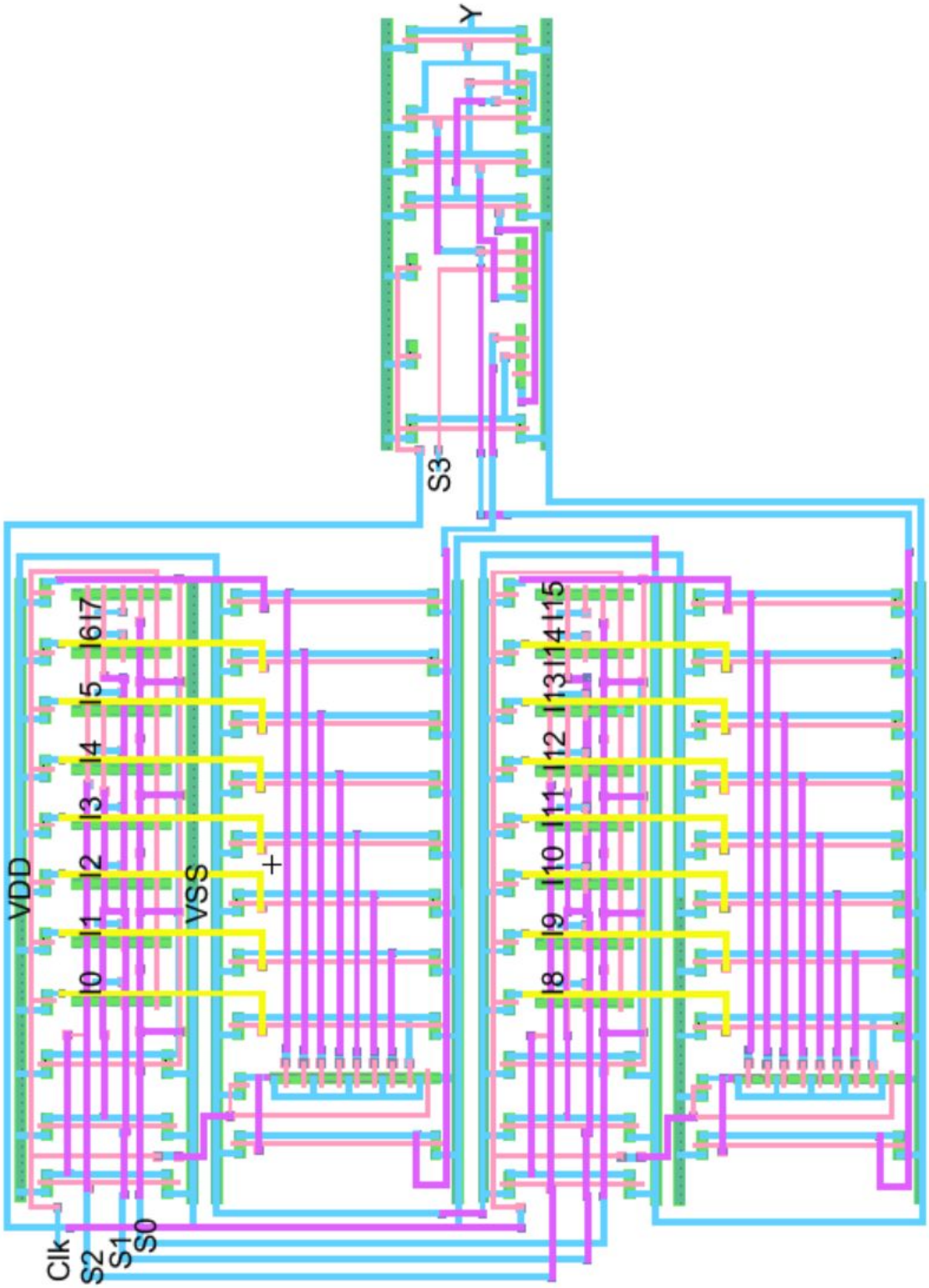

Figure 36: *Electric Layout for 16:1 Multiplexer ~ Dynamic CMOS*

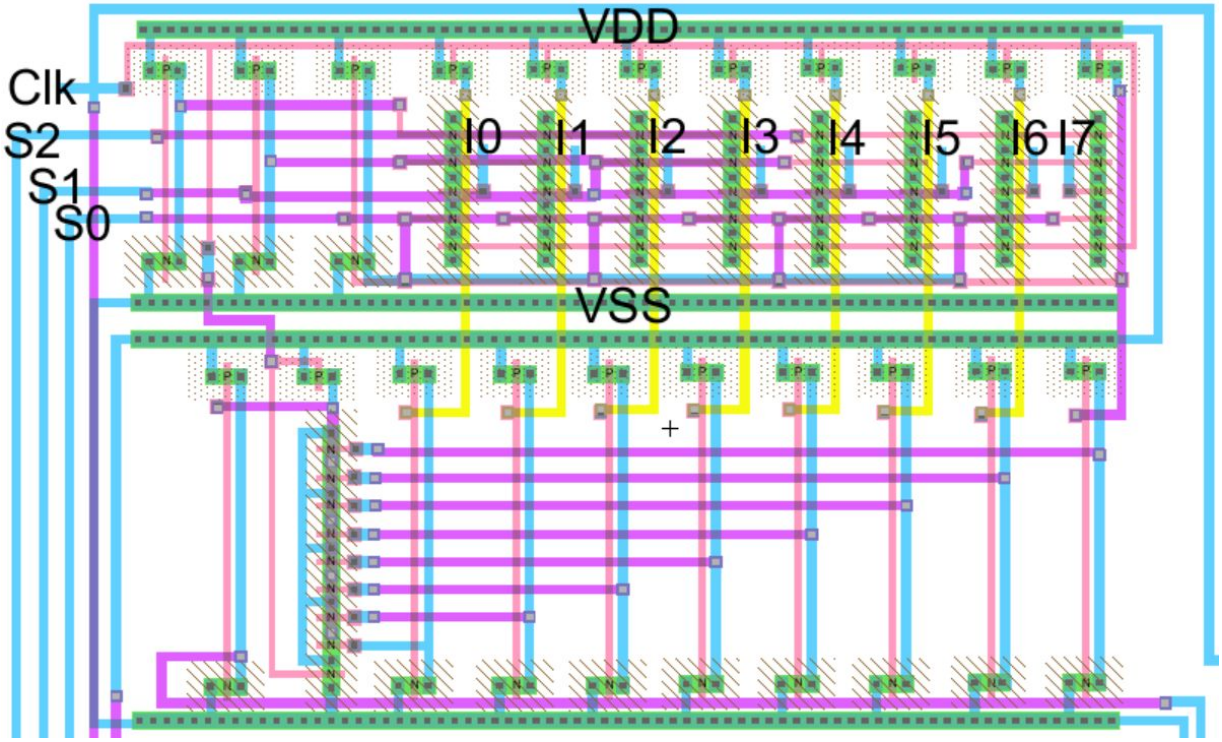

Figure 37: *Electric Layout for 16:1 Multiplexer Input ~ Dynamic CMOS*

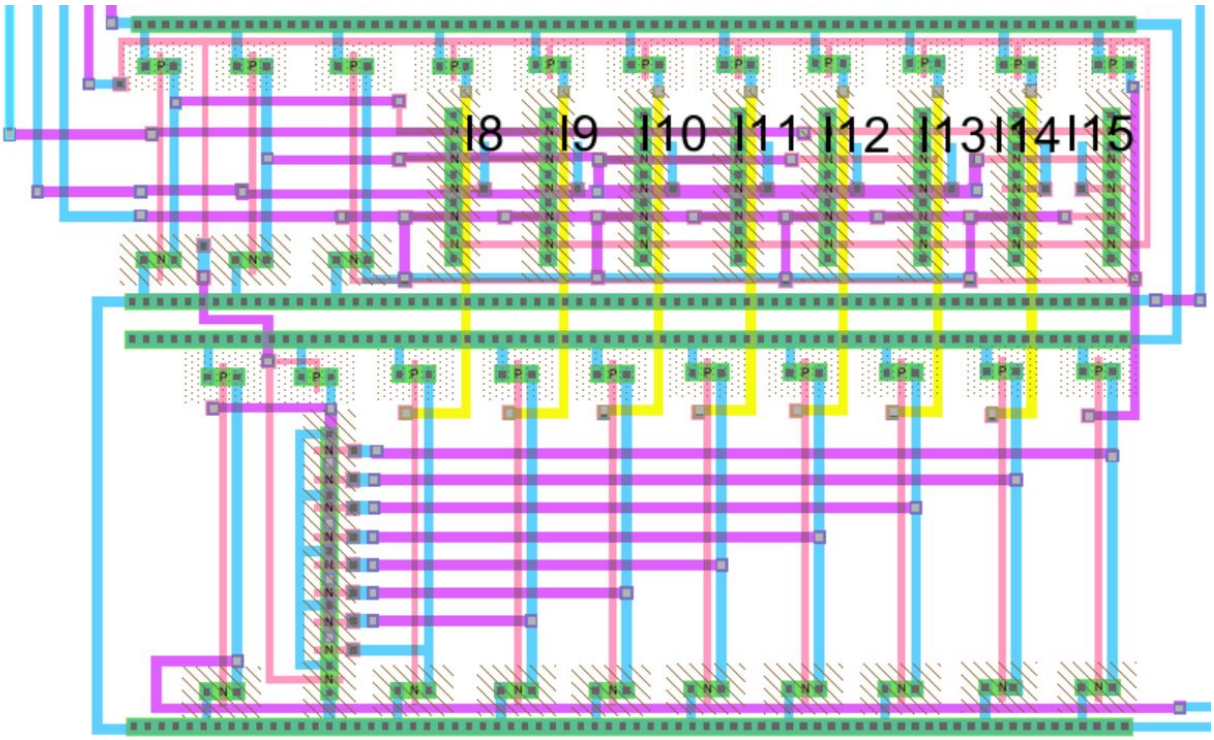

Figure 38: *Electric Layout for 16:1 Multiplexer Input ~ Dynamic CMOS*

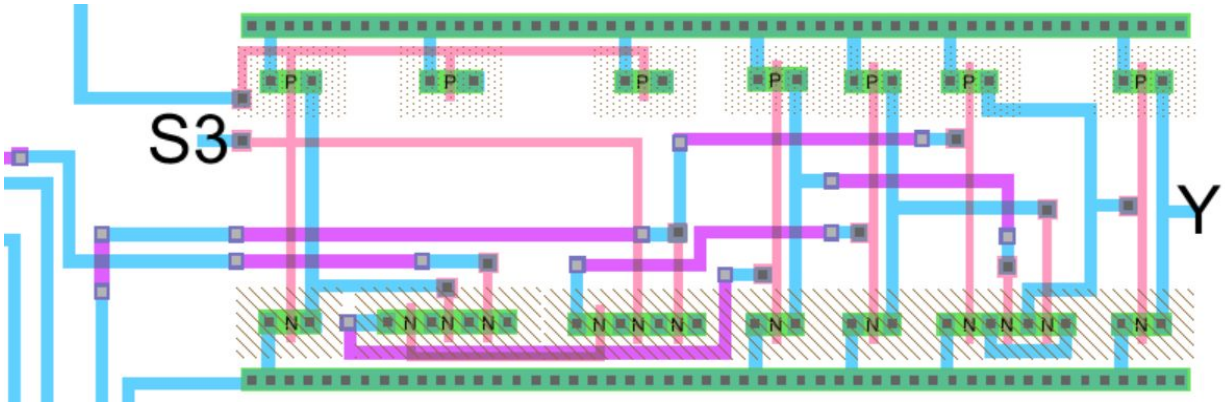

Figure 39: *Electric Layout for 16:1 Multiplexer Output ~ Dynamic CMOS*

5. LTSPICE code and parasitic extractions with calculation analysis

```
vDD  vDD 0 DC 3.3
vSS  vSS 0 DC 0
vI0  I0  0 PWL(0 0   50n 0   50.1n 3.3  100n 3.3  100.1n 0)
vI1  I1  0 PWL(0 0  250n 0  250.1n 3.3  300n 3.3  300.1n 0)
vI2  I2  0 PWL(0 0  450n 0  450.1n 3.3  500n 3.3  500.1n 0)
vI3  I3  0 PWL(0 0  650n 0  650.1n 3.3  700n 3.3  700.1n 0)
vI4  I4  0 PWL(0 0  850n 0  850.1n 3.3  900n 3.3  900.1n 0)
vI5  I5  0 PWL(0 0 1050n 0 1050.1n 3.3 1100n 3.3 1100.1n 0)
vI6  I6  0 PWL(0 0 1250n 0 1250.1n 3.3 1300n 3.3 1300.1n 0)
vI7  I7  0 PWL(0 0 1450n 0 1450.1n 3.3 1500n 3.3 1500.1n 0)
vI8  I8  0 PWL(0 0 1650n 0 1650.1n 3.3 1700n 3.3 1700.1n 0)
vI9  I9  0 PWL(0 0 1850n 0 1850.1n 3.3 1900n 3.3 1900.1n 0)
vI10 I10 0 PWL(0 0 2050n 0 2050.1n 3.3 2100n 3.3 2100.1n 0)
vI11 I11 0 PWL(0 0 2250n 0 2250.1n 3.3 2300n 3.3 2300.1n 0)
vI12 I12 0 PWL(0 0 2450n 0 2450.1n 3.3 2500n 3.3 2500.1n 0)
vI13 I13 0 PWL(0 0 2650n 0 2650.1n 3.3 2700n 3.3 2700.1n 0)
vI14 I14 0 PWL(0 0 2850n 0 2850.1n 3.3 2900n 3.3 2900.1n 0)
vI15 I15 0 PWL(0 0 3050n 0 3050.1n 3.3 3100n 3.3 3100.1n 0)
vS0  S0  0 PULSE(3.3 0 0 0.1n 0.1n 200n  400n)
vS1  S1  0 PULSE(3.3 0 0 0.1n 0.1n 400n  800n)
vS2  S2  0 PULSE(3.3 0 0 0.1n 0.1n 800n  1600n)
vS3  S3  0 PULSE(3.3 0 0 0.1n 0.1n 1600n 3200n)
.tran 0 3200n
.include C:\Electric\technology_model.txt
.END
```

Figure 40: *16:1 Multiplexer SPICE Deck*

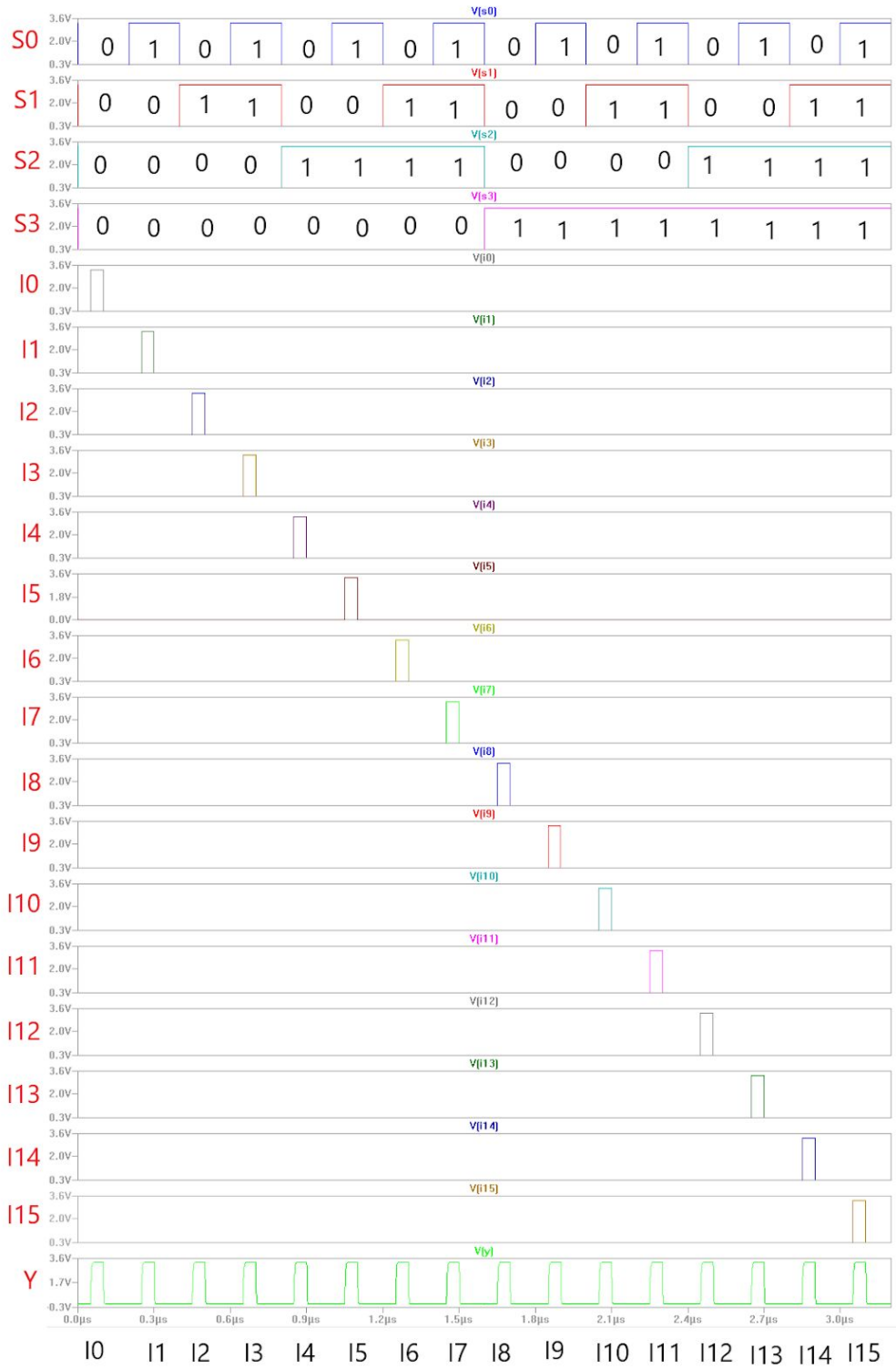

Figure 41: *16:1 Multiplexer Electric Schematic LTspice Simulation ~ Transmission Gate*

```
***    P-Active:    areacap=0.9FF/um^2, edgecap=0.0FF/um,   res=2.5ohms/sq
***    N-Active:    areacap=0.9FF/um^2, edgecap=0.0FF/um,   res=3.0ohms/sq
***    Polysilicon-1:   areacap=0.1467FF/um^2,  edgecap=0.0608FF/um,    res=6.2ohms/sq
***    Polysilicon-2:   areacap=1.0FF/um^2, edgecap=0.0FF/um,   res=50.0ohms/sq
***    Transistor-Poly: areacap=0.09FF/um^2,    edgecap=0.0FF/um,   res=2.5ohms/sq
***    Poly-Cut:    areacap=0.0FF/um^2, edgecap=0.0FF/um,   res=2.2ohms/sq
***    Active-Cut:  areacap=0.0FF/um^2, edgecap=0.0FF/um,   res=2.5ohms/sq
***    Metal-1: areacap=0.1209FF/um^2,  edgecap=0.1104FF/um,    res=0.078ohms/sq
***    Via1:    areacap=0.0FF/um^2, edgecap=0.0FF/um,   res=1.0ohms/sq
***    Metal-2: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,    res=0.078ohms/sq
***    Via2:    areacap=0.0FF/um^2, edgecap=0.0FF/um,   res=0.9ohms/sq
***    Metal-3: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,    res=0.078ohms/sq
***    Via3:    areacap=0.0FF/um^2, edgecap=0.0FF/um,   res=0.8ohms/sq
***    Metal-4: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,    res=0.078ohms/sq
***    Via4:    areacap=0.0FF/um^2, edgecap=0.0FF/um,   res=0.8ohms/sq
***    Metal-5: areacap=0.0843FF/um^2,  edgecap=0.0974FF/um,    res=0.078ohms/sq
***    Via5:    areacap=0.0FF/um^2, edgecap=0.0FF/um,   res=0.8ohms/sq
***    Metal-6: areacap=0.0423FF/um^2,  edgecap=0.1273FF/um,    res=0.036ohms/sq
***    Hi-Res:  areacap=0.0FF/um^2, edgecap=0.0FF/um,   res=1.0ohms/sq

** Extracted Parasitic Capacitors ***
C0 net@9 0 4.797fF
C1 net@9#2contact@5_metal-1-p-act 0 31.422fF
C2 I1 0 7.521fF
C3 I1#0contact@7_metal-1-n-act 0 4.107fF
C4 net@7 0 4.092fF
C5 net@7#2contact@9_metal-1-p-act 0 20.438fF
C6 S0 0 27.421fF
C7 I0 0 9.241fF
C8 I0#2contact@24_metal-1-metal-2 0 4.232fF
C9 net@7#5contact@22_metal-1-n-act 0 4.082fF
C10 net@9#9contact@26_metal-1-polysilicon-1 0 24fF
C11 S0#6contact@29_metal-1-polysilicon-1 0 23.374fF
C12 I3 0 10.399fF
C13 I3#0contact@38_metal-1-n-act 0 3.866fF
C14 net@128#6contact@39_metal-1-n-act 0 3.852fF
C15 net@128 0 22.652fF
C16 I2 0 12.043fF
C17 I2#2contact@52_metal-1-metal-2 0 3.992fF
C18 net@128#2contact@55_metal-1-metal-2 0 3.841fF
C19 net@188#5contact@79_metal-1-metal-2 0 4.797fF
C20 net@188 0 20.457fF
C21 net@128#16contact@69_metal-1-p-act 0 15.199fF
C22 net@128#14contact@70_metal-1-n-act 0 3.866fF
C23 net@180#6contact@71_metal-1-n-act 0 3.957fF
C24 net@180 0 19.234fF
C25 S1#1contact@73_metal-1-polysilicon-1 0 7.897fF
C26 S1#0contact@76_metal-1-polysilicon-1 0 21.836fF
C27 net@74#4contact@88_metal-1-metal-2 0 13.215fF
C28 net@74#6contact@87_metal-1-metal-2 0 4.096fF
C29 net@180#2contact@90_metal-1-metal-2 0 3.946fF
C30 net@188#8contact@89_metal-1-polysilicon-1 0 13.008fF
C31 S1#6contact@92_metal-1-polysilicon-1 0 12.374fF
C32 net@245 0 17.797fF
C33 net@242 0 25.209fF
C34 net@248 0 12.872fF
C35 net@248#2contact@116_metal-1-metal-2 0 3.594fF
C36 I5 0 13.282fF
C37 I5#0contact@131_metal-1-n-act 0 3.594fF
C38 net@248#12contact@137_metal-1-metal-2 0 3.59fF
C39 net@248#7contact@133_metal-1-p-act 0 20.597fF
C40 I4#0contact@146_metal-1-metal-2 0 10.576fF
C41 I4#2contact@145_metal-1-metal-2 0 3.73fF
C42 net@248#14contact@148_metal-1-metal-2 0 3.58fF
C43 I7#0contact@159_metal-1-n-act 0 14.725fF
C44 net@245#7contact@177_metal-1-metal-2 0 29.077fF
C45 I6#0contact@174_metal-1-metal-2 0 15.6fF
C46 net@366#5contact@197_metal-1-metal-2 0 4.797fF
C47 net@366 0 14.841fF
C48 net@242#14contact@188_metal-1-n-act 0 13.929fF
C49 net@362#6contact@189_metal-1-n-act 0 3.685fF
C50 net@362 0 26.656fF
C51 S2#1contact@191_metal-1-polysilicon-1 0 21.273fF
C52 net@180#14contact@206_metal-1-metal-2 0 11.865fF
C53 net@180#16contact@205_metal-1-metal-2 0 3.971fF
C54 net@362#2contact@208_metal-1-metal-2 0 3.674fF
C55 net@366#8contact@207_metal-1-polysilicon-1 0 7.331fF
C56 S2#6contact@210_metal-1-polysilicon-1 0 6.722fF
C57 I9#0contact@438_metal-1-metal-2 0 16.031fF
C58 net@717 0 29.674fF
C59 I8#0contact@449_metal-1-metal-2 0 16.906fF
C60 I11#0contact@453_metal-1-n-act 0 17.324fF
C61 net@724 0 27.734fF
C62 I10#0contact@467_metal-1-metal-2 0 18.199fF
C63 net@724#14contact@481_metal-1-n-act 0 16.454fF
C64 net@761 0 25.844fF
C65 net@717#4contact@499_metal-1-metal-2 0 18.373fF
C66 net@809 0 15.16fF
C67 net@806 0 36.527fF
C68 net@812 0 17.08fF
C69 I13#0contact@537_metal-1-n-act 0 18.618fF
C70 net@812#7contact@539_metal-1-p-act 0 28.381fF
C71 I12#0contact@552_metal-1-metal-2 0 19.492fF
C72 I15#0contact@565_metal-1-n-act 0 16.603fF
C73 net@809#7contact@583_metal-1-metal-2 0 26.441fF
C74 I14#0contact@580_metal-1-metal-2 0 17.179fF
C75 net@930 0 33.84fF
C76 net@761#14contact@612_metal-1-metal-2 0 14.543fF
C77 net@1020#6contact@648_metal-1-polysilicon-1 0 7.437fF
C78 net@1020 0 6.168fF
C79 Y 0 21.64fF
C80 S3#0contact@632_metal-1-polysilicon-1 0 12.156fF
C81 net@362#14contact@646_metal-1-metal-2 0 3.709fF
C82 S3#5contact@651_metal-1-polysilicon-1 0 2.818fF
C83 S1 0 15.87fF
C84 I4 0 4.34fF
C85 I7 0 4.738fF
C86 I6 0 5.634fF
C87 S2 0 11.765fF
C88 I9 0 6.044fF
C89 I8 0 6.94fF
C90 I10 0 8.233fF
C91 I11 0 7.338fF
C92 I13 0 8.631fF
C93 I12 0 9.527fF
C94 I15 0 6.616fF
C95 I14 0 7.213fF
C96 S3 0 10.565fF
```

Figure 42: *16:1 Multiplexer LTspice Parasitic Extraction (Capacitance) & Resistance and Capacitance Per um^2 ~ Transmission Gate Layout*

```
** Extracted Parasitic Resistors ***
R0 S0#0pmos01_poly-left S0#0pmos01_poly-left##0 9.94
R1 S0#0pmos01_poly-left##0 S0#0pmos01_poly-left##1 9.94
R2 S0#0pmos01_poly-left##1 S0#0pmos01_poly-left##2 9.94
R3 S0#0pmos01_poly-left##2 S0#0pmos01_poly-left##3 9.94
R4 S0#0pmos01_poly-left##3 S0#0pmos01_poly-left##4 9.94
R5 S0#0pmos01_poly-left##4 S0#0pmos01_poly-left##5 9.94
R6 S0#0pmos01_poly-left##5 S0#0pmos01_poly-left##6 9.94
R7 S0#0pmos01_poly-left##6 S0#0pmos01_poly-left##7 9.94
R8 S0#0pmos01_poly-left##7 S0#0pmos01_poly-left##8 9.94
R9 S0#0pmos01_poly-left##8 S0#0pmos01_poly-left##9 9.94
R10 S0#0pmos01_poly-left##9 S0#0pmos01_poly-left##10 9.94
R11 S0#0pmos01_poly-left##10 S0#0pmos01_poly-left##11 9.94
R12 S0#0pmos01_poly-left##11 S0#0pmos01_poly-left##12 9.94
R13 S0#0pmos01_poly-left##12 S0#0pmos01_poly-left##13 9.94
R14 S0#0pmos01_poly-left##13 S0#0pmos01_poly-left##14 9.94
R15 S0#0pmos01_poly-left##14 S0#0pmos01_poly-left##15 9.94
R16 S0#0pmos01_poly-left##15 S0#0pmos01_poly-left##16 9.94
R17 S0#0pmos01_poly-left##16 S0#0pmos01_poly-left##17 9.94
R18 S0#0pmos01_poly-left##17 S0#0pmos01_poly-left##18 9.94
R19 S0#0pmos01_poly-left##18 S0#0pmos01_poly-left##19 9.94
R20 S0#0pmos01_poly-left##19 S0#0pmos01_poly-left##20 9.94
R21 S0#0pmos01_poly-left##20 S0#0pmos01_poly-left##21 9.94
R22 S0#0pmos01_poly-left##21 S0#0pmos01_poly-left##22 9.94
R23 S0#0pmos01_poly-left##22 S0#0pmos01_poly-left##23 9.94
R24 S0#0pmos01_poly-left##23 S0#0pmos01_poly-left##24 9.94
R25 S0#0pmos01_poly-left##24 S0#0pmos01_poly-left##25 9.94
R26 S0#0pmos01_poly-left##25 S0#0pmos01_poly-left##26 9.94
R27 S0#0pmos01_poly-left##26 S0#0pmos01_poly-left##27 9.94
R28 S0#0pmos01_poly-left##27 S0#0pmos01_poly-left##28 9.94
R29 S0#0pmos01_poly-left##28 S0#0pmos01_poly-left##29 9.94
R30 S0#0pmos01_poly-left##29 S0#0pmos01_poly-left##30 9.94
R31 S0#0pmos01_poly-left##30 S0#0pmos01_poly-left##31 9.94
R32 S0#0pmos01_poly-left##31 S0#0pmos01_poly-left##32 9.94
R33 S0#0pmos01_poly-left##32 S0#0pmos01_poly-left##33 9.94
R34 S0#0pmos01_poly-left##33 S0#0pmos01_poly-left##34 9.94
R35 S0#0pmos01_poly-left##34 S0#0pmos01_poly-left##35 9.94
R36 S0#0pmos01_poly-left##35 S0#0pmos01_poly-left##36 9.94
R37 S0#0pmos01_poly-left##36 S0#0pmos01_poly-left##37 9.94
R38 S0#0pmos01_poly-left##37 S0#0pmos01_poly-left##38 9.94
R39 S0#0pmos01_poly-left##38 S0#0pmos01_poly-left##39 9.94
R40 S0#0pmos01_poly-left##39 S0#0pmos01_poly-left##40 9.94
R41 S0#0pmos01_poly-left##40 S0#0pmos01_poly-left##41 9.94
R42 S0#0pmos01_poly-left##41 S0#0pmos01_poly-left##42 9.94
R43 S0#0pmos01_poly-left##42 S0#0pmos01_poly-left##43 9.94
R44 S0#0pmos01_poly-left##43 S0#0pmos01_poly-left##44 9.94
R45 S0#0pmos01_poly-left##44 S0#0pmos01_poly-left##45 9.94
R46 S0#0pmos01_poly-left##45 S0#0pmos01_poly-left##46 9.94
R47 S0#0pmos01_poly-left##46 S0#0pmos01_poly-left##47 9.94
R48 S0#0pmos01_poly-left##47 S0#0pmos01_poly-left##48 9.94
R49 S0#0pmos01_poly-left##48 S0#0pmos01_poly-left##49 9.94
R50 S0#0pmos01_poly-left##49 S0#0pmos01_poly-left##50 9.94
R51 S0#0pmos01_poly-left##50 S0#0pmos01_poly-left##51 9.94
R52 S0#0pmos01_poly-left##51 S0#0pmos01_poly-left##52 9.94
R53 S0#0pmos01_poly-left##52 S0#0pmos01_poly-left##53 9.94
R54 S0#0pmos01_poly-left##53 S0#0pmos01_poly-left##54 9.94
R55 S0#0pmos01_poly-left##54 S0#0pmos01_poly-left##55 9.94
R56 S0#0pmos01_poly-left##55 S0#0pmos01_poly-left##56 9.94
R57 S0#0pmos01_poly-left##56 S0#0pmos01_poly-left##57 9.94
R58 S0#0pmos01_poly-left##57 S0#0pmos01_poly-left##58 9.94
R59 S0#0pmos01_poly-left##58 S0#0pmos01_poly-left##59 9.94
R60 S0#0pmos01_poly-left##59 S0#0pmos01_poly-left##60 9.94
R61 S0#0pmos01_poly-left##60 S0#0pmos01_poly-left##61 9.94
R62 S0#0pmos01_poly-left##61 S0 9.94
R63 S0 S0##0 8.913
R64 S0##0 S0##1 8.913
R65 S0##1 S0##2 8.913
R66 S0##2 S0##3 8.913
R67 S0##3 S0##4 8.913
R68 S0##4 S0##5 8.913
R69 S0##5 S0##6 8.913
R70 S0##6 S0#2nmos00_poly-right 8.913
R71 S0#3nmos01_poly-right S0#3nmos01_poly-right##0 8.913
R72 S0#3nmos01_poly-right##0 S0#3nmos01_poly-right##1 8.913
R73 S0#3nmos01_poly-right##1 S0#3nmos01_poly-right##2 8.913
R74 S0#3nmos01_poly-right##2 S0#3nmos01_poly-right##3 8.913
R75 S0#3nmos01_poly-right##3 S0#3nmos01_poly-right##4 8.913
R76 S0#3nmos01_poly-right##4 S0#3nmos01_poly-right##5 8.913
R77 S0#3nmos01_poly-right##5 S0#3nmos01_poly-right##6 8.913
R78 S0#3nmos01_poly-right##6 S0 8.913
R79 net09#4pmos00_poly-left net09#4pmos00_poly-left##0 7.75
R80 net09#4pmos00_poly-left##0 net09#4pmos00_poly-left##1 7.75
R81 net09#4pmos00_poly-left##1 net09#4pmos00_poly-left##2 7.75
R82 net09#4pmos00_poly-left##2 net09#2contact05_metal-1-p-act 7.75
R83 net09#2contact05_metal-1-p-act net09 5.499
R84 I1 I1#0contact07_metal-1-n-act 4.641
R85 I0 I0#2contact024_metal-1-metal-2 4.797
R86 net09#8nmos02_poly-right net09#8nmos02_poly-right##0 9.92
R87 net09#8nmos02_poly-right##0 net09#8nmos02_poly-right##1 9.92
R88 net09#8nmos02_poly-right##1 net09#8nmos02_poly-right##2 9.92
R89 net09#8nmos02_poly-right##2 net09#8nmos02_poly-right##3 9.92
R90 net09#8nmos02_poly-right##3 net09#9contact026_metal-1-polysilicon-1 9.92
R91 S0#5pmos02_poly-left S0#5pmos02_poly-left##0 9.61
R92 S0#5pmos02_poly-left##0 S0#5pmos02_poly-left##1 9.61
R93 S0#5pmos02_poly-left##1 S0#5pmos02_poly-left##2 9.61
R94 S0#5pmos02_poly-left##2 S0#5pmos02_poly-left##3 9.61
R95 S0#5pmos02_poly-left##3 S0#6contact029_metal-1-polysilicon-1 9.61
R96 net07#2contact09_metal-1-p-act net07 4.654
R97 net07#2contact09_metal-1-p-act net07#5contact022_metal-1-n-act 4.641
R98 net0128 net0128#2contact055_metal-1-metal-2 4.342
R99 net09#10pmos03_poly-left net09#10pmos03_poly-left##0 7.75
R100 net09#10pmos03_poly-left##0 net09#10pmos03_poly-left##1 7.75
R101 net09#10pmos03_poly-left##1 net09#10pmos03_poly-left##2 7.75
R102 net09#10pmos03_poly-left##2 net09#2contact05_metal-1-p-act 7.75
R103 I3 I3#0contact038_metal-1-n-act 4.342
R104 I2 I2#2contact052_metal-1-metal-2 4.498
R105 net09#12nmos04_poly-right net09#12nmos04_poly-right##0 9.92
R106 net09#12nmos04_poly-right##0 net09#12nmos04_poly-right##1 9.92
R107 net09#12nmos04_poly-right##1 net09#12nmos04_poly-right##2 9.92
R108 net09#12nmos04_poly-right##2 net09#12nmos04_poly-right##3 9.92
R109 net09#12nmos04_poly-right##3 net09#9contact026_metal-1-polysilicon-1 9.92
R110 S0#7pmos04_poly-left S0#7pmos04_poly-left##0 9.61
```

```
R672 S3#2nmos052_poly-right##10 S3#2nmos052_poly-right##11 9.533
R673 S3#2nmos052_poly-right##11 S3#2nmos052_poly-right##12 9.533
R674 S3#2nmos052_poly-right##12 S3#2nmos052_poly-right##13 9.533
R675 S3#2nmos052_poly-right##13 S3#2nmos052_poly-right##14 9.533
R676 S3#2nmos052_poly-right##14 S3#2nmos052_poly-right##15 9.533
R677 S3#2nmos052_poly-right##15 S3#2nmos052_poly-right##16 9.533
R678 S3#2nmos052_poly-right##16 S3#2nmos052_poly-right##17 9.533
R679 S3#2nmos052_poly-right##17 S3#2nmos052_poly-right##18 9.533
R680 S3#2nmos052_poly-right##18 S3#0contact0632_metal-1-polysilicon-1 9.533
R681 net0102#3pmos051_poly-left net0102#3pmos051_poly-left##0 7.75
R682 net0102#3pmos051_poly-left##0 net0102#3pmos051_poly-left##1 7.75
R683 net0102#3pmos051_poly-left##1 net0102#3pmos051_poly-left##2 7.75
R684 net0102#3pmos051_poly-left##2 net0102# 7.75
R685 net0102#5nmos053_poly-right net0102#5nmos053_poly-right##0 7.75
R686 net0102#5nmos053_poly-right##0 net0102#5nmos053_poly-right##1 7.75
R687 net0102#5nmos053_poly-right##1 net0102#5nmos053_poly-right##2 7.75
R688 net0102#5nmos053_poly-right##2 net0102#6contact0648_metal-1-polysilicon-1 7.75
R689 S3#4pmos053_poly-left S3#4pmos053_poly-left##0 9.92
R690 S3#4pmos053_poly-left##0 S3#4pmos053_poly-left##1 9.92
R691 S3#4pmos053_poly-left##1 S3#4pmos053_poly-left##2 9.92
R692 S3#4pmos053_poly-left##2 S3#4pmos053_poly-left##3 9.92
R693 S3#4pmos053_poly-left##3 S3#5contact0651_metal-1-polysilicon-1 9.92
R694 S3#0contact0632_metal-1-polysilicon-1 S3#0contact0632_metal-1-polysilicon-1##0 7.362
C103 S3#0contact0632_metal-1-polysilicon-1##0 0 10.565fF
R695 S3#0contact0632_metal-1-polysilicon-1##0 S3#0contact0632_metal-1-polysilicon-1##1 7.362
C104 S3#0contact0632_metal-1-polysilicon-1##1 0 10.565fF
R696 S3#0contact0632_metal-1-polysilicon-1##1 S3 7.362
R697 net0717 net0717#4contact0499_metal-1-metal-2 8.788
R698 net0724 net0724#1contact0481_metal-1-n-act 6.76
R699 net0812#7contact0539_metal-1-p-act net0812 7.436
R700 net0809#7contact0583_metal-1-metal-2 net0809 5.408
R701 net07#2contact09_metal-1-p-act net07#2contact09_metal-1-p-act##0 5.759
C105 net07#2contact09_metal-1-p-act##0 0 7.346fF
R702 net07#2contact09_metal-1-p-act##0 net07#1#4contact088_metal-1-metal-2 5.759
R703 net0128 net0128#1#contact069_metal-1-p-act 9.49
R704 net0362#1#contact0646_metal-1-metal-2 net0362 4.147
R705 net01020 net01020#6contact0648_metal-1-polysilicon-1 5.304
R706 S3#6pmos052_poly-left S3#6pmos052_poly-left##0 9.92
R707 S3#6pmos052_poly-left##0 S3#6pmos052_poly-left##1 9.92
R708 S3#6pmos052_poly-left##1 S3#6pmos052_poly-left##2 9.92
R709 S3#6pmos052_poly-left##2 S3#6pmos052_poly-left##3 9.92
R710 S3#6pmos052_poly-left##3 S3#5contact0651_metal-1-polysilicon-1 9.92
R711 S3#5contact0651_metal-1-polysilicon-1 S3#5contact0651_metal-1-polysilicon-1##0 9.94
R712 S3#5contact0651_metal-1-polysilicon-1##0 S3#5contact0651_metal-1-polysilicon-1##1 9.94
R713 S3#5contact0651_metal-1-polysilicon-1##1 S3#5contact0651_metal-1-polysilicon-1##2 9.94
R714 S3#5contact0651_metal-1-polysilicon-1##2 S3#5contact0651_metal-1-polysilicon-1##3 9.94
R715 S3#5contact0651_metal-1-polysilicon-1##3 S3#5contact0651_metal-1-polysilicon-1##4 9.94
R716 S3#5contact0651_metal-1-polysilicon-1##4 S3#5contact0651_metal-1-polysilicon-1##5 9.94
R717 S3#5contact0651_metal-1-polysilicon-1##5 S3#5contact0651_metal-1-polysilicon-1##6 9.94
R718 S3#5contact0651_metal-1-polysilicon-1##6 S3#5contact0651_metal-1-polysilicon-1##7 9.94
R719 S3#5contact0651_metal-1-polysilicon-1##7 S3#5contact0651_metal-1-polysilicon-1##8 9.94
R720 S3#5contact0651_metal-1-polysilicon-1##8 S3#5contact0651_metal-1-polysilicon-1##9 9.94
R721 S3#5contact0651_metal-1-polysilicon-1##9 S3#5contact0651_metal-1-polysilicon-1##10 9.94
R722 S3#5contact0651_metal-1-polysilicon-1##10 S3#5contact0651_metal-1-polysilicon-1##11 9.94
R723 S3#5contact0651_metal-1-polysilicon-1##11 S3#5contact0651_metal-1-polysilicon-1##12 9.94
R724 S3#5contact0651_metal-1-polysilicon-1##12 S3#5contact0651_metal-1-polysilicon-1##13 9.94
R725 S3#5contact0651_metal-1-polysilicon-1##13 S3#5contact0651_metal-1-polysilicon-1##14 9.94
R726 S3#5contact0651_metal-1-polysilicon-1##14 S3#5contact0651_metal-1-polysilicon-1##15 9.94
R727 S3#5contact0651_metal-1-polysilicon-1##15 S3#5contact0651_metal-1-polysilicon-1##16 9.94
R728 S3#5contact0651_metal-1-polysilicon-1##16 S3#5contact0651_metal-1-polysilicon-1##17 9.94
R729 S3#5contact0651_metal-1-polysilicon-1##17 S3#5contact0651_metal-1-polysilicon-1##18 9.94
R730 S3#5contact0651_metal-1-polysilicon-1##18 S3#5contact0651_metal-1-polysilicon-1##19 9.94
R731 S3#5contact0651_metal-1-polysilicon-1##19 S3#5contact0651_metal-1-polysilicon-1##20 9.94
R732 S3#5contact0651_metal-1-polysilicon-1##20 S3#5contact0651_metal-1-polysilicon-1##21 9.94
R733 S3#5contact0651_metal-1-polysilicon-1##21 S3#5contact0651_metal-1-polysilicon-1##22 9.94
R734 S3#5contact0651_metal-1-polysilicon-1##22 S3#5contact0651_metal-1-polysilicon-1##23 9.94
R735 S3#5contact0651_metal-1-polysilicon-1##23 S3#5contact0651_metal-1-polysilicon-1##24 9.94
R736 S3#5contact0651_metal-1-polysilicon-1##24 S3#5contact0651_metal-1-polysilicon-1##25 9.94
R737 S3#5contact0651_metal-1-polysilicon-1##25 S3#5contact0651_metal-1-polysilicon-1##26 9.94
R738 S3#5contact0651_metal-1-polysilicon-1##26 S3#5contact0651_metal-1-polysilicon-1##27 9.94
R739 S3#5contact0651_metal-1-polysilicon-1##27 S3#5contact0651_metal-1-polysilicon-1##28 9.94
R740 S3#5contact0651_metal-1-polysilicon-1##28 S3#5contact0651_metal-1-polysilicon-1##29 9.94
R741 S3#5contact0651_metal-1-polysilicon-1##29 S3#5contact0651_metal-1-polysilicon-1##30 9.94
R742 S3#5contact0651_metal-1-polysilicon-1##30 S3#5contact0651_metal-1-polysilicon-1##31 9.94
R743 S3#5contact0651_metal-1-polysilicon-1##31 S3#5contact0651_metal-1-polysilicon-1##32 9.94
R744 S3#5contact0651_metal-1-polysilicon-1##32 S3#5contact0651_metal-1-polysilicon-1##33 9.94
R745 S3#5contact0651_metal-1-polysilicon-1##33 S3#5contact0651_metal-1-polysilicon-1##34 9.94
R746 S3#5contact0651_metal-1-polysilicon-1##34 S3#5contact0651_metal-1-polysilicon-1##35 9.94
R747 S3#5contact0651_metal-1-polysilicon-1##35 S3#5contact0651_metal-1-polysilicon-1##36 9.94
R748 S3#5contact0651_metal-1-polysilicon-1##36 S3#5contact0651_metal-1-polysilicon-1##37 9.94
R749 S3#5contact0651_metal-1-polysilicon-1##37 S3#5contact0651_metal-1-polysilicon-1##38 9.94
R750 S3#5contact0651_metal-1-polysilicon-1##38 S3#5contact0651_metal-1-polysilicon-1##39 9.94
R751 S3#5contact0651_metal-1-polysilicon-1##39 S3#5contact0651_metal-1-polysilicon-1##40 9.94
R752 S3#5contact0651_metal-1-polysilicon-1##40 S3#5contact0651_metal-1-polysilicon-1##41 9.94
R753 S3#5contact0651_metal-1-polysilicon-1##41 S3#5contact0651_metal-1-polysilicon-1##42 9.94
R754 S3#5contact0651_metal-1-polysilicon-1##42 S3#5contact0651_metal-1-polysilicon-1##43 9.94
R755 S3#5contact0651_metal-1-polysilicon-1##43 S3#5contact0651_metal-1-polysilicon-1##44 9.94
R756 S3#5contact0651_metal-1-polysilicon-1##44 S3#0contact0632_metal-1-polysilicon-1 9.94
```

Figure 43: *16:1 Multiplexer LTspice Parasitic Extraction (Resistors) R0 - R110:R672 - R756 ~ Transmission Gate Layout*

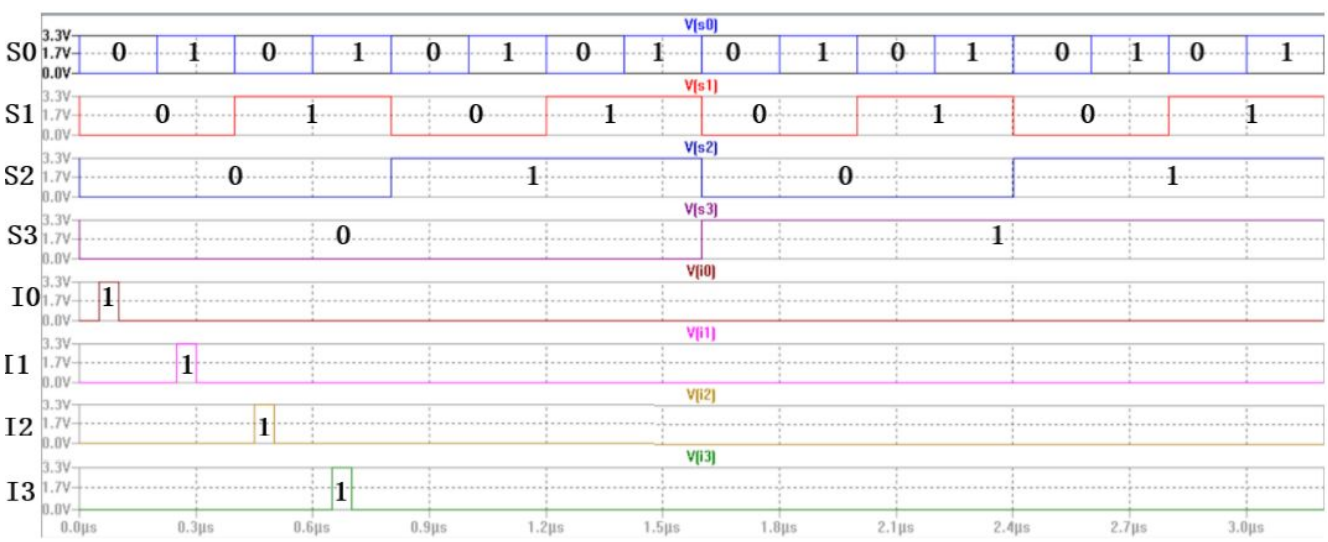

Figure 44: *16:1 Multiplexer Electric Schematic LTspice Simulation ~ Static CMOS*

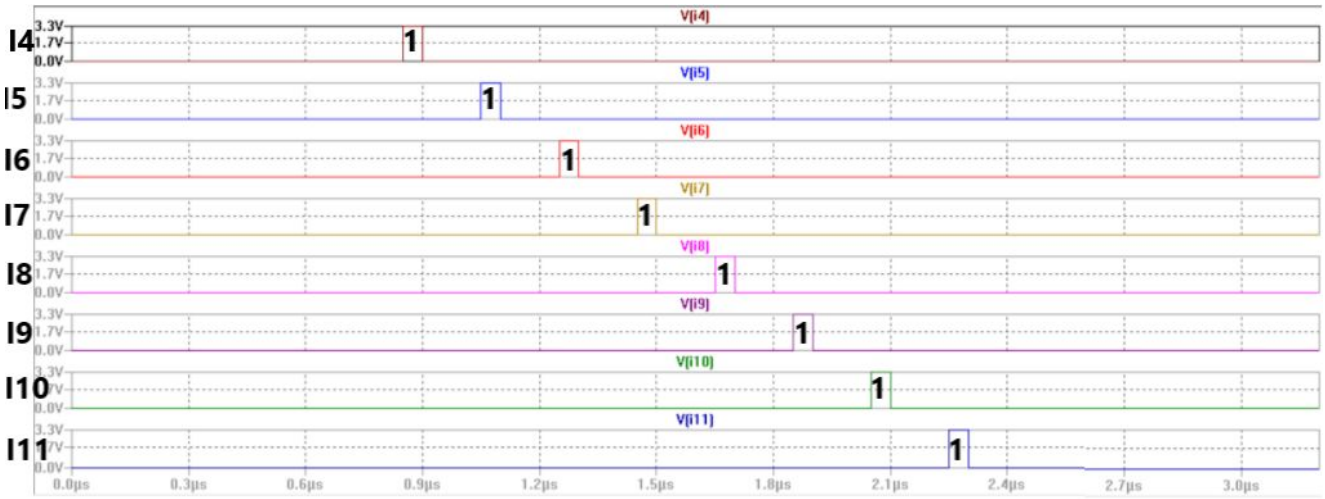

Figure 45: *16:1 Multiplexer Electric Schematic LTspice Simulation ~ Static CMOS*

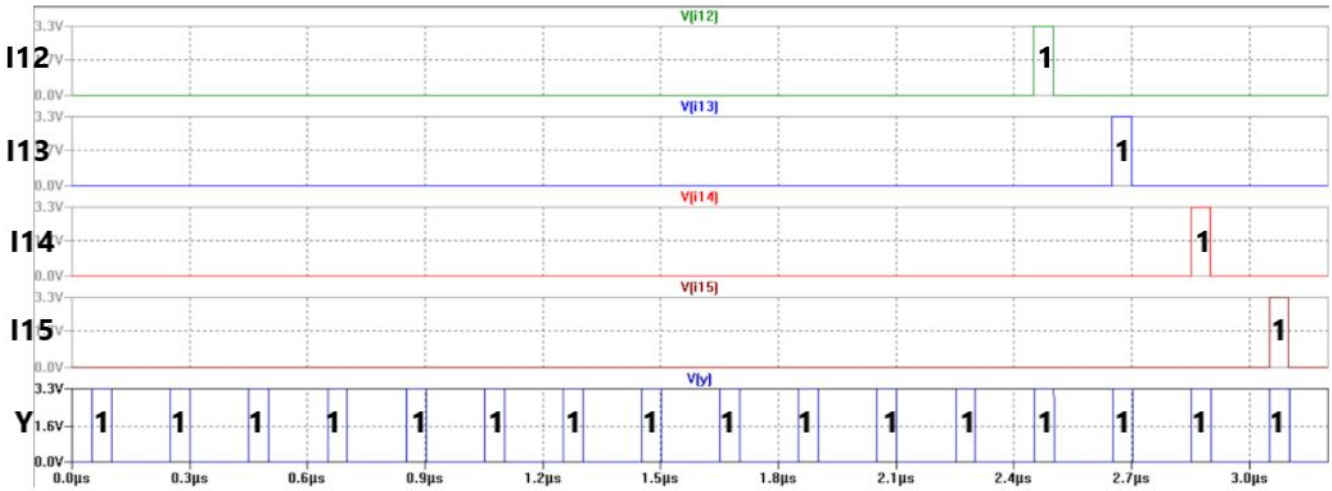

Figure 46: *16:1 Multiplexer Electric Schematic LTspice Simulation ~ Static CMOS*

```
** Extracted Parasitic Capacitors ***
C0 S1 0 39.686fF
C1 net@49 0 7.293fF
C2 net@24 0 8.176fF
C3 net@1 0 7.95fF
C4 net@0 0 7.267fF
C5 net@13 0 7.225fF
C6 S0 0 49.013fF
C7 net@335 0 7.239fF
C8 net@6 0 7.158fF
C9 net@387 0 7.058fF
C10 net@378 0 7.124fF
C11 net@15 0 7.127fF
C12 S0#0contact@102_metal-1-p-act 0 7.254fF
C13 Clk 0 17.862fF
C14 S2 0 16.659fF
C15 S2#5contact@115_metal-1-metal-2 0 5.824fF
C16 I0 0 0.981fF
C17 I1 0 0.946fF
C18 I2 0 0.946fF
C19 I3 0 0.946fF
C20 I4 0 0.917fF
C21 I5 0 0.917fF
C22 I6 0 0.917fF
C23 I7 0 0.946fF
C24 net@225 0 17.909fF
C25 net@229 0 8.291fF
```

```
** Extracted Parasitic Resistors ***
R0 Clk#0pmos@1_poly-right Clk#0pmos@1_poly-right##0 6.2
R1 Clk#0pmos@1_poly-right##0 Clk#1pin@0_polysilicon-1 6.2
R2 Clk#1pin@0_polysilicon-1 Clk#1pin@0_polysilicon-1##0 9.723
C227 Clk#1pin@0_polysilicon-1##0 0 0.104fF
R3 Clk#1pin@0_polysilicon-1##0 Clk#1pin@0_polysilicon-1##1 9.723
C228 Clk#1pin@0_polysilicon-1##1 0 0.104fF
R4 Clk#1pin@0_polysilicon-1##1 Clk#1pin@0_polysilicon-1##2 9.723
C229 Clk#1pin@0_polysilicon-1##2 0 0.104fF
R5 Clk#1pin@0_polysilicon-1##2 Clk#1pin@0_polysilicon-1##3 9.723
C230 Clk#1pin@0_polysilicon-1##3 0 0.104fF
R6 Clk#1pin@0_polysilicon-1##3 Clk#1pin@0_polysilicon-1##4 9.723
C231 Clk#1pin@0_polysilicon-1##4 0 0.104fF
R7 Clk#1pin@0_polysilicon-1##4 Clk#1pin@0_polysilicon-1##5 9.723
C232 Clk#1pin@0_polysilicon-1##5 0 0.104fF
R8 Clk#1pin@0_polysilicon-1##5 Clk#1pin@0_polysilicon-1##6 9.723
C233 Clk#1pin@0_polysilicon-1##6 0 0.104fF
R9 Clk#1pin@0_polysilicon-1##6 Clk#1pin@0_polysilicon-1##7 9.723
C234 Clk#1pin@0_polysilicon-1##7 0 0.104fF
R10 Clk#1pin@0_polysilicon-1##7 Clk#1pin@0_polysilicon-1##8 9.723
C235 Clk#1pin@0_polysilicon-1##8 0 0.104fF
R11 Clk#1pin@0_polysilicon-1##8 Clk#1pin@0_polysilicon-1##9 9.723
C236 Clk#1pin@0_polysilicon-1##9 0 0.104fF
R12 Clk#1pin@0_polysilicon-1##9 Clk#2pin@1_polysilicon-1 9.723
R13 Clk#2pin@1_polysilicon-1 Clk#2pin@1_polysilicon-1##0 5.425
R14 Clk#2pin@1_polysilicon-1##0 Clk#3pmos@3_poly-right 5.425
R15 Clk#2pin@1_polysilicon-1 Clk#2pin@1_polysilicon-1##0 9.582
```

Figure 47: *16:1 Multiplexer LTspice Parasitic Extraction Excerpts for Capacitance & Resistance and Capacitance Per um^2 ~ Static CMOS Layout*

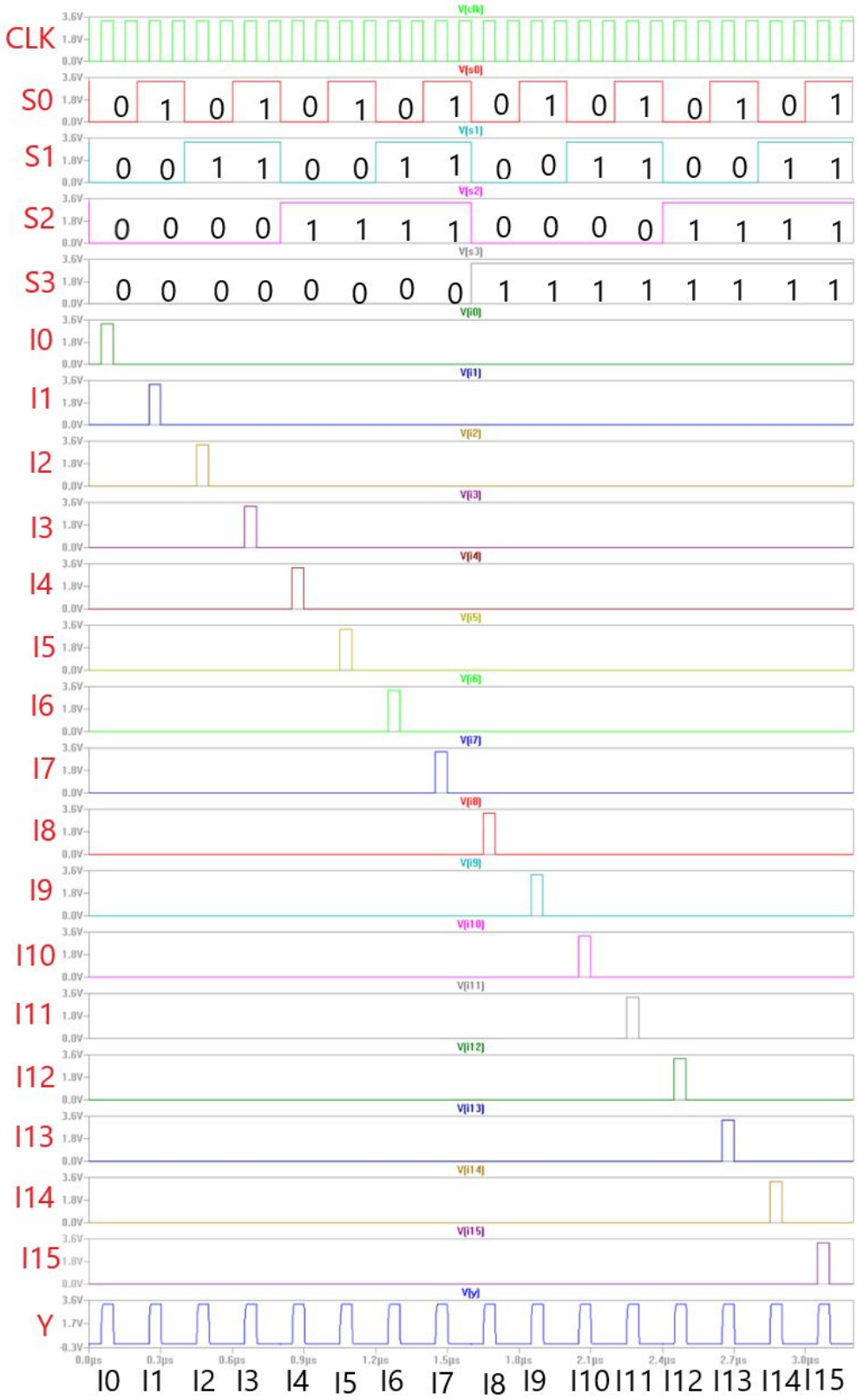

Figure 48: *16:1 Multiplexer Electric Schematic LTspice Simulation ~ Dynamic CMOS*

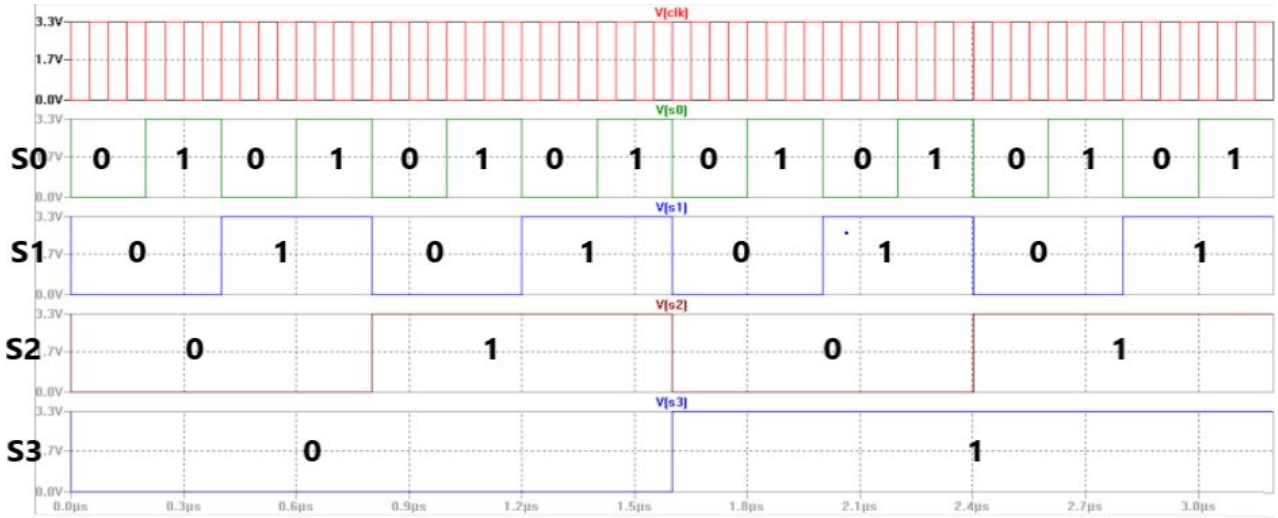

Figure 49: *16:1 Multiplexer Electric Layout LTspice Simulation ~ Dynamic CMOS*

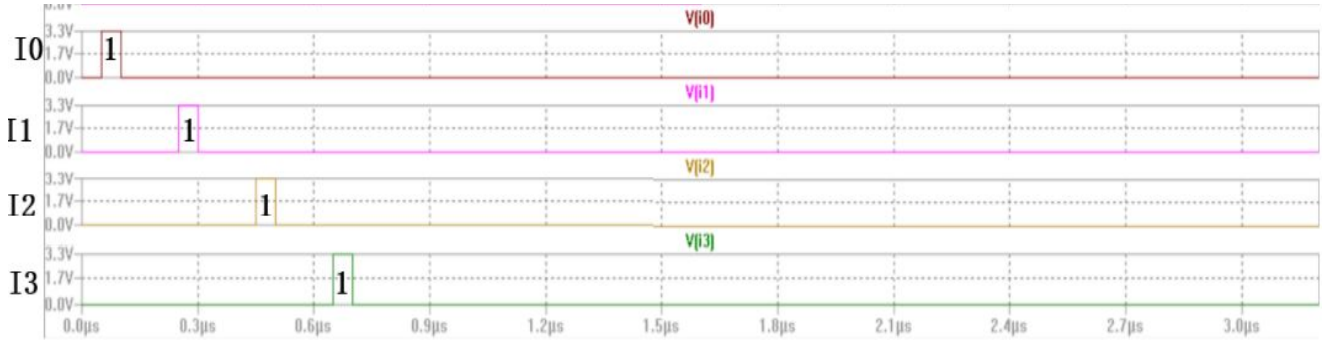

Figure 50: *16:1 Multiplexer Electric Layout LTspice Simulation ~ Dynamic CMOS*

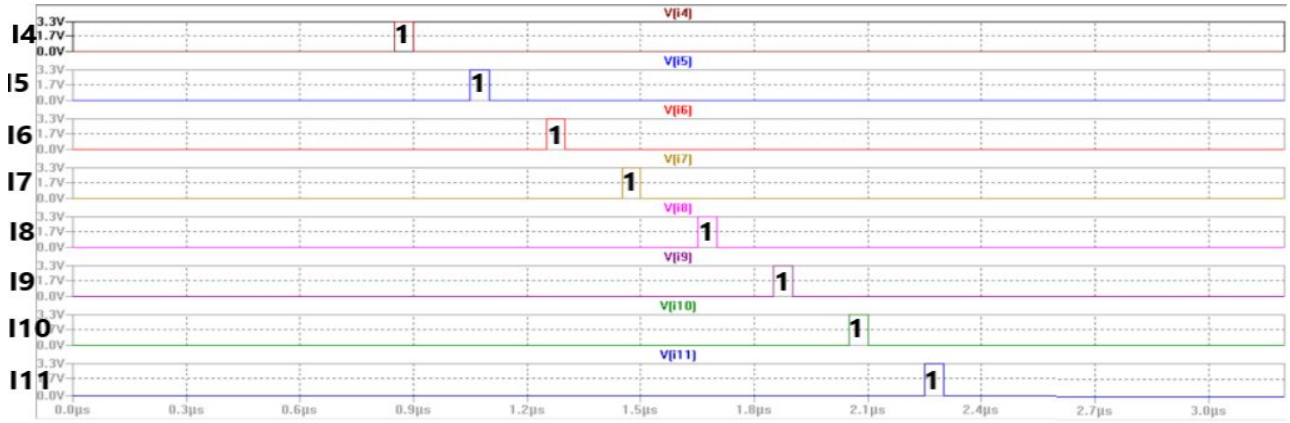

Figure 51: *16:1 Multiplexer Electric Layout LTspice Simulation ~ Dynamic CMOS*

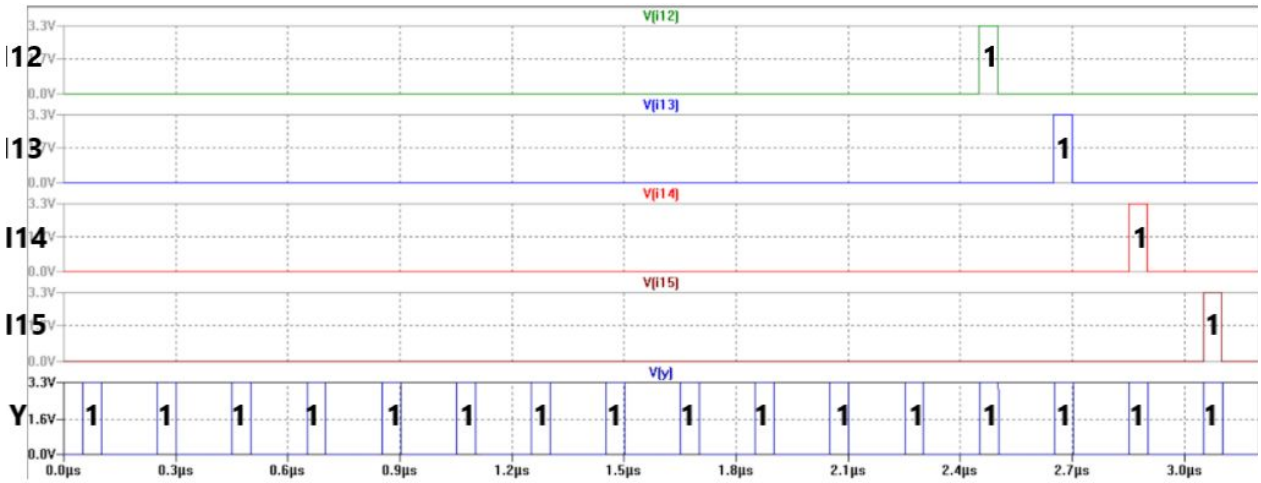

Figure 52: *16:1 Multiplexer Electric Layout LTspice Simulation ~ Dynamic CMOS*

```
Mpmos@48 Y net@1150#7pmos@48_poly-left net@109
** Extracted Parasitic Capacitors ***
C0 S1 0 39.686fF
C1 net@49 0 7.293fF
C2 net@24 0 8.176fF
C3 net@1 0 7.95fF
C4 net@0 0 7.267fF
C5 net@13 0 7.225fF
C6 S0 0 49.013fF
C7 net@335 0 7.239fF
C8 net@6 0 7.158fF
C9 net@387 0 7.058fF
C10 net@378 0 7.124fF
C11 net@15 0 7.127fF
C12 S0#0contact@102_metal-1-p-act 0 7.254fF
C13 Clk 0 17.862fF
C14 S2 0 16.659fF
C15 S2#5contact@115_metal-1-metal-2 0 5.824fF
C16 I0 0 0.981fF
C17 I1 0 0.946fF
C18 I2 0 0.946fF
C19 I3 0 0.946fF
C20 I4 0 0.917fF
C21 I5 0 0.917fF
C22 I6 0 0.917fF
```

```
C226 net@1115#9pmos@46_poly-left 0 0.104fF
** Extracted Parasitic Resistors ***
R0 Clk#0pmos@1_poly-right Clk#0pmos@1_poly-right##0 6.2
R1 Clk#0pmos@1_poly-right##0 Clk#1pin@0_polysilicon-1 6.2
R2 Clk#1pin@0_polysilicon-1 Clk#1pin@0_polysilicon-1##0 9.723
C227 Clk#1pin@0_polysilicon-1##0 0 0.104fF
R3 Clk#1pin@0_polysilicon-1##0 Clk#1pin@0_polysilicon-1##1 9.723
C228 Clk#1pin@0_polysilicon-1##1 0 0.104fF
R4 Clk#1pin@0_polysilicon-1##1 Clk#1pin@0_polysilicon-1##2 9.723
C229 Clk#1pin@0_polysilicon-1##2 0 0.104fF
R5 Clk#1pin@0_polysilicon-1##2 Clk#1pin@0_polysilicon-1##3 9.723
C230 Clk#1pin@0_polysilicon-1##3 0 0.104fF
R6 Clk#1pin@0_polysilicon-1##3 Clk#1pin@0_polysilicon-1##4 9.723
C231 Clk#1pin@0_polysilicon-1##4 0 0.104fF
R7 Clk#1pin@0_polysilicon-1##4 Clk#1pin@0_polysilicon-1##5 9.723
C232 Clk#1pin@0_polysilicon-1##5 0 0.104fF
R8 Clk#1pin@0_polysilicon-1##5 Clk#1pin@0_polysilicon-1##6 9.723
C233 Clk#1pin@0_polysilicon-1##6 0 0.104fF
R9 Clk#1pin@0_polysilicon-1##6 Clk#1pin@0_polysilicon-1##7 9.723
C234 Clk#1pin@0_polysilicon-1##7 0 0.104fF
R10 Clk#1pin@0_polysilicon-1##7 Clk#1pin@0_polysilicon-1##8 9.723
C235 Clk#1pin@0_polysilicon-1##8 0 0.104fF
R11 Clk#1pin@0_polysilicon-1##8 Clk#1pin@0_polysilicon-1##9 9.723
C236 Clk#1pin@0_polysilicon-1##9 0 0.104fF
R12 Clk#1pin@0_polysilicon-1##9 Clk#2pin@1_polysilicon-1 9.723
R13 Clk#2pin@1_polysilicon-1 Clk#2pin@1_polysilicon-1##0 5.425
```

Figure 53: *16:1 Multiplexer LTspice Parasitic Extraction Excerpts for Capacitance & Resistance and Capacitance Per um^2 ~ Dynamic CMOS Layout*

6. IRSIM Logic Simulations and Measurements for Layout and Schematic

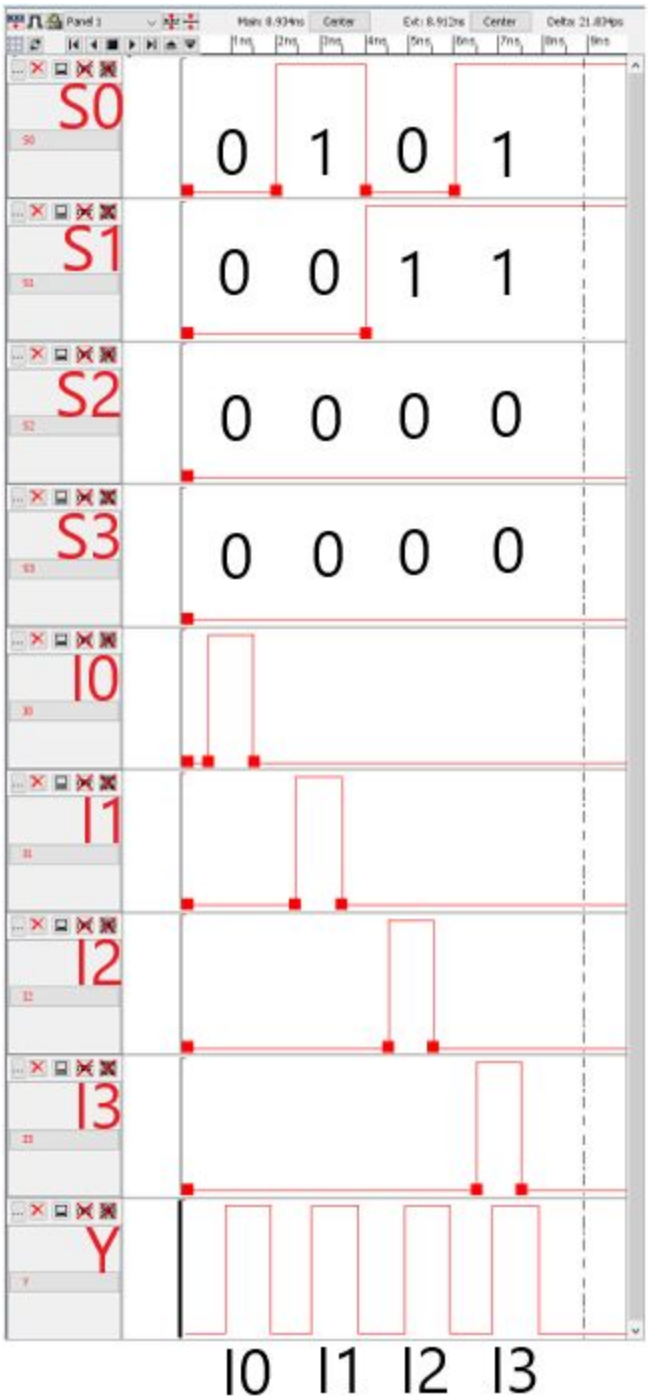

Figure 54: *16:1 Multiplexer Schematic IRSIM Simulation (I0 - 13) ~ Transmission Gate*

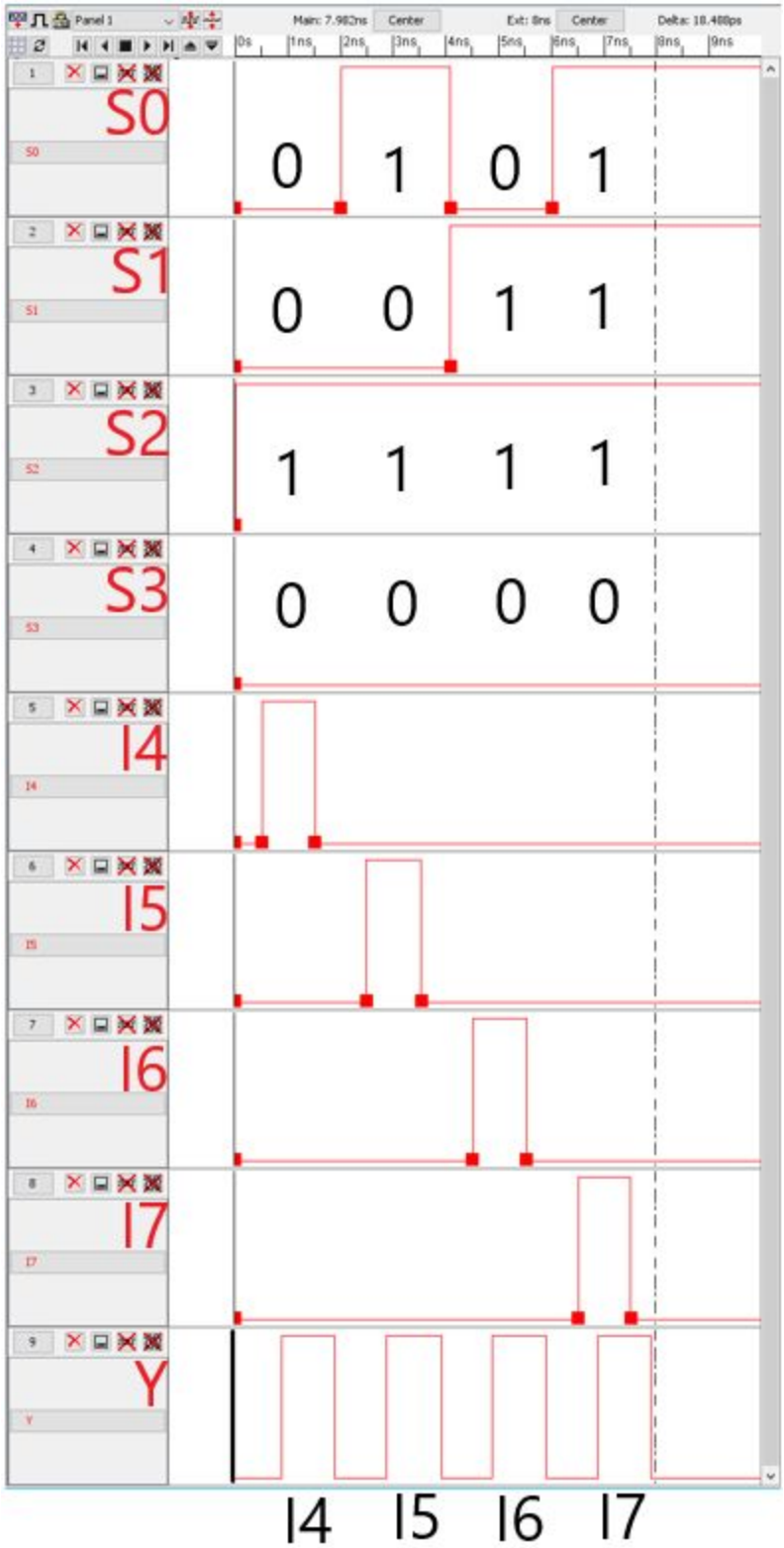

Figure 55: *16:1 Multiplexer Schematic IRSIM Simulation (I4 - 17) ~ Transmission Gate*

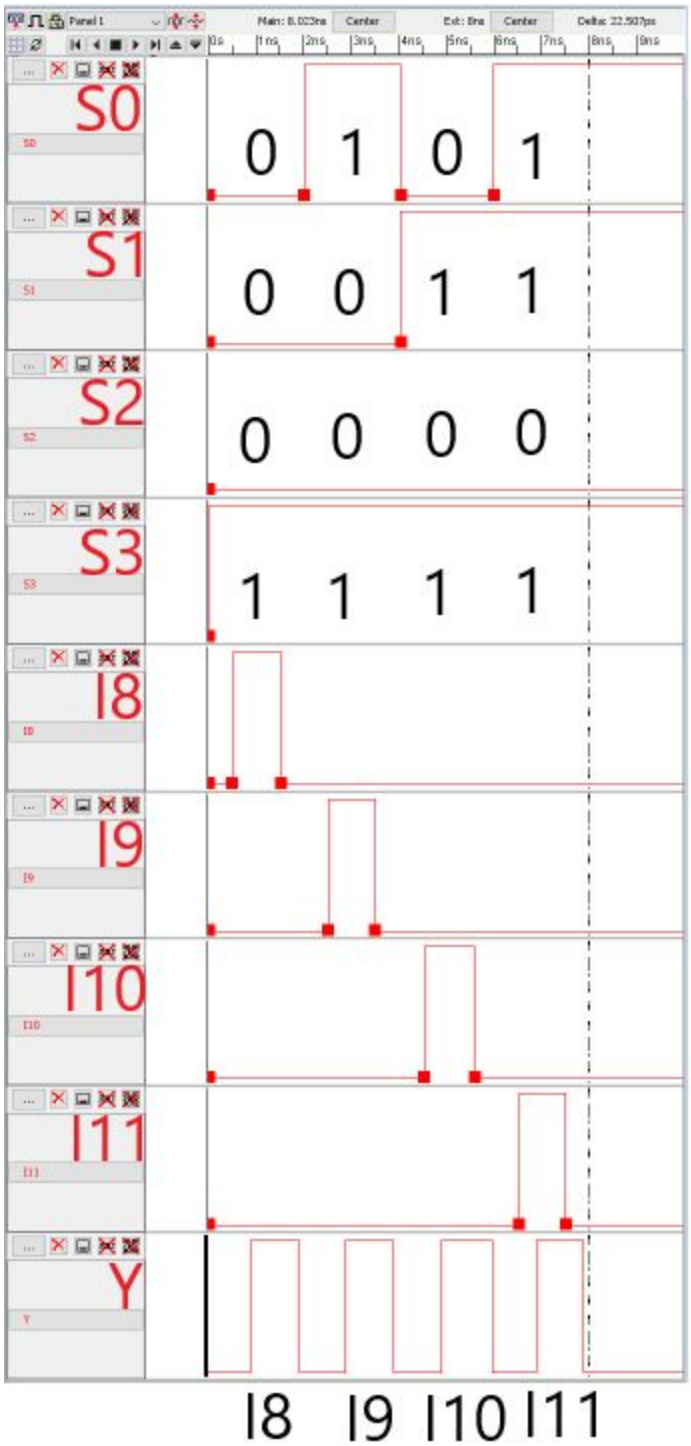

Figure 56: *16:1 Multiplexer Schematic IRSIM Simulation (I8 - 111) ~ Transmission Gate*

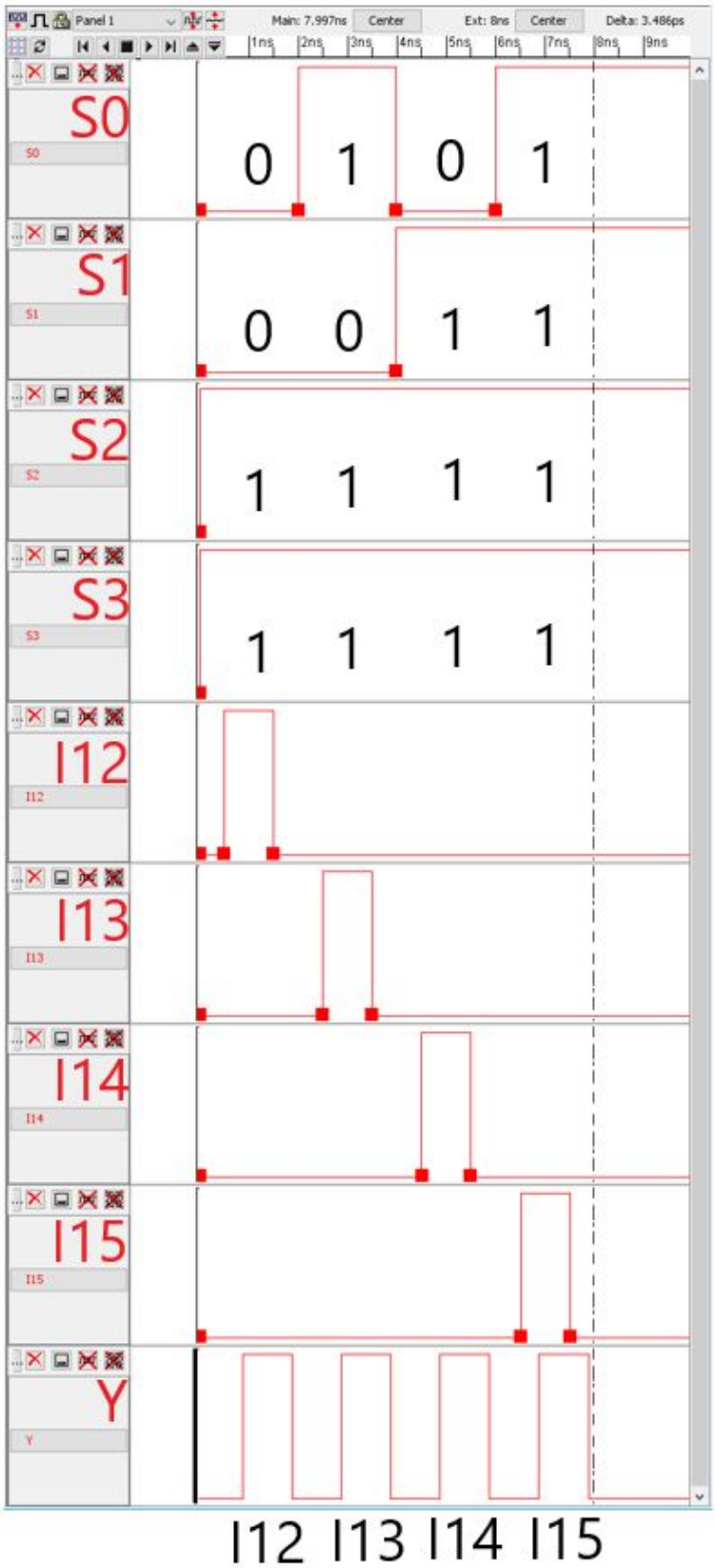

Figure 57: *16:1 Multiplexer Schematic IRSIM Simulation (I12 - 115) ~ Transmission Gate*

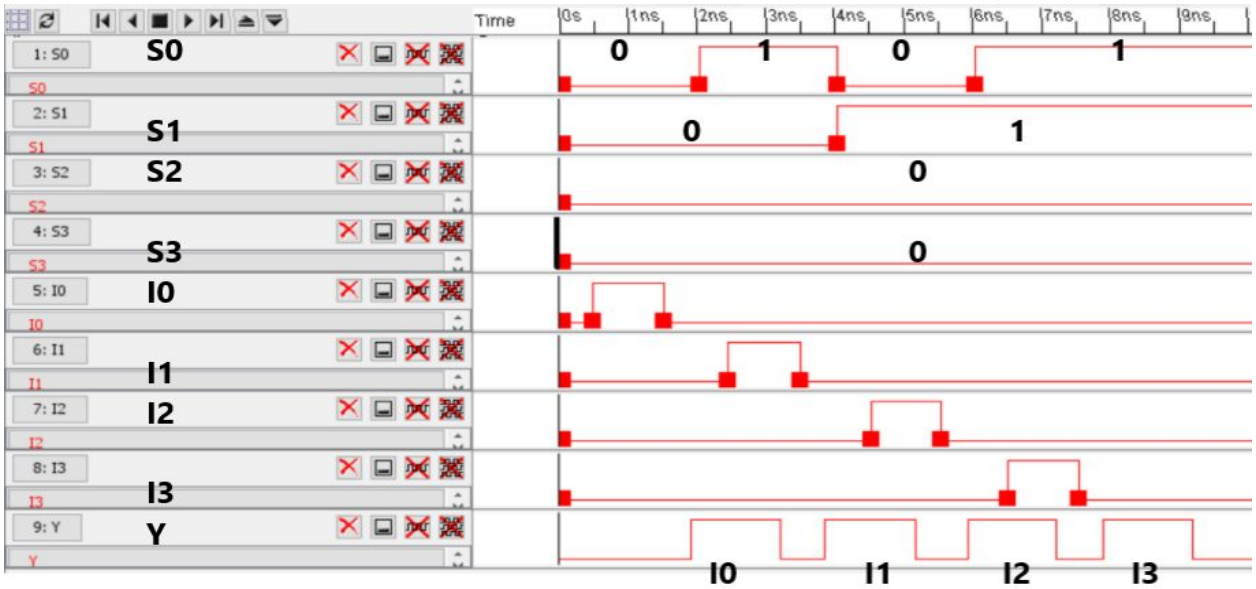

Figure 58: *16:1 Multiplexer Schematic IRSIM Simulation (I0 - 13) ~ Static CMOS*

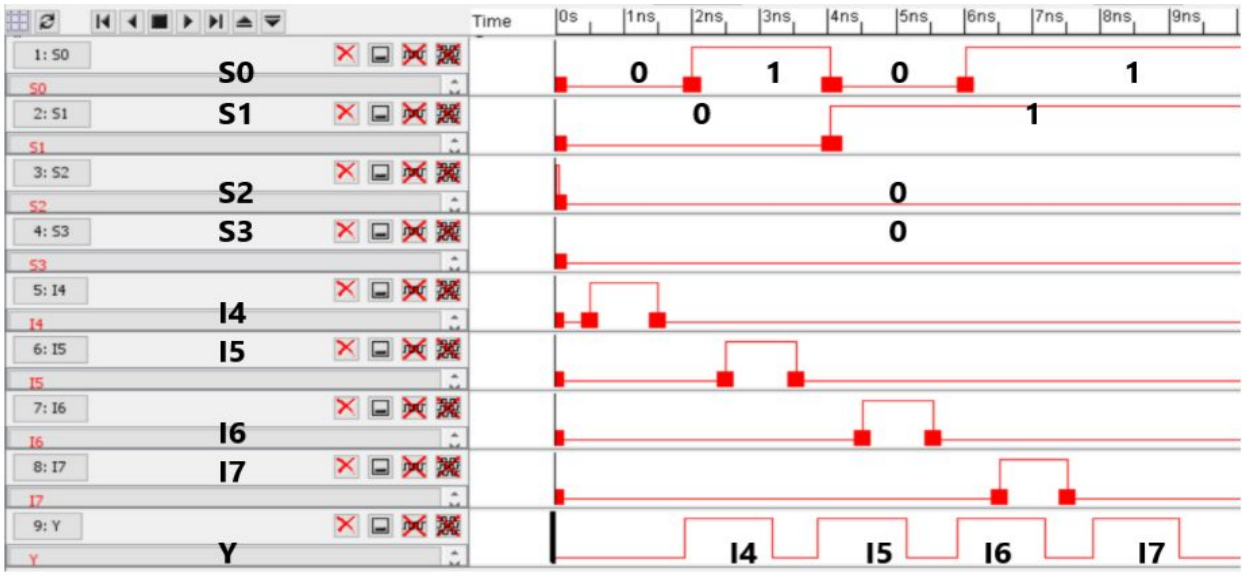

Figure 59: *16:1 Multiplexer Schematic IRSIM Simulation (I4 - 17) ~ Static CMOS*

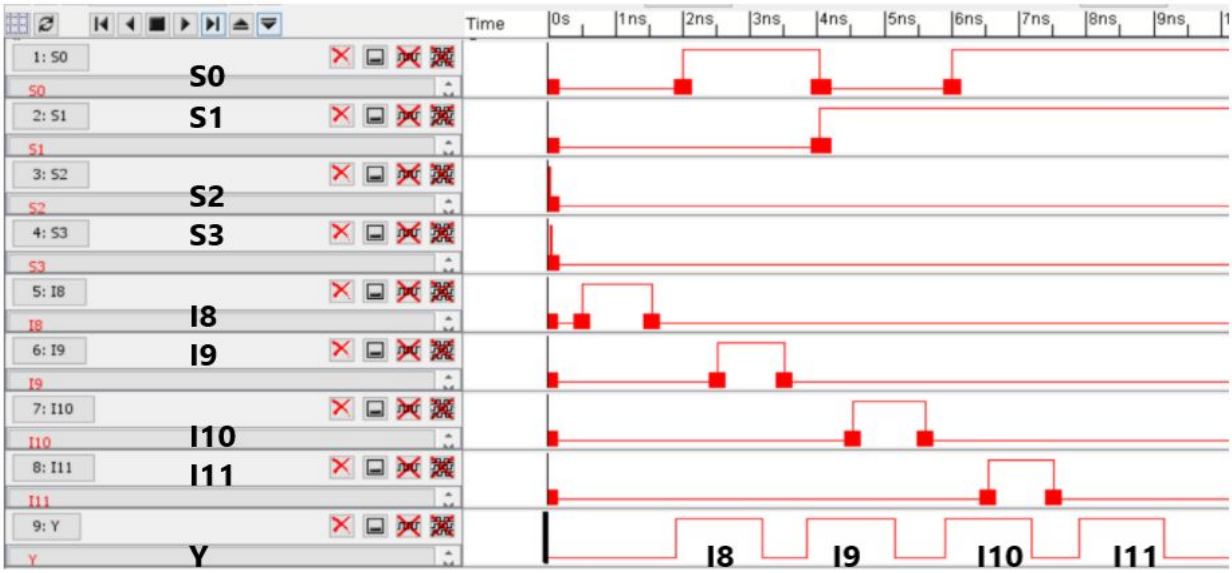

Figure 60: *16:1 Multiplexer Schematic IRSIM Simulation (I8 - 111) ~ Static CMOS*

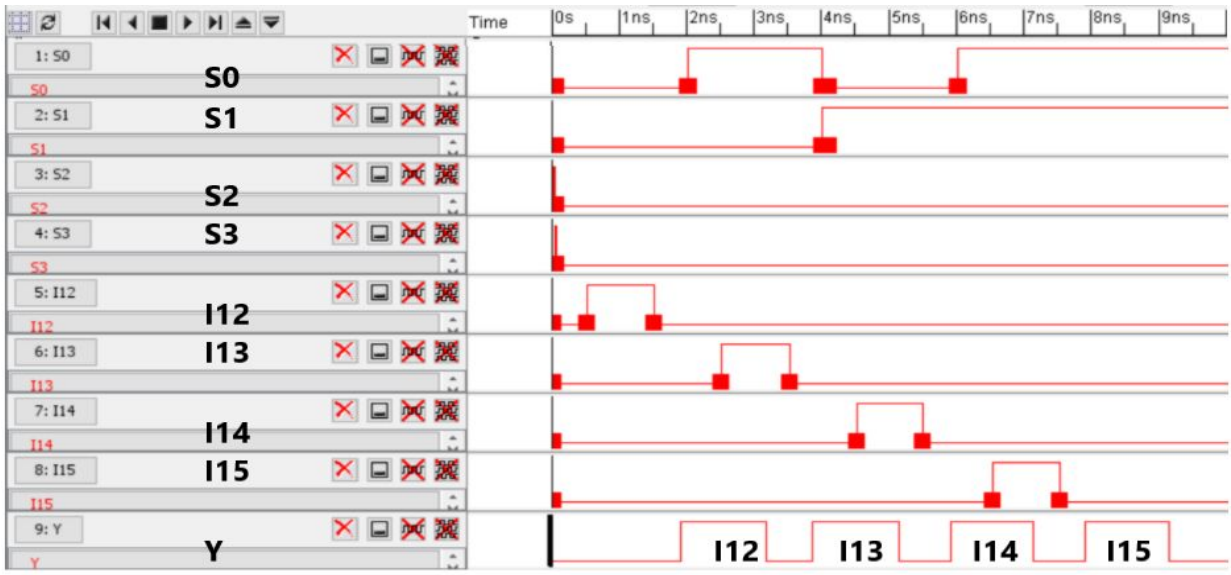

Figure 61: *16:1 Multiplexer Schematic IRSIM Simulation (I12 - 115) ~ Static CMOS*

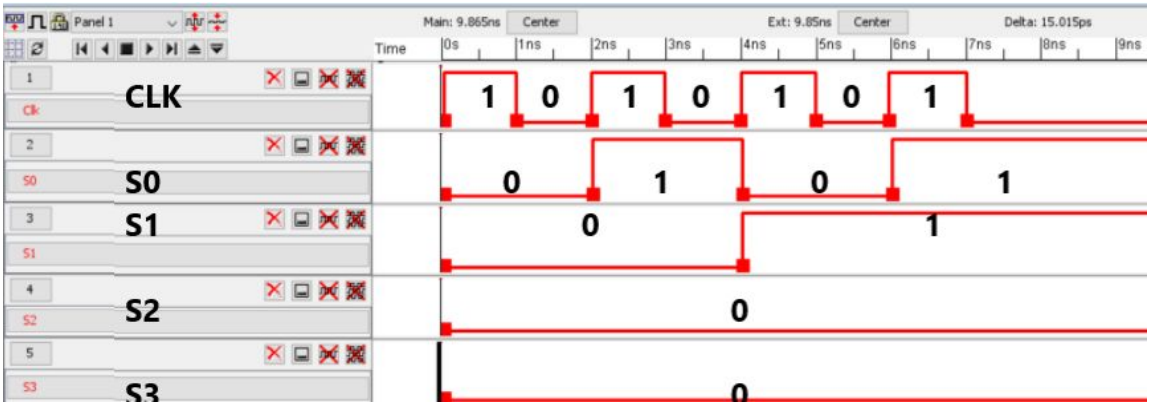

Figure 62: *16:1 Multiplexer Layout IRSIM Simulation (Clk - S3) ~ Dynamic CMOS*

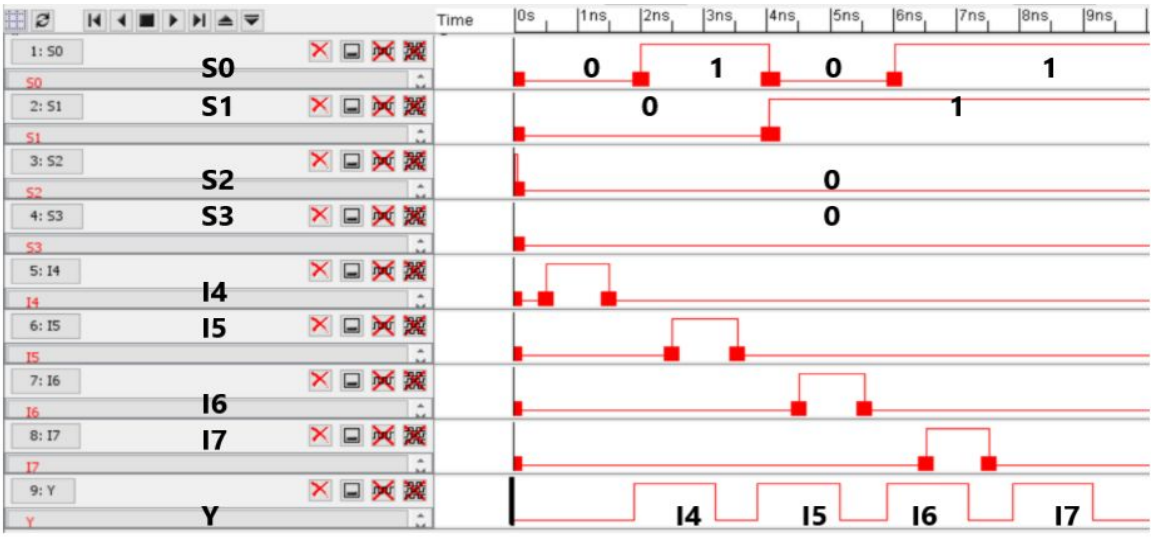

Figure 63: *16:1 Multiplexer Layout IRSIM Simulation (I4 - 17) ~ Dynamic CMOS*

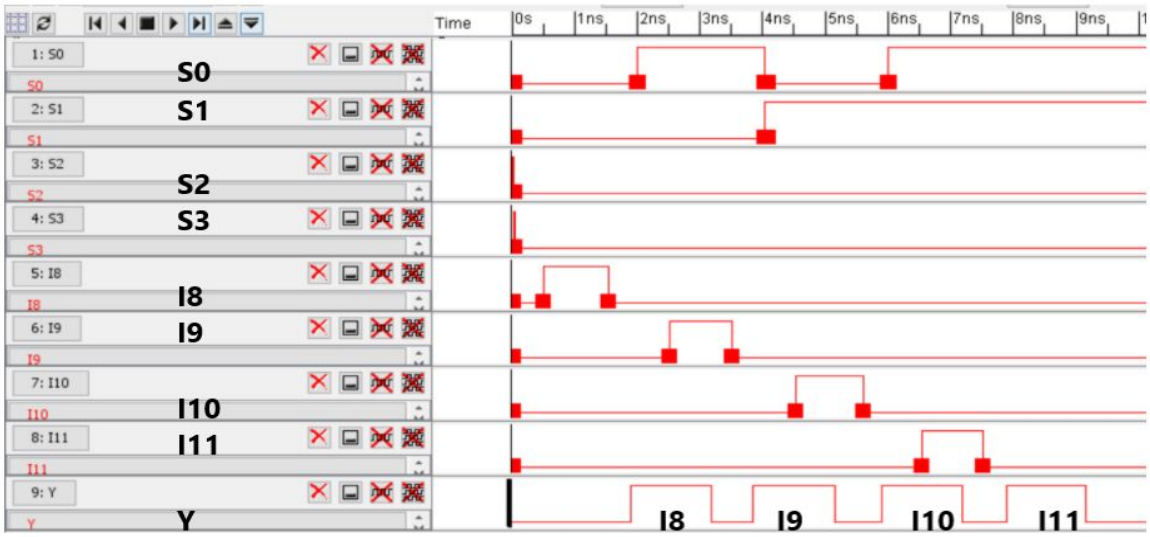

Figure 64: *16:1 Multiplexer Layout IRSIM Simulation (I8 - 111) ~ Dynamic CMOS*

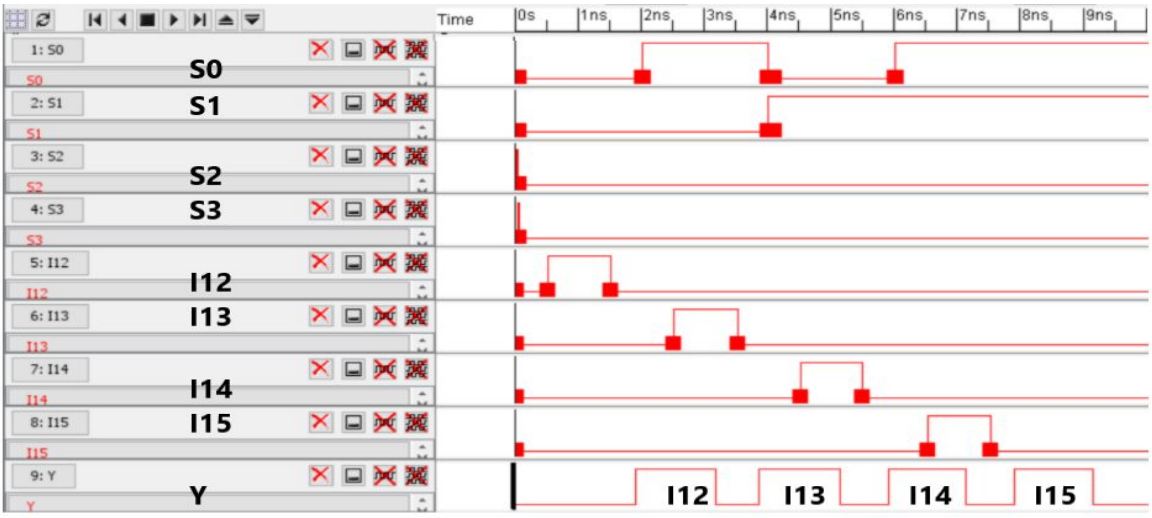

Figure 65: *16:1 Multiplexer Layout IRSIM Simulation (I12 - 115) ~ Dynamic CMOS*

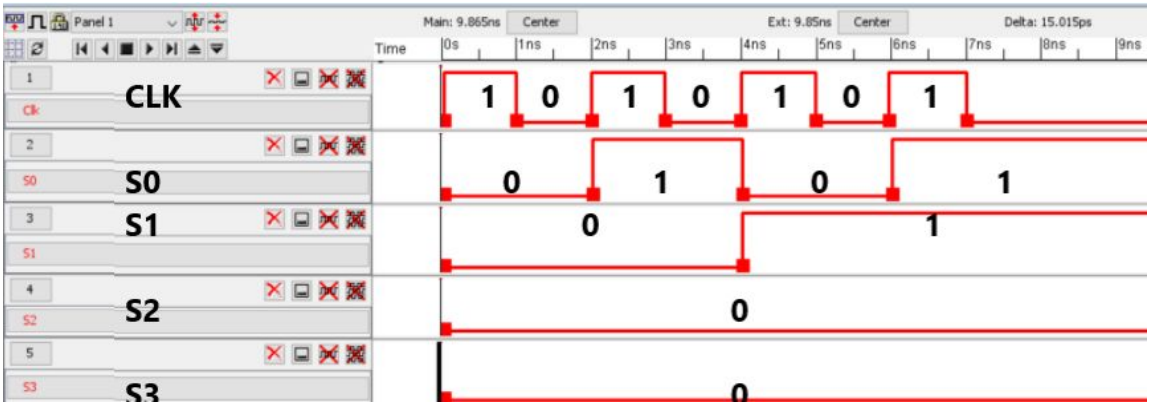

Figure 66: *16:1 Multiplexer Schematic IRSIM Simulation (Clk - S3) ~ Dynamic CMOS*

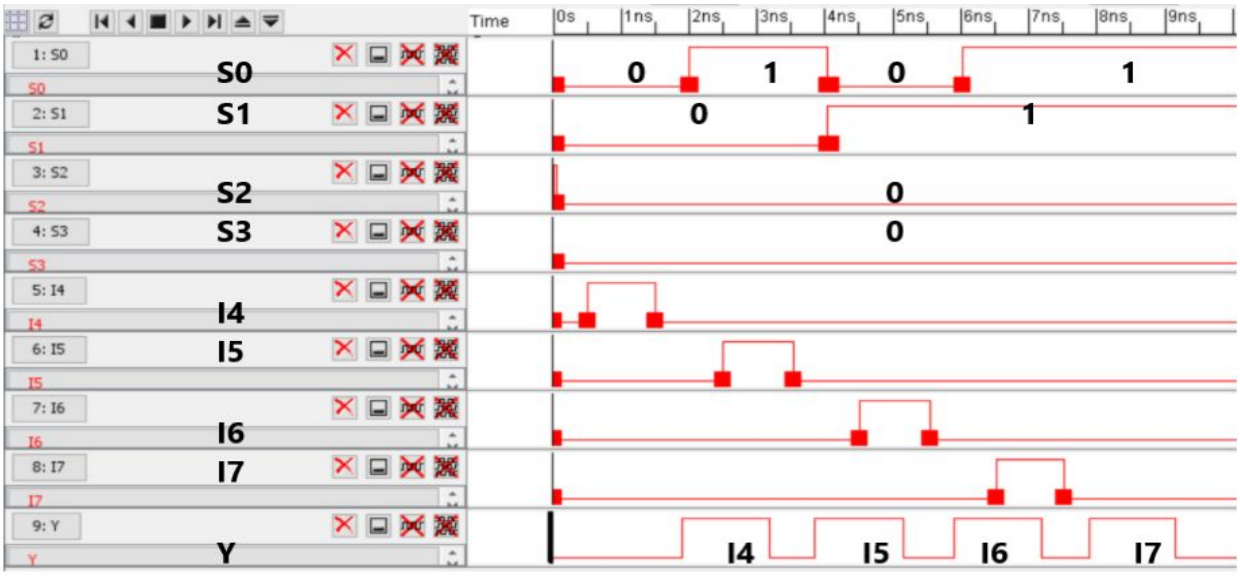

Figure 67: *16:1 Multiplexer Schematic IRSIM Simulation (I4 - 17) ~ Dynamic CMOS*

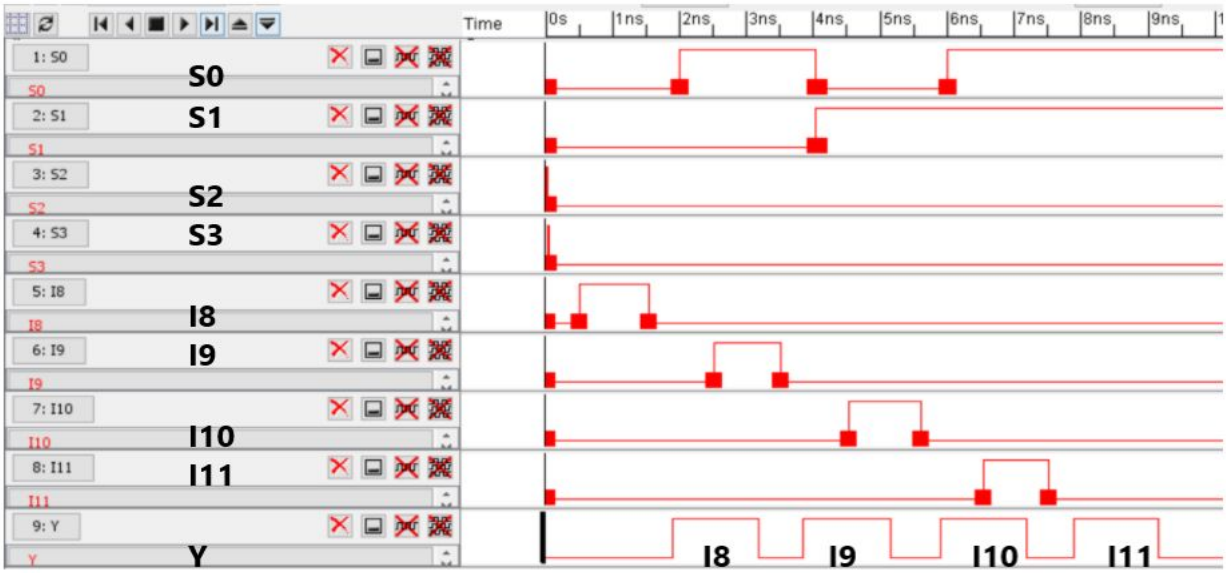

Figure 68: *16:1 Multiplexer Schematic IRSIM Simulation (I8 - 111) ~ Dynamic CMOS*

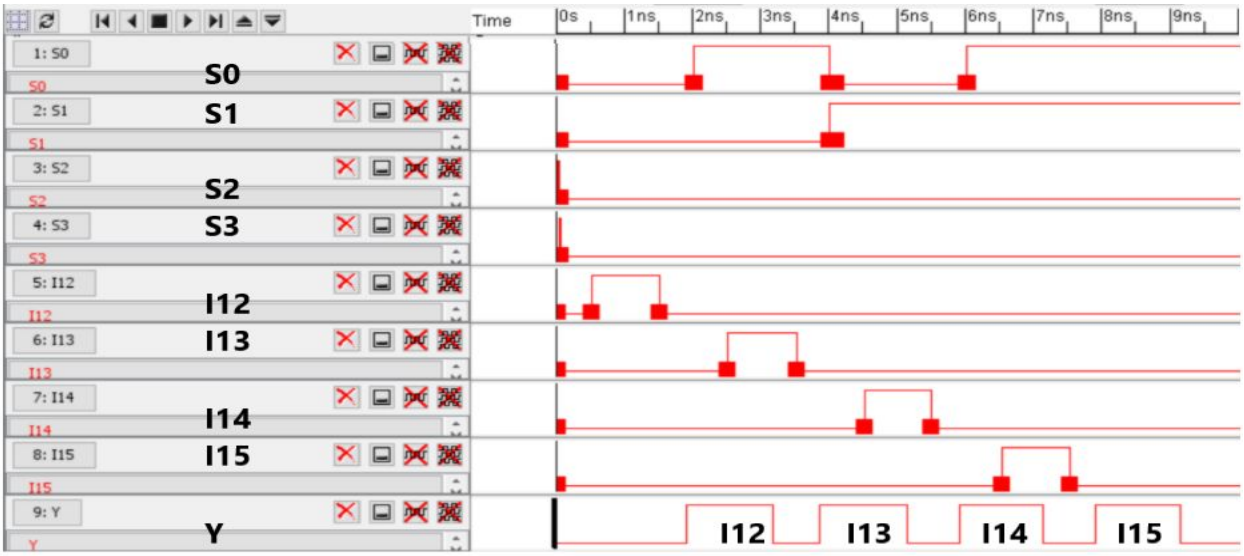

Figure 69: *16:1 Multiplexer Schematic IRSIM Simulation (I12 - 115) ~ Dynamic CMOS*

16:1 Multiplexer IRSIM Response Delay

	Schematic	*Layout*
Static CMOS	.5ns	.7ns
Transmission Gate	.1ns	.15ns
Dynamic CMOS	1ns	1.4ns

7. Measurements in LTSPICE for delays for Layout and Schematic

$$t_p = (t_{pHL} + t_{pLH})/2$$

Figure 70: *Propagation Delay Formula*

```
.measure tpdr_out v(Y) val=0 rise=1 td=0 targ v(Y) val=3.3 rise=1
.measure tpdf_out v(Y) val=3.3 fall=1 td=0 targ v(Y) val=0 fall=1
.measure tpdr_in_out trig v(S0) val='3.3/2' rise=1 td=0 targ v(Y) val='3.3/2' rise=1
.measure tpdf_in_out trig v(S0) val='3.3/2' fall=1 td=0 targ v(Y) val='3.3/2' fall=1
.measure tpd param='(-tpdr_in_out+tpdf_in_out)/2' goal=0
.measure diff param='tpdf_in_out-tpdr_in_out' goal=0
```

Figure 71: *16:1 Multiplexer Measurement SPICE Deck*

SPICE Error Log: C:\Electric\mux_16_1_tg.log

```
tpdr_out=5.22334e-008 FROM 0 TO 5.22334e-008
tpdf_out=6.72745e-018 FROM 0 TO 6.72745e-018
tpdr_in_out=-1.49989e-007 FROM 2.0015e-007 TO 5.01607e-008
tpdf_in_out=1.00125e-007 FROM 5e-011 TO 1.00175e-007
tpd: ((-tpdr_in_out+tpdf_in_out)/2)=1.25057e-007
diff: (tpdf_in_out-tpdr_in_out)=2.50115e-007
```

Figure 72: *16:1 Multiplexer LTspice Measurement Simulation (Rise, Fall, Propagation Delay) ~ Transmission Gate Schematic*

SPICE Error Log: C:\Electric\mux_16_1_tg.log

```
tpdr_out=9.84588e-008 FROM 0 TO 9.84588e-008
tpdf_out=3.85921e-014 FROM 0 TO 3.85921e-014
tpdr_in_out=-1.48377e-007 FROM 2.0015e-007 TO 5.17725e-008
tpdf_in_out=1.01571e-007 FROM 5e-011 TO 1.01621e-007
tpd: ((-tpdr_in_out+tpdf_in_out)/2)=1.24974e-007
diff: (tpdf_in_out-tpdr_in_out)=2.49949e-007
```

Figure 73: *16:1 Multiplexer LTspice Measurement Simulation (Rise, Fall, Propagation Delay) ~ Transmission Gate Layout*

SPICE Error Log: C:\Electric\16-to-1-Mux.log

```
tpdr_out=5.19186e-008 FROM 0 TO 5.19186e-008
tpdf_out=5.46361e-017 FROM 0 TO 5.46361e-017
tpdr_in_out=-1.49145e-007 FROM 2.0015e-007 TO 5.10047e-008
tpdf_in_out=1.01191e-007 FROM 5e-011 TO 1.01241e-007
tpd: ((-tpdr_in_out+tpdf_in_out)/2)=1.25168e-007
diff: (tpdf_in_out-tpdr_in_out)=2.50336e-007
```

Figure 74: *16:1 Multiplexer LTspice Measurement Simulation (Rise, Fall, Propagation Delay) ~ Static CMOS Schematic*

SPICE Error Log: C:\Electric\16-to-1-Mux.log

```
tpdr_out=1.00611e-007 FROM 0 TO 1.00611e-007
tpdf_out=3.83566e-017 FROM 0 TO 3.83566e-017
tpdr_in_out=-1.49314e-007 FROM 2.0015e-007 TO 5.08361e-008
tpdf_in_out=1.01304e-007 FROM 5e-011 TO 1.01354e-007
tpd: ((-tpdr_in_out+tpdf_in_out)/2)=1.25309e-007
diff: (tpdf_in_out-tpdr_in_out)=2.50618e-007
```

Figure 75: *16:1 Multiplexer LTspice Measurement Simulation (Rise, Fall, Propagation Delay) ~ Static CMOS Schematic*

SPICE Error Log: C:\Electric\mux_16_1.log

```
tpdr_out=5.1394e-008 FROM 0 TO 5.1394e-008
tpdf_out=8.36726e-018 FROM 0 TO 8.36726e-018
tpdr_in_out=-1.4961e-007 FROM 2.0015e-007 TO 5.05403e-008
tpdf_in_out=1.0094e-007 FROM 5e-011 TO 1.0099e-007
tpd: ((-tpdr_in_out+tpdf_in_out)/2)=1.25275e-007
diff: (tpdf_in_out-tpdr_in_out)=2.50549e-007
```

Figure 76: *16:1 Multiplexer LTspice Measurement Simulation (Rise, Fall, Propagation Delay) ~ Dynamic CMOS Schematic*

SPICE Error Log: C:\Electric\mux_16_1.log

```
tpdr_out=1.02395e-007 FROM 0 TO 1.02395e-007
tpdf_out=4.69373e-013 FROM 0 TO 4.69373e-013
tpdr_in_out=-1.48038e-007 FROM 2.0015e-007 TO 5.21119e-008
tpdf_in_out=1.03632e-007 FROM 5e-011 TO 1.03682e-007
tpd: ((-tpdr_in_out+tpdf_in_out)/2)=1.25835e-007
diff: (tpdf_in_out-tpdr_in_out)=2.5167e-007
```

Figure 77: *16:1 Multiplexer LTspice Measurement Simulation (Rise, Fall, Propagation Delay) ~ Dynamic CMOS Layout*

8. Measurements of power, delay, chip area, timing, number of transistors for the layout

16:1 Multiplexer Transistor Count

Transmission Gate	68
Static CMOS	350
Dynamic CMOS	151

16:1 Multiplexer Propogation Delay

	tpdr_out	*tpdf_out*	*tpdr_in_out*	*tpdf_in_out*	*tpd*	*diff*
Static CMOS (Shematic)	5.19E-08	5.46E-17	1.49E-07	1.01E-07	1.25E-07	2.50E-07
Transmission Gate (Shematic)	5.22E-08	6.73E-18	1.50E-07	1.00E-07	1.25E-07	2.50E-07
Dynamic CMOS (Schematic)	5.14E-08	8.37E-18	1.50E-07	1.01E-07	1.25E-07	2.51E-07
Static CMOS (Layout)	1.01E-07	3.84E-17	1.49E-07	1.01E-07	1.25E-07	2.51E-07
Transmission Gate (Layout)	9.85E-08	3.86E-14	1.48E-07	1.02E-07	1.25E-07	2.50E-07
Dynamic CMOS (Layout)	1.02E-07	4.69E-13	1.48E-07	1.04E-07	1.26E-07	2.52E-07

$$P = I \times V$$

Figure 78: *Formula for Power Calculation*

16:1 Multiplexer Power Assessment

	Schematic	*Layout*
Static CMOS	5.1 mW	8.1 mW
Transmission Gate	2.4 mW	7.9 mW
Dynamic CMOS	3.8 mW	11.9 mW

Figure 79: *16:1 Multiplexer Power (Schematic) ~ Transmission Gate*

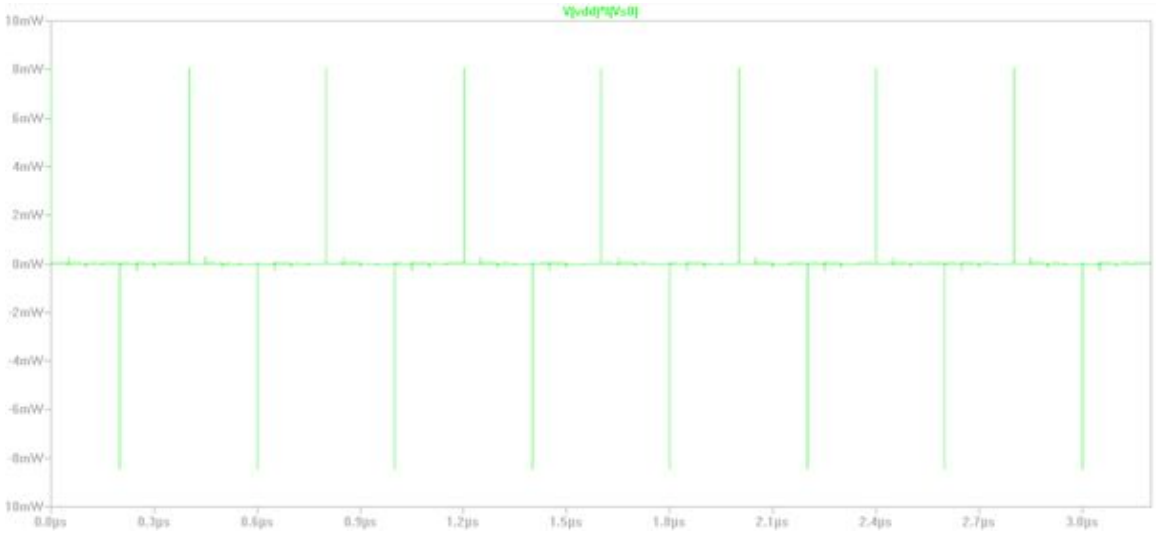

Figure 80: *16:1 Multiplexer Power (Layout) ~ Transmission Gate*

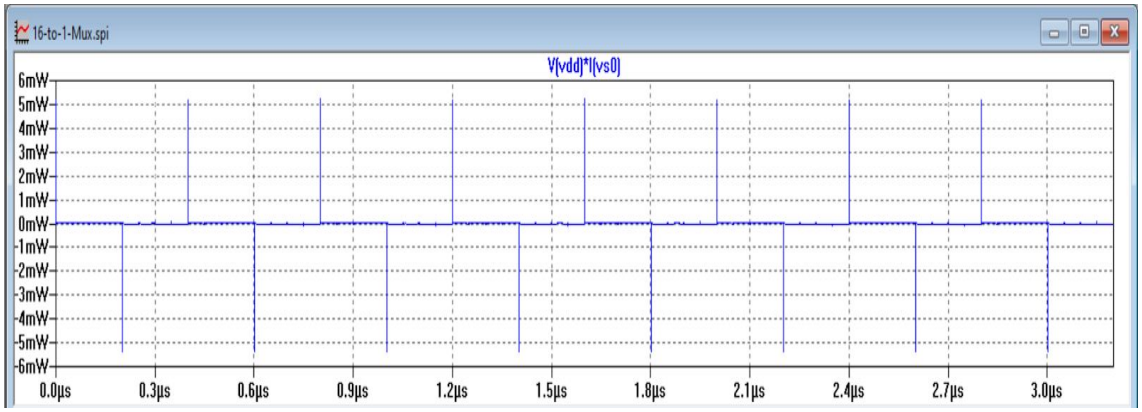

Figure 81: *16:1 Multiplexer Power (Schematic) ~ Static CMOS*

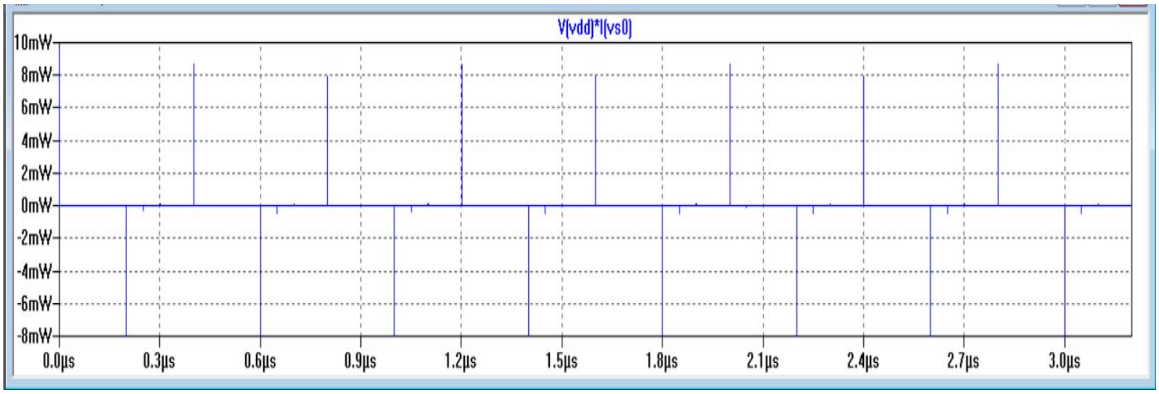

Figure 82: *16:1 Multiplexer Power (Layout) ~ Dynamic CMOS*

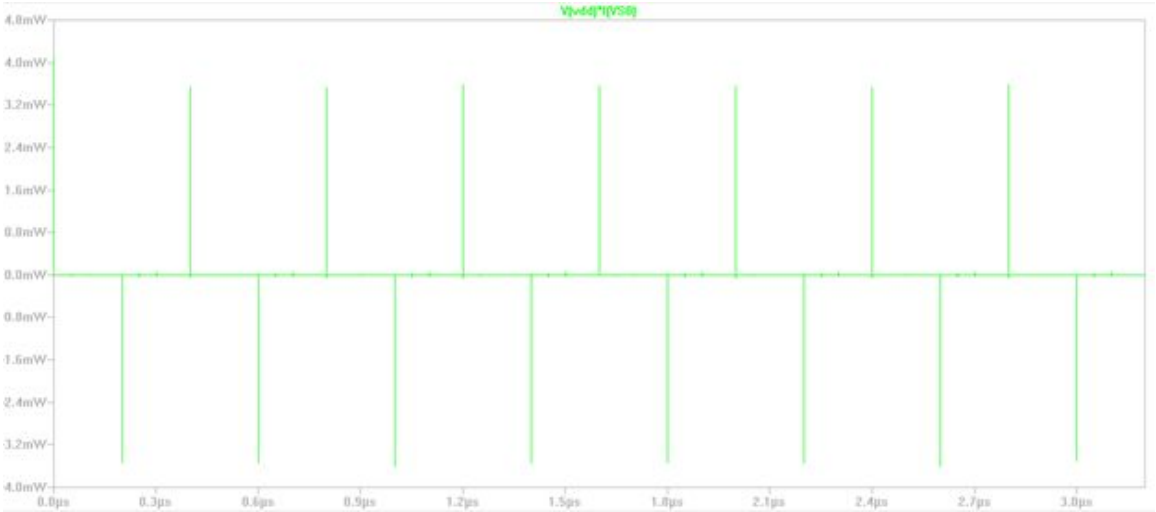

Figure 83: *16:1 Multiplexer Power (Schematic) ~ Dynamic CMOS*

Figure 84: *16:1 Multiplexer Power (Layout) ~ Dynamic CMOS*

$$Total\ Chip\ Area = W_{\lambda}\ \lambda \times L_{\lambda}\lambda$$

Figure 85: *Formula for Total Chip Area Calculation*

16:1 Multiplexer Total Chip Area

Static CMOS	1.71E-07
Transmission Gate	7.46E-09
Dynamic CMOS	1.341E-07

9. Conclusions

Ultimately, after having implemented and assessed the performance of our 16:1 multiplexers implemented using static/dynamic CMOS logic and transmission gate logic, it is very apparent that there are significant performance advantages in integrated circuit networks that implement transmission gates. The transmission gate design resulted in increased speed and a reduction in the number of components needed to implement the system. Subsequently, a reduction in chip area is also realized in the 16:1 multiplexer design implemented using transmission gates. The dynamic CMOS implementation results in increased power consumption with comparison to the static CMOS and transmission gate designs as indicated by the data detailed in the 16:1 Multiplexer Power Assessment table in section 8.

References

- https://www.tutorialspoint.com/digital_circuits/digital_circuits_multiplexers.htm
- http://data.conferenceworld.in/IETEAUGUST2017/55.pdf
- https://en.wikipedia.org/wiki/Multiplexer
- https://www.quora.com/How-do-I-design-a-16-to-1-mux-using-one-8-1-mux-and-two-2-1-mux
- https://www.researchgate.net/figure/a-Block-diagram-of-one-16-1-MUX-channel-It-consists-of-15-single-2-1-MUX-stages_fig1_327441895
- http://data.conferenceworld.in/IETEAUGUST2017/55.pdf
- https://www.geeksforgeeks.org/multiplexers-in-digital-logic/