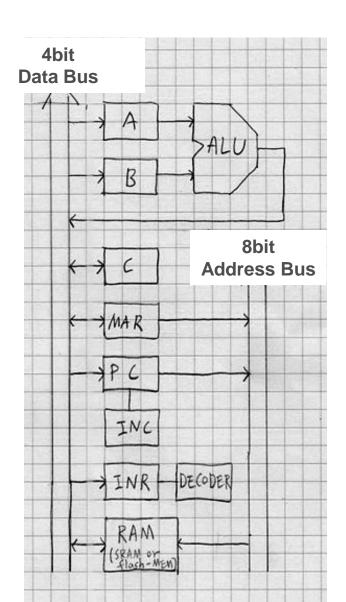




#### 전체 구성

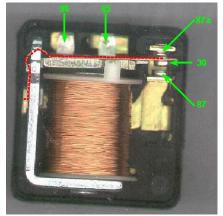
- 3개 레지스터
- **7**가지 연산기능 **ALU**
- Program Counter
- Instruction 레지스터(INR)
- 명령어 해독기(Decoder)
- 메모리 주소 레지스터(MAR)
- ROM

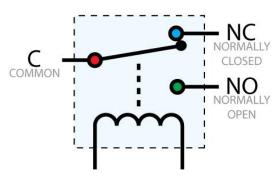


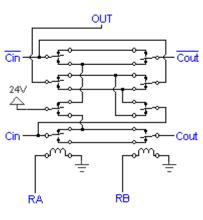


## Relay(릴레이)

- 전자석에 전류를 흘려줌으로써 스위치 역할을 하는 소자
- 트랜지스터의 스위칭 기능을 구현 가능







1-BIT FULL ADDER



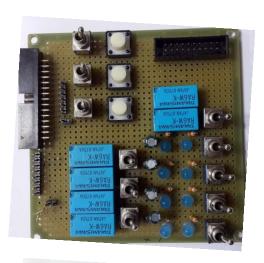
### **ALU & Register**

- ADD, AND, OR, XOR, NOT 5가지 논리연산
- Increaser(INC): +1, MSB Carry Out 표시 됨
- Left Shift 1Bit(LST): circulating, non-circulating 선택가능
- Register A,B 는 ALU 입력에 직결
- Register C는 범용 레지스터로 사용





# ALU & Register











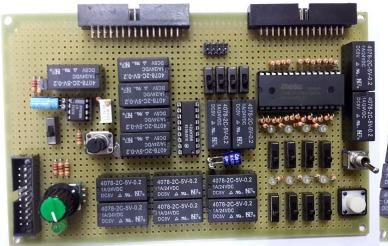
# Oscilator, State sequencer, Instruction register, Decoder

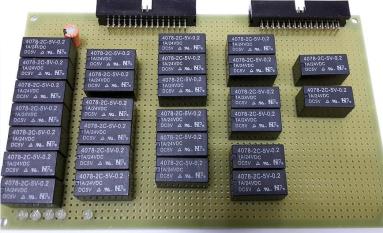
- Timer IC 555 기반 Oscilator, 수동 펄스 입력 가능
- 10-state sequencer
- Instruction register
- Decoder mux 사용 16가지 opcode 가능

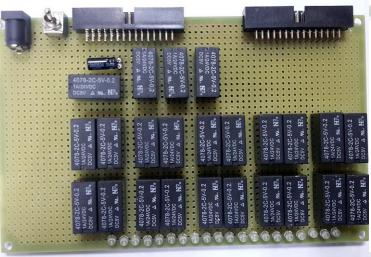
opcode		
0000	NOP	
0001		
0010	MOV A,C	TOWN DE SIZE AND THE PARTY OF T
0011	JUMP	2N - V - NOON
0100	Load A ) 15182101 27262 752	
0101	load B by Lond.	4078-2C-5V-0.2 4078-2C-5V-0.2 4078-2C-5V-0.2 4078-2C-5V-0.2 4078-2C-5V-0.2 4078-2C-5V-0.2 4078-2C-5V-0.2
0110	MOV MEN, C ) 747	4078-2C-3V-0.2 -0079-2C-3V-0.2
0111	MOV CIMEN 19202	
1000	HALT 7	COPY & N. AS. COPY & N. M. COPY & N. M.
1001	ADD	
1010	INC	9.9.9.9
1011	AND ALL	V
1100	OR ALU	
1101	XoK	
1110	NOT 2	Entractation Control and Contr
1111	LST A register	9.99

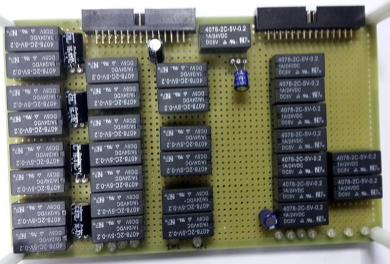


### Oscillator, FSM, INR, INC, MAR



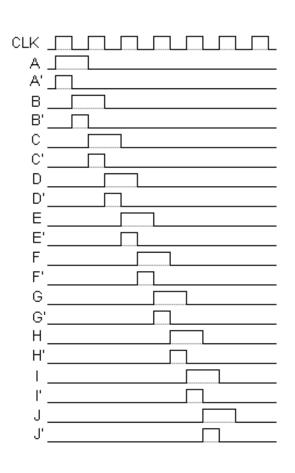


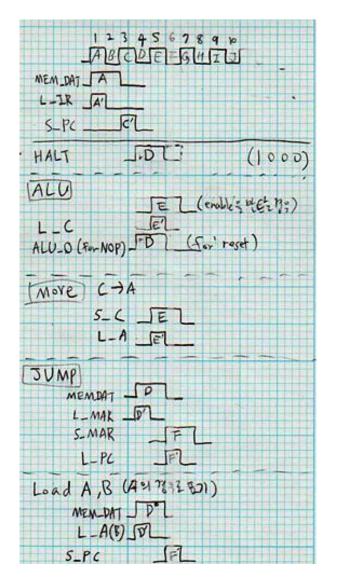






#### 10-State sequencer

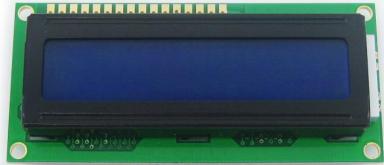






#### Character LCD

- 4비트 제어 가능
- A 레지스터는 제어
- B 레지스터의 2비트는 LCD enable용으로 사용





Upper bits bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)			0	0	P		F					9	≡,	O.	p
0001	CG RAM (2)		i	1	A	Q	₫	4				F	7	Ġ	ä	9
0010	CG RAM (3)		11	2	8	R	b	r			Г	4	ij	×	F	
0011	CG RAM (4)		#	3	C	5	C	S			.J	ŋ	Ŧ	ŧ	€.	60
0100	CG RAM (5)		\$	4	D	T	d	t.			ĸ.	I	ŀ	†	H	52
0101	CG RAM (6)		7.	5	E	U	9	IJ				7	<b>;</b>	1	Œ	ü
0110	CG RAM (7)		8.	6	F	Ų	f	Ų			ş	Ħ			ρ	Σ
0111	CG RAM (8)		7	7	6	W	9	IJ			7	#	X	7	9	Л
1000	CG RAM (1)		(	8	H	X	h	X			4	7	‡	IJ	<b>.</b> Г	X
1001	CG RAM (2)		)	9	I	Y	i	<b>'</b>			<u> </u>	丁	Į	ij	-:	닠
1010	CG RAM (3)		*	::	J	Z	j	Z			I		'n	ŀ	j	Ŧ
1011	CG RAM (4)		+	;	K	E	k	{			7	ţ			×	沔
1100	CG RAM (5)		;	<	<u>L</u>	¥	1	I			†?	=)	Į	ŋ	4	F
1101	CG RAM (6)				M		M	}				Z	^,	_,	<b>‡</b> .	÷
1110	CG RAM (7)			>	N	•	n	÷			3	t	#	• •	ñ	
1111	CG RAM (8)		1	?			0	÷				IJ	7		Ö	



#### Sample code 1/2

#### Printing "Hello World"

Add	lress	DATA				
7~4	3~0	-	comment			
0000	0000	0100	; Load A			
0000	0001	0010	; Set to 4 bit operation			
0000	0010	0100	; Load A			
0000	0011	0010	; Function set, 8 bit			
0000	0100	0100	; Load A			
0000	0101	1000	; 2nd nibble			
0000	0110	0100	; Load A			
0000	0111	0000	; Display ON, Cursor On, Cursor Blinking			
0000	1000	0100	; Load A			
0000	1001	1111	; 2nd nibble			
0000	1010	0100	; Load A			
0000	1011	0000	; Entry Mode, Increment cursor position, No display shift			
0000	1100	0100	; Load A			
0000	1101	0110	; 2nd nibble			
0000	1110	0101	; Load B			
0000	1111	0011	; RS=1, lcd not enable			
0001	0000	0100	; Load A			
0001	0001	0100	]; H			
0001	0010	0101	; Load B			
0001	0011	0001	; RS=1, lcd enable			
0001	0100	0100	; Load A			
0001	0101	1000	; 2nd nibble			
0001	0110	0100	; Load A			
0001	0111	0110	]; e			



## Sample code 2/2

Add	ress	DATA	comment
7~4	3~0	-	comment
0001	1000	0100	; Load A
0001	1001	0101	; 2nd nibble
0001	1010	0100	; Load A
0001	1011	0110	]; I
0001	1100	0100	; Load A
0001	1101	1100	; 2nd nibble
0001	1110	0100	; Load A
0001	1111	0110	]; I
0010	0000	0100	; Load A
0010	0001	1100	; 2nd nibble
0010	0010	0100	; Load A
0010	0011	0110	; o
0010	0100	0100	; Load A
0010	0101	1111	; 2nd nibble
0010	0110	0100	; Load A
0010	0111	0010	; space
0010	1000	0100	; Load A
0010	1001	0000	; 2nd nibble
0010	1010	0100	; Load A
0010	1011	0101	; w
0010	1100	0100	; Load A
0010	1101	0111	; 2nd nibble
0010	1110	0100	; Load A
0010	1111	0110	]; o

Add	ress	DATA	
7~4	3~0	-	comment
0011	0000	0100	; Load A
0011	0001	1111	; 2nd nibble
0011	0010	0100	; Load A
0011	0011	0111	] ; r
0011	0100	0100	; Load A
0011	0101	0010	; 2nd nibble
0011	0110	0100	; Load A
0011	0111	0110	]; I
0011	1000	0100	; Load A
0011	1001	1100	; 2nd nibble
0011	1010	0100	; Load A
0011	1011	0110	] ; d
0011	1100	0100	; Load A
0011	1101	0100	; 2nd nibble
0011	1110	0000	; NOP
0011	1111	1000	; HALT



시연

