1 Instruction Encoding

1.1 ARM7TDMI – ARM Instructions

The ARM7TDMI uses a fixed-length, 32-bit instruction encoding scheme for all ARM instructions. The basic encoding for all ARM7TDMI instructions is shown below. Individual instruction descriptions and encodings are shown in section 4 of this document.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Multiply (accumulate)	cond				0	0	0	0	0	0	A	S	Rd				Rn				Rs				1	0	0	1	Rm			
Multiply (accumulate) long	cond				0	0	0	0	1	U	A	S	RdHi				RdLo				Rn				1	0	0	1	Rm			
Branch and exchange	cond				0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	Rn			
Single data swap	cond				0	0	0	1	0	B	0	0	Rn				Rd				0	0	0	0	1	0	0	1	Rm			
Halfword data transfer, register offset	cond				0	0	0	P	U	0	W	L	Rn				Rd				0	0	0	0	1	0	1	1	Rm			
Halfword data transfer, immediate offset	cond				0	0	0	P	U	1	W	L	Rn				Rd				offset				1	0	1	1	offset			
Signed data transfer (byte/halfword)	cond				0	0	0	P	U	B	W	L	Rn				Rd				addr_mode				1	1	H	1	addr_mode			
Data processing and PSR transfer	cond				0	0	I	opcode				S	Rn				Rd				operand2											
Load/store register/unsigned byte	cond				0	1	I	P	U	B	W	L	Rn				Rd				addr_mode											
Undefined	cond				0	1	1																					1				
Block data transfer	cond				1	0	0	P	U	0	W	L	Rn				register list															
Branch	cond				1	0	1	L	offset																							
Coprocessor data transfer	cond				1	1	0	P	U	N	W	L	Rn				CRd				CP#				offset							
Coprocessor data operation	cond				1	1	1	0	CP opcode				CRn				CRd				CP#				CP			0	CRm			
Coprocessor register transfer	cond				1	1	1	0	CP opc			L	CRn				Rd				CP#				CP			1	CRm			
Software interrupt	cond				1	1	1	1	ignored by processor																							