Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits

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***Abstract*—The modular multilevel converter (MMC) has become the most promising converter technology for high-voltage direct current (HVDC) transmission systems. However, similar to any other voltage-sourced converter-based HVDC system, MMC-HVDC systems with the half-bridge submodules (SMs) lack the capability of handling dc-side short-circuit faults, which are of severe concern for overhead transmission lines. In this paper, two new SM circuit configurations as well as a hybrid design methodology to embed the dc-fault-handling capability in the MMC-HVDC systems are proposed. By combining the features of various SM configurations, the dc-fault current path through the freewheeling diodes is eliminated and the dc-fault current is enforced to zero. Several MMC configurations based on the proposed hybrid design method and various SM circuits, that is, the half-bridge, the full-bridge, the clamp-double, and the five-level cross-connected SMs, as well as the newly proposed unipolar-voltage full-bridge and three-level cross-connected SMs, are investigated and compared in terms of the dc-fault-handing capability, semiconductor power losses, and component requirements. The studies are carried out based on time-domain simulation in the PSCAD/EMTDC software environment for various SM configurations and dc-fault conditions. The reported study results demonstrate the proposed hybrid-designed MMC-HVDC system based on the combination of the half-bridge and the proposed SM circuits is the optimal design among all evaluated systems in terms of the dc-fault-handing capability, semiconductor power losses, and component requirements.**

***Index Terms*—DC-side short-circuit fault, fault clearance, modular multilevel converter (MMC).**

I. Introduction

THE MODULAR multilevel converter (MMC) has become the most attractive converter topology for voltage-sourced converter (VSC) high-voltage direct-current (HVDC) transmission systems because of its modularity and scalability [1]–[11].

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One of the major challenges associated with the MMC-HVDC systems with the conventional half-bridge submodules (SMs) is the lack of the dc-fault-handling capability. This problem is of severe concern, particularly for HVDC transmission systems with overhead lines.

The existing solutions to interrupt and clear the dc-side short-circuit fault of an MMC-HVDC system can be summarized as follows.

- Opening the ac-side circuit breakers (CBs). This solution is not sufficiently fast as it takes a few cycles (e.g., 2 to 3 cycles) for the CB to trip. Consequently, the freewheeling diodes of the MMC that form an uncontrolled rectifier should tolerate the high fault current for a few cycles. Although parallel connection of a protective thyristor with each SM can bypass the short-circuit current flowing through the diodes, the fault current interruption relies on tripping the ac CBs [5], [12]–[15].
- Employing the dc-side CBs. Although a solid-state dc CB for HVDC applications has recently been developed, the technology is not sufficiently mature and cost-effective [14], [16]–[20].
- Embedding the dc-fault-handling capability in the HVDC converter station. As of now, the MMC-HVDC systems have been realized mainly based on a single SM circuit configuration, that is, the half-bridge, the full-bridge, or the clamp-double SMs [4], [11], [15], [20]–[22]. The MMC topology with the full-bridge or clamp-double SMs eliminates the current path of the freewheeling diodes and can potentially interrupt the fault current within a fraction of a second. However, compared to the MMC with the half-bridge SMs, this solution sacrifices the cost and power losses. Although the alternate arm converter proposed in [23] and [24] combines the features of the two-level and the MMC based on the full-bridge SMs to handle the dc-side short-circuit faults, it still has the drawbacks of the MMC with the full-bridge SMs and does not provide a tradeoff between the number of required components and efficiency of the system.

This paper aims at exploiting the salient features of various SM circuit configurations to handle the dc-side short-circuit faults of an MMC-HVDC system without significant penalties on the cost and efficiency of the system. This paper proposes two new SM circuits as well as a hybrid design methodology to embed the dc-fault-handling capability in the MMC. The proposed

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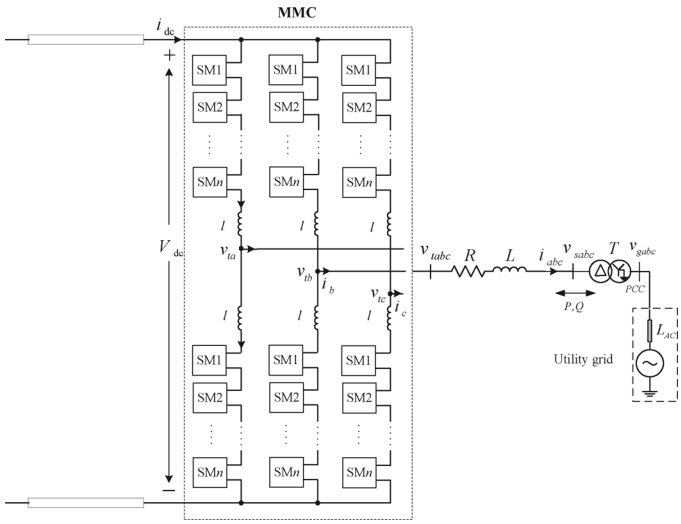

Fig. 1. Schematic representation of an MMC-HVDC converter station.

hybrid design methodology is realized based on a combination of the half-bridge SMs with the full-bridge, the clamp-double, the five-level cross-connected SMs, or the two newly proposed unipolar-voltage full-bridge and three-level cross-connected SMs. Based on the hybrid design method, by replacing a number of half-bridge SMs of the MMC system with those SMs with the dc-fault-handling capability, the dc-fault-handling capability can be embedded without changing the control/modulation methods. In the proposed hybrid MMC configuration, any dc-side short-circuit fault is interrupted by blocking all of the switching devices of the SMs within a fraction of a second. Based on the proposed design concept, the MMCs with variants of SMs are investigated and compared in terms of their semiconductor device requirements and power losses. The studies are carried out based on time-domain simulation in the PSCAD/EMTDC environment for various SM configurations, under dc-fault conditions.

The rest of this paper is organized as follows. Section II analyzes various SM circuit topologies which can be used for the MMC-HVDC system. Section II also introduces two new SM circuits, that is, a unipolar-voltage full-bridge and a three-level cross-connected SM. Section III proposes the hybrid design methodology for the MMC-HVDC systems. Section IV presents the principle of dc-side fault clearance of the hybrid MMC-HVDC system. Section V presents the study results. Section VI provides some discussions and Section VII concludes this paper.

II. SM Circuit Topologies

Figure 1 shows a schematic diagram of a point-to-point MMC-HVDC converter station. The MMC, as shown in Fig. 1, consists of two arms per each phase where each arm is comprised of n series-connected, nominally identical SMs, and a series-connected inductor. The dc side of the MMC is connected to the dc transmission line while its ac side is connected to a utility grid through a three-phase transformer.

Each SM of the MMC of Fig. 1 can be realized by the following circuits [4], [25], [26]:

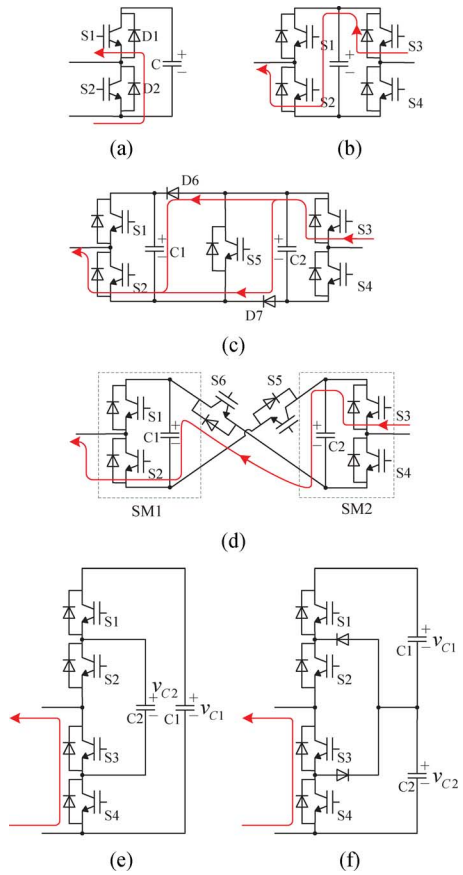

Fig. 2. Various SM topologies: (a) the half-bridge, (b) the full-bridge, (c) the clamp-double, (d) the five-level cross-connected, (e) the three-level FC, and (f) the three-level NPC SM.

- The half-bridge SM circuit: As shown in Fig. 2(a), due to having only two switches within each SM, the efficiency of an MMC-HVDC system based on the half-bridge SMs is high. During a dc-side short-circuit fault, the fault current, as shown in Fig. 2(a), flows from the ac side toward the dc side through the antiparallel diodes of the SMs [4]. Once a fault occurs, two phases need to be considered:
  1) In Phase I, prior to detection of the fault, due to a large amount of inserted SMs in the short-circuit loop, the discharging current of the SM capacitors dominates the dc-fault current.
  2) Phase II, subsequent to detection of the fault and blocking all of the IGBTs, the dc-fault current flows from the ac side. The amplitude of the fault current is determined by the ac-side system parameters, arm inductors, dc transmission lines/cables characteristics, and the fault location.
- The full-bridge SM circuit: As shown in Fig. 2(b), the power losses as well as the cost of the full-bridge MMC-HVDC system are significantly higher than the half-bridge one. Subsequent to a dc-side fault, when all of the IGBTs of the SMs are blocked, the capacitor voltages can generate reverse voltages to block the ac-side currents, as shown in Fig. 2(b). Thus, the full-bridge SMs can provide the dc-fault-handling capability [4].

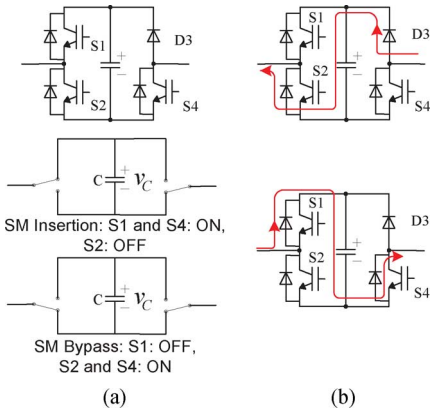

Fig. 3. Proposed unipolar voltage full-bridge SM circuit: (a) normal operation and (b) its current path when all switches are turned off.

- The clamp-double SM circuit: As shown in Fig. 2(c), compared to the half- and full-bridge MMCs with the same number of voltage levels, the clamp-double MMC has higher semiconductor losses than the half-bridge MMC and lower than the full-bridge MMC. In the clamp-double MMC-HVDC system, although the SMs have the capability of blocking the dc-fault current, they can only generate a reverse voltage $V_{\mathrm{dc}}/2$ per arm, that is, half of the reverse voltage produced by the full-bridge SMs per arm. Thus, the clamp-double MMC needs more time to drive the fault current to zero [4].
- The five-level cross-connected SM circuit: During a fault, the two capacitors of the five-level cross-connected SM connected in series can block the short-circuit current, as shown in Fig. 2(d). The five-level cross-connected MMC system can generate a reverse voltage V_{dc} per arm, which is the same as the voltage produced by the full-bridge MMC [25].
- The three-level SM circuit: As shown in Fig. 2(e) and (f), similar to the half-bridge SM, the three-level NPC and FC SMs do not provide any dc-fault-handling capability. Furthermore, from a manufacturing perspective, that is, cost, control, and number of components per SM, this solution is not very attractive [26].

In addition to the aforementioned SM circuit configurations, two types of improved SM circuits with the dc-fault-handling capability are proposed in this paper:

- The proposed unipolar-voltage full-bridge SM: As shown in Fig. 3, the circuit is based on the full-bridge SM whose IGBT *S*3 and its antiparallel diode are replaced by the diode *D*3. During normal operation, as shown in Fig. 3(a), by controlling the switches *S*1 and *S*2, the SM is inserted/bypassed while the switch *S*4 is always on. Under normal conditions, the unipolar-voltage full-bridge SM can output the voltage levels zero and v_C. The possible switching states and their impacts on the SM capacitor voltage are listed in Table I. Assuming that the semiconductor devices of the switches *S*1 to *S*3 in the unipolar-voltage full-bridge SM are identical to those of the full-bridge SM, their conduction losses are identical. However, the conduction losses of the conducting switch *S*4 are greater than any one of the other switches. That is similar to the clamp-double SM, where, as shown in Fig. 2(c), during normal operation, the switch *S*5 remains always on. During a dc-side short-circuit fault, the operation and fault current path of a unipolar-voltage full-bridge SM, shown in Fig. 3(b), is similar to those of a full-bridge SM. Therefore, the proposed unipolar-voltage full-bridge SM can block dc-fault current and provide the dc-fault-handling capability.
- The proposed three-level cross-connected SM: As shown in Fig. 4, the circuit is derived from the clamp-double and five-level cross-connected SMs. Operation of the three-level cross-connected SM, during normal operation, is similar to the clamp-double SM, as shown in Fig. 4(a). Assuming $v_{C1} = v_{C2} = v_C$, the three-level cross-connected SM can output three voltage levels, that is, 0, v_C, and $2v_C$. The possible switching states and their impacts on the SM capacitor voltages are shown in Table II. In the proposed SM, the conduction losses and blocking voltage for the conduction switch *S*5 are higher than those for the switches *S*1–*S*4. Unlike the clamp-double MMC, the three-level cross-connected MMC can generate a reverse voltage V_{dc} per arm, that is, the same as the reverse voltage

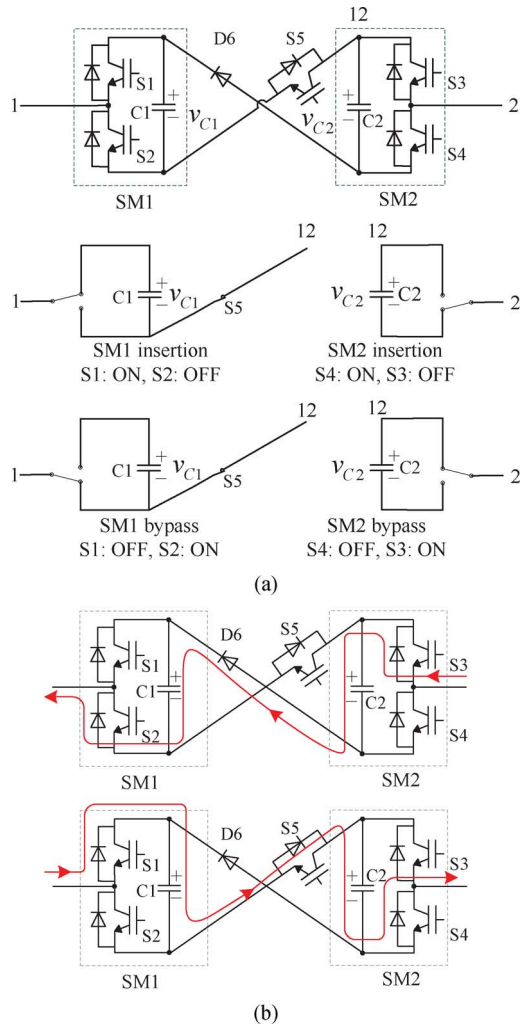

Fig. 4. Proposed three-level cross-connected SM circuit: (a) normal operation and (b) its current path when all switches are turned off.

TABLE I
SWITCHING STATES AND THEIR IMPACTS ON THE CAPACITOR VOLTAGE OF A UNIPOLAR-VOLTAGE FULL-BRIDGE SM

S1	S2	S4	i_{arm}	v_C	v_{out}
1	0	1	>0	$\uparrow$	v_C
1	0	1	<0	$\downarrow$	v_C
0	1	1	$\times$	$-$	0
1	0	0	>0	$\uparrow$	v_C
1	0	0	<0	$-$	0
0	1	0	>0	$-$	0
0	1	0	<0	$\uparrow$	v_C
0	0	0	>0	$\uparrow$	v_C
0	0	0	<0	$\uparrow$	v_C

TABLE II
SWITCHING STATES AND THEIR IMPACTS ON THE CAPACITOR VOLTAGE OF A THREE-LEVEL CROSS-CONNECTED SM

S1	S2	S3	S4	S5	i_{arm}	v_{C1}	v_{C2}	v_{out}
SM1								v_{1-12}
1	0	$\times$	$\times$	1	>0	$\uparrow$	$\times$	v_{C1}
1	0	$\times$	$\times$	1	<0	$\downarrow$	$\times$	v_{C1}
0	1	$\times$	$\times$	1	$\times$	$-$	$\times$	0
SM2								v_{12-2}
$\times$	$\times$	0	1	1	>0	$\times$	$\uparrow$	v_{C2}
$\times$	$\times$	0	1	1	<0	$\times$	$\downarrow$	v_{C2}
$\times$	$\times$	1	0	1	$\times$	$\times$	$-$	0
Fault								v_{1-2}
0	0	0	0	0	>0	$\uparrow$	$\uparrow$	$v_{C1}+v_{C2}$
0	0	0	0	0	<0	$\uparrow$	$\uparrow$	$v_{C1}+v_{C2}$

produced by the full-bridge MMC. Thus, compared to the full-bridge MMC, the three-level cross-connected MMC takes the same time to drive the fault current to zero.

Assuming that n is the total number of the SMs in each arm and N_C is the total number of SM capacitors within each arm, then $n = N_C$ in the half-bridge, full-bridge, and unipolar-voltage full-bridge MMC systems, and $n = N_C/2$ in the clamp-double and three/five-level cross-connected MMC systems.

III. PROPOSED HYBRID DESIGN OF THE MMC–HVDC SYSTEM

Conventionally, the MMC–HVDC system is realized based on a single type of SM circuit configuration, that is, the half-bridge SMs for underground or subsea cables, the full-bridge, or the clamp-double SMs for overhead lines. However, there is a tradeoff between the prominent advantages and disadvantages of the MMC-HVDC systems based on either of the SMs. Although the half-bridge MMC does not provide any dc-fault-handling capability, it provides the highest efficiency and lowest cost, all due to the lowest number of components. The full-bridge and clamp-double MMCs do provide the dc-fault-handling capability but sacrifice efficiency and cost. To pursue the optimal design in terms of the fault-handling capability, efficiency, and cost, a hybrid design method is introduced to develop an MMC system that borrows different features of various SM circuit configurations. The hybrid design concept in this paper refers to using two types of SMs in the design of an MMC system, that is, the half-bridge SM for lower losses in conjunction with an SM which provides the dc-fault-handling capability, that is, the full-bridge, the clamp-double, and the proposed unipolar-voltage full-bridge and three-level cross-connected SMs. In this way, the hybrid-designed MMC system can potentially offer lower losses and cost, compared to the full-bridge and clamp-double MMC systems, while possessing the dc-fault-handling capability. Figure 5 shows a hybrid-designed MMC-HVDC system which is composed of the half- and full-bridge SMs.

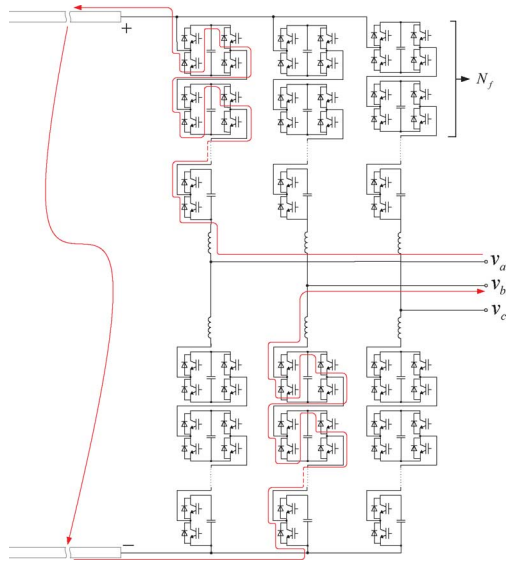

Fig. 5. Block diagram of a hybrid MMC-HVDC system, including the half-bridge and full-bridge SMs with a highlighted dc-fault current path.

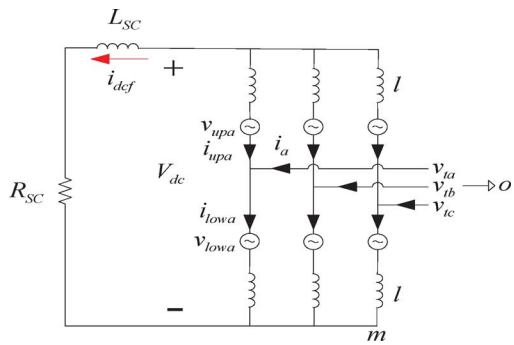

Fig. 6. Equivalent circuit of an MMC system during phase I of a dc-side short-circuit fault.

IV. PRINCIPLE OF DC-SIDE FAULT CLEARANCE IN A HYBRID MMC–HVDC SYSTEM

A. Phase I: Prior to Fault Detection

Similar to the conventional MMC-HVDC system, the hybrid MMC-HVDC system has the same equivalent circuit during phase I of a dc fault, as shown in Fig. 6. The dc-fault current is mainly dominated by discharging current of the on-state SM capacitors during phase I. Considering the upper and lower loop, the dynamics of the converter during phase I are described as follows:

$$v_{tj} + V_{\mathrm{om}} + l\frac{di_{\mathrm{upj}}}{dt} + v_{\mathrm{upj}} = L_{\mathrm{SC}}\frac{di_{\mathrm{dcf}}}{dt} + R_{\mathrm{SC}}i_{\mathrm{dcf}}, \quad (1)$$

$$v_{tj} + V_{\mathrm{om}} = l\frac{di_{\mathrm{lowj}}}{dt} + v_{\mathrm{lowj}} \quad (2)$$

where $j = a, b, c$, and L_{SC} and R_{SC} represent the equivalent values of the inductance and resistance of the transmission line including the short-circuit fault resistance. Adding the equations

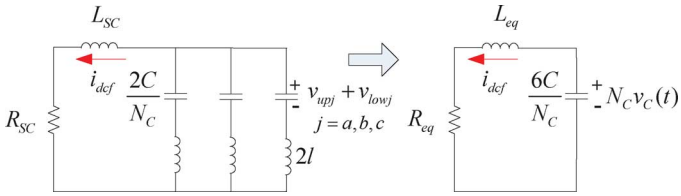

Fig. 7. Simplified equivalent circuit of Fig. 6.

in (1) and (2) for the three phases and subtracting one from the other one, and assuming a balanced three-phase system, yield

$$\frac{1}{3}\sum_{j=a,b,c}(v_{upj}+v_{\mathrm{lowj}}) = L_{\mathrm{eq}}\frac{di_{\mathrm{dcf}}}{dt} + R_{\mathrm{eq}}i_{\mathrm{dcf}} \tag{3}$$

where $L_{\mathrm{eq}} = L_{\mathrm{SC}} + 2l/3$ and $R_{\mathrm{eq}} = R_{\mathrm{SC}}$. Equation (3) shows that the dc-fault current is mainly dominated by discharging the on-state SM capacitors during phase I. Subsequent to the fault occurrence, in each phase of the MMC, there are N_C series-connected capacitors with an equal initial voltage V_{dc} that is discharged in each phase. Assuming that the SM capacitor voltages are balanced at the same value and all capacitors will discharge the energy equally, the equivalent capacitance of each phase and the total capacitance of the three-phase MMC, as shown in Fig. 7, are $2C/N_C$ and $6C/N_C$, respectively. The dynamics of the dc-fault current i_{dcf} are expressed as

$$i_{\mathrm{dcf}} = -\sum_{j=a,b,c}\frac{2C}{N_C}\frac{d(v_{\mathrm{upj}}+v_{\mathrm{lowj}})}{dt}. \tag{4}$$

Assuming all capacitor voltages are balanced at $v_C(t)$ and $N_C v_C(t) = v_{\mathrm{upj}} + v_{\mathrm{lowj}}$, (4) can be simplified to

$$i_{\mathrm{dcf}} = -6C\frac{dv_C}{dt}. \tag{5}$$

Based on (3) and (5), it is deduced as

$$\frac{d^2 i_{\mathrm{dcf}}}{dt^2} + \frac{R_{\mathrm{eq}}}{L_{\mathrm{eq}}}\frac{di_{\mathrm{dcf}}}{dt} + \frac{1}{L_{\mathrm{eq}}C_{\mathrm{eq}}}i_{\mathrm{dcf}} = 0 \tag{6}$$

where $C_{\mathrm{eq}} = 6C/N_C$. Solving the second-order equation (6), the dc-fault current during phase I can be deduced. In this paper, only the condition in which $R_{\mathrm{eq}} < 2\sqrt{L_{\mathrm{eq}}/C_{\mathrm{eq}}}$ is assumed. Based on [27], assuming that the fault occurs at $t = 0$, the solution with the initial condition of $N_C v_C(0) = V_{\mathrm{dc}}$ and $i_{\mathrm{dcf}}(0) = I_{\mathrm{dcf}}$ is

$$i_{\mathrm{dcf}} = -\frac{I_{\mathrm{dcf}}\omega_0}{\omega}e^{-\delta t}\sin(\omega t - \beta) + \frac{V_{\mathrm{dc}}}{\omega L_{\mathrm{eq}}}e^{-\delta t}\sin(\omega t) \tag{7}$$

where $\omega_0 = \sqrt{1/(L_{\mathrm{eq}}C_{\mathrm{eq}})}$, $\delta = R_{\mathrm{eq}}/(2L_{\mathrm{eq}})$, $\omega = \sqrt{1/(L_{\mathrm{eq}}C_{\mathrm{eq}}) - (R_{\mathrm{eq}}/(2L_{\mathrm{eq}}))^2}$, and $\beta = \arctan(\omega/\delta)$. Thus, prior to the fault detected, the accurate maximum fault current can be calculated by (7) with a given detection time t_d. When the dc fault occurs, the changing rate of the fault current can be determined by the derivative of (7) at $t = 0$, which is expressed by

$$k = \frac{di_{\mathrm{dcf}}}{dt}|_{t=0} = -\frac{I_{\mathrm{dcf}}\omega_0\delta}{\omega}\sin\beta - I_{\mathrm{dcf}}\omega_0\cos\beta + \frac{V_{\mathrm{dc}}}{L_{\mathrm{eq}}}. \tag{8}$$

Assuming a small detection time t_d, the maximum current can be estimated as kt_d.

Based on the aforementioned analysis, the maximum fault current can be determined. During phase I, the SMs are switched on/off by a voltage-balancing strategy and the fault current flows through the IGBTs and diodes of each arm which are required to withstand one-third of the possible maximum fault current under the specified detection time t_d.

B. Phase II: Subsequent to Fault Detection

In the hybrid MMC-HVDC system, assuming that N_f represents the number of series-connected SM capacitors per arm in the short-circuit loop, subsequent to fault detection when all IGBTs are turned off, the steady-state SM capacitor voltage $V_{\mathrm{cap\_fault}}$ satisfies the following inequality:

$$2N_f V_{\mathrm{cap\_fault}} \geq V_{\mathrm{amp}\_LL} \tag{9}$$

where V_{amp_LL} is the amplitude of the ac-side line-to-line voltage. Equation (9) implies that N_f series-connected SM capacitors in each arm can produce a voltage opposed to the ac-side voltage to block the fault current, as shown in the example of the MMC-HVDC system of Fig. 5. During normal operation, if

$$2N_f v_C < V_{\mathrm{amp}\_LL} \tag{10}$$

when a dc-side short-circuit fault occurs, the capacitors of the SMs with the dc-fault-handling capability are charged to $V_{\mathrm{cap}} = V_{\mathrm{amp}\_LL}/2N_f$ and, consequently, block the fault current after being charged.

To ensure that the SM capacitor voltages during a fault are maintained at their nominal values $V_{\mathrm{cap\_ref}}$, based on (9), N_f can be ideally determined by

$$N_f \geq \frac{V_{\mathrm{amp}\_LL}}{2V_{\mathrm{cap\_ref}}}. \tag{11}$$

Subsequently, the required number of the SMs can be determined.

The number of series-connected capacitors in the SMs with the fault-handling capability determines the fault-blocking time. The higher this number is, the higher reverse voltage is generated by the SMs with the fault-handling capability. For the MMC-HVDC systems based on a single type of the full bridge, the unipolar-voltage full-bridge, the three-level, or the five-level cross-connected SMs, they have the blocking voltage V_{dc} per arm and can block the fault current faster than the clamp-double MMC-HVDC which has a blocking voltage $V_{\mathrm{dc}}/2$. For the hybrid MMC-HVDC system, since the blocking voltage generated by each arm is smaller than that of the full-bridge MMC-HVDC, the fault-blocking time is longer than the full-bridge MMC-HVDC system.

Subsequent to fault detection, all IGBTs are blocked and the fault current is interrupted within a short period of time. If the fault is permanent, the system will be kept in off-state mode. If the fault is non-permanent, when the fault is cleared completely, the converter starts to recover the power transfer and, consequently, the system returns to its normal operation.

TABLE III
PARAMETERS OF THE STUDY MMC–HVDC SYSTEM OF FIG. 1

Quantity	Value
MMC nominal power (and S_b)	50 MVA
AC system nominal voltage (and V_b)	138 kV
AC System inductance L_{AC}	150 mH
Short Circuit Ratio (SCR) at the PCC	5
Nominal frequencies f_1 and f_2	60 Hz
Transformer voltage rating T	138 kV/30 kV (Y/Δ)
Transformer power rating	55 MVA
Transformer leakage reactance	5%
Transformer loss	1%
R	0.03 Ω
L	5 mH
l	3 mH
DC Source Voltage V_{dc}	60 kV
Number of SM capacitors per arm N_C	20
SM capacitor C	14000 μF

V. STUDY RESULTS

In this section, the performance of various MMCs with different SM configurations is evaluated and compared based on simulation studies conducted on a 21-level MMC-HVDC converter station in the PSCAD/EMTDC environment. The study system parameters are listed in Table III.

A. Case 1: Comparative Studies for Various MMC Configurations

In Table IV, six MMC configurations based on the half-bridge, the full-bridge, the clamp-double, the unipolar-voltage full-bridge, the three-level cross-connected, and the five-level cross-connected SMs in terms of the semiconductor power losses and the required number of semiconductor components are compared. In normal operating mode, the MMC system of Fig. 1 is in a steady-state condition and 25-MW real power flows from the dc side to the ac side. The system also provides 18-MVar reactive power. The semiconductor power losses and the number of required SMs, capacitors, and IGBTs/diodes are listed in Table IV. The estimated switching and conduction losses that are based on the IGBT module 5SNA2000K451300 and the calculation method in [28], [29] are calculated as a percentage of the transferred real power. In the three-level cross-connected SM, to meet the required voltage ratings of the switch *S*5 and diode *D*6, two series-connected IGBT modules and diodes are used for realization of the switch *S*5 and diode *D*6, respectively. Similarly, for the five-level cross-connected SM, two series-connected IGBT modules/diodes are used for realization of the switch *S*5 *S*6. As shown in Table IV, for the same number of voltage levels, the half-bridge MMC provides the minimum power losses while the full-bridge, the unipolar-voltage full-bridge, the three-level, and the five-level cross-connected MMC provides the maximum power losses. The number of required IGBTs/diodes are the highest for the full-bridge and the five-level cross-connected MMC and the least for the half-bridge MMC.

In Table V, five hybrid MMC-HVDC systems with the dc-fault-handling capability are presented and compared. The required number of series-connected SM capacitors, which are used to block the dc-fault current, are determined by (11) and set to $N_f = 8$, the minimum value among all possible results to obtain low-power losses and component requirements. This means that for each hybrid-designed scheme, eight series-connected capacitors in the SMs with the dc-fault-handling capability are required during a fault. The number of the required half-bridge SMs can be calculated based on the corresponding system configuration and N_f. Based on the same control strategy and operating conditions, the hybrid MMCs in Table V have the same semiconductor losses if all switches are identical, which are smaller than the MMCs with the dc-fault-handling capability in Table IV. The extra power losses of the hybrid-designed MMCs are mainly due to the conduction losses of the conducting switches. If the semiconductor switches with lower conduction losses are used as the conducting switches, the extra power losses can be further reduced. Based on Tables IV and V, the hybrid designs III and V require the lowest number of semiconductor components. Therefore, the hybrid MMCs III and V with respect to the dc-fault-handling capability and efficiency are the optimal MMCs among all possible designed configurations in Tables IV and V. In Fig. 8, the arm configuration of the hybrid MMC V is shown, where 4 three-level cross-connected and 12 half-bridge SMs are connected in series. In Fig. 9, the power losses associated with the aforementioned MMC-HVDC systems are depicted as a percentage of the real power transferred over a wide operating range. As shown in Fig. 9, among all of the considered MMC configurations, the half-bridge MMC has the minimum losses. Furthermore, the hybrid MMCs provide the highest efficiency when compared to the full-bridge and clamp-double MMCs over a wide operating range.

B. Case 2: DC-Side Fault Handling Based on Hybrid Design III and V

In this section, the dc-fault-handling capability of the hybrid-designed MMC systems is demonstrated. Figure 10 shows the study results of the hybrid design III. Initially, the system of Fig. 1 is in a steady-state condition, that is, $P = 25$ MW and $Q = 18$ MVar. At $t = 0.5$ s, a dc-side short-circuit fault occurs, lasting for 100 ms. The fault is cleared at $t = 0.7$ s when the MMC system is recovered to transfer power.

Subsequent to the fault occurrence and before the fault is detected, as shown in Fig. 10(b), the dc fault current increases to the peak. Once the fault is detected and all IGBTs are turned off, the dc current can be blocked. The transferred real and reactive power are shown in Fig. 10(c). As shown in Fig. 10(d) and (e), the capacitor voltages of the lower and upper arms of phase-a are maintained at their nominal values during the fault. The upper and lower arm currents of phase-a are shown in Fig. 10(f). The three-phase currents and line-to-line voltages of the MMC-HVDC systems are shown in Fig. 10(g) and (h). As shown in Fig. 10, after turning off all of the IGBTs, there are no overcurrent or overcharged capacitor phenomena. The corresponding simulation results for the hybrid design V are also shown in Fig. 11, which are identical to the results shown in Fig. 10. Figures 10 and 11 demonstrate the dc fault-handling capability of the proposed hybrid MMC configurations along with the associated SM circuits. The results of Figs. 10 and 11 confirm that, subsequent to fault detection, the hybrid-designed MMCs react to the fault in a similar way. The only difference is the fault

TABLE IV
COMPARISON OF THE MMC CONFIGURATIONS WITH VARIOUS SMS

MMC configuration	Half-bridge MMC	Full-bridge MMC	Clamp-double MMC	Unipolar-voltage full-bridge MMC	Three-level cross-connected MMC	Five-level cross-connected MMC
SM circuit	HBSM	FBSM	CDSM	UFBSM	3LCCSM	5LCCSM
Dc-fault-handling capability	×	✓	✓	✓	✓	✓
Voltage levels	21	21	21	21	21	21
No. of capacitors per arm	20	20	20	20	20	20
No. of SMs per arm	20	20	10	20	10	10
No. of IGBTs/diodes per arm (inserting/bypassing SMs)	40	80	40	40	40	40
No. of extra switches per arm (conducting switches)	0	0	10 ($S5$)	20 ($S4$)	20 ($S5$)	40 ($S5, S6$)
No. of extra diodes per arm	0	0	20 ($D6, D7$)	20 ($D3$)	20 ($D6$)	0
Estimated power loss	0.69%	0.96%	0.83%	0.96%	0.83%	0.83%
Extra power loss compared to the half-bridge MMC	0	38%	19%	38%	38%	38%

TABLE V
COMPARISON OF THE HYBRID MMC CONFIGURATIONS WITH VARIOUS SMS

MMC configuration	Hybrid design I	Hybrid design II	Hybrid design III	Hybrid design IV	Hybrid design V
SM circuit	HBSM+FBSM	HBSM+CDSM	HBSM+UFBSM	HBSM+5LCCSM	HBSM+3LCCSM
Dc-fault-handling capability	✓	✓	✓	✓	✓
Voltage levels	21	21	21	21	21
No. of capacitors per arm	20	20	20	20	20
No. of SMs per arm	20	12	20	16	16
No. of HBSM per arm	12	4	12	12	12
No. of FBSM per arm	8	0	0	0	0
No. of CDSM per arm	0	8	0	0	0
No. of UFBSM per arm	0	0	8	0	0
No. of 5LCCSM per arm	0	0	0	4	0
No. of 3LCCSM per arm	0	0	0	0	4
No. of IGBTs/diodes per arm (inserting/bypassing SMs)	56	40	40	40	40
No. of extra switches per arm (conducting switches)	0	8 ($S5$)	8 ($S4$)	16 ($S5, S6$)	8 ($S5$)
No. of extra diodes per arm	0	16 ($D6, D7$)	8 ($D3$)	0	8 ($D6$)
Estimated power loss	0.798%	0.798%	0.798%	0.798%	0.798%
Extra power loss compared to the half-bridge MMC	16%	16%	16%	16%	16%

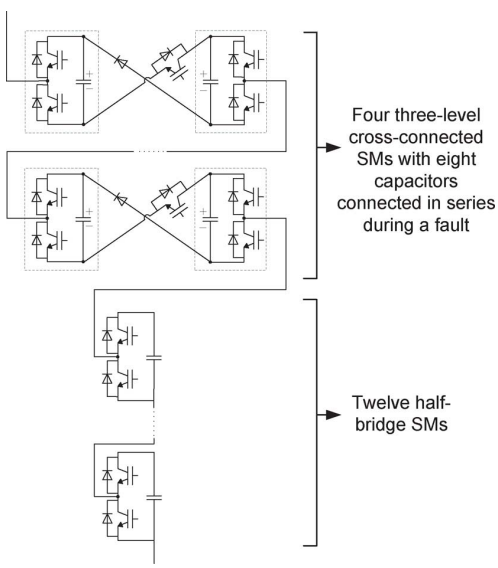

Fig. 8. Arm configuration of the hybrid MMC V (combining the three-level cross-connected and the half-bridge SMs).

blocking time, which is influenced by the number of inserted SMs and, consequently, the number of series-connected capacitors in the short-circuit loop during the dc-fault condition. This is studied in the next case study.

C. Case 3: DC Fault Current Blocking Time

Initially, the MMC-HVDC system is in a steady-state condition, that is, $P = 25$ MW and $Q = 18$ MVar. At $t = 0.5$ s, a dc-side short-circuit fault occurs, which lasts for 100 ms. In the study system, $R_{\text{eq}} = 1.1\ \Omega$, $L_{\text{eq}} = 2$ mH, and $C_{\text{eq}} = 4.2$ mF. Subsequent to the fault occurrence, based on (8), the rate of fault current change is $k = 30\ \text{A}/\mu\text{s}$. Assuming that the fault detection time is $t_d = 68\ \mu$s, the peak fault current is estimated as $kt_d - 25\ \texttt{MW}/60\ \texttt{kV} = 1.62$ kA. Subsequent to fault detection when all IGBTs are blocked, as shown in Fig. 12(a)–(c), the dc fault current in the hybrid MMC-HVDC systems is completely blocked within 400 μs, which is longer than that of the full-bridge MMC-HVDC system. The reason is that in the full-bridge MMC-HVDC, 20 capacitors per arm are connected in series to block the dc fault current while in the hybrid MMC-HVDC systems, 8 series-connected capacitors

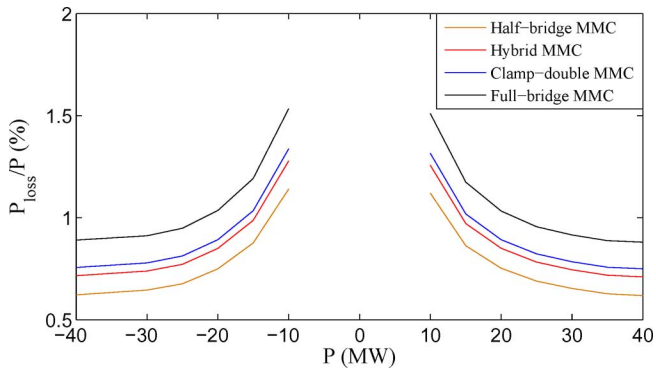

Fig. 9. Estimated semiconductor power losses as a percentage of transferred real power ($Q = 18$ MVar).

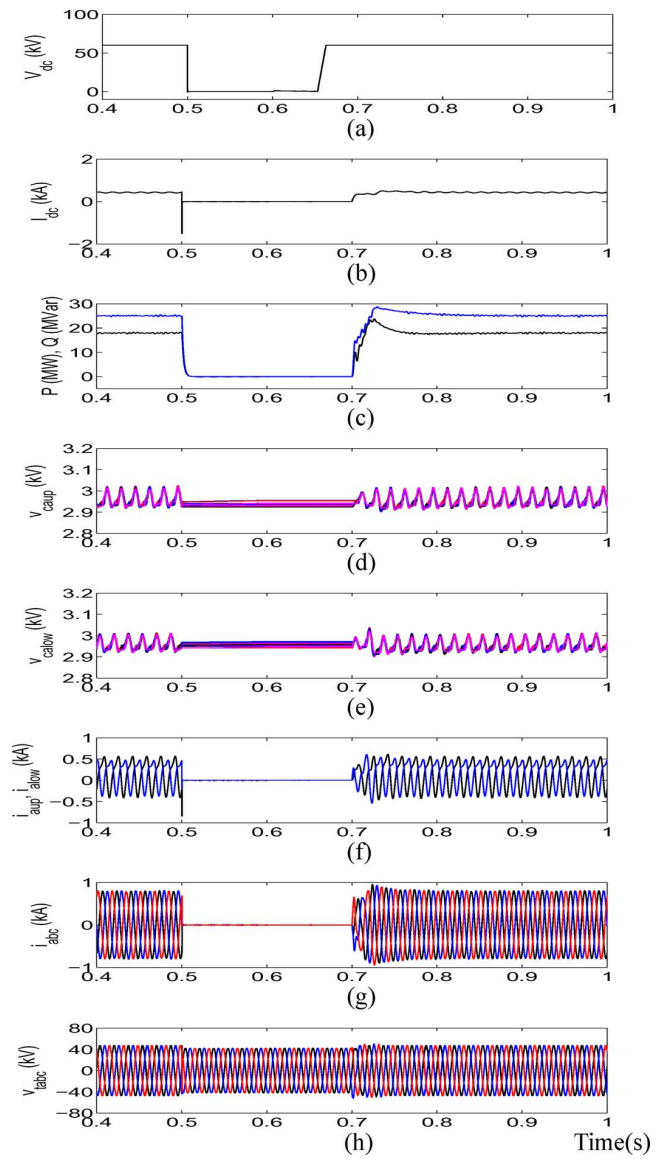

Fig. 10. DC-side short-circuit fault handling of the hybrid-designed MMC-HVDC system (hybrid design III) with the half-bridge and unipolar-voltage full-bridge SMs: (a) and (b) dc voltage and current, (c) real and reactive power, (d) and (e) SM capacitor voltages of the upper and lower arms of phase-a, (f) phase-a arm currents, and (g) and (h) ac-side currents and voltages.

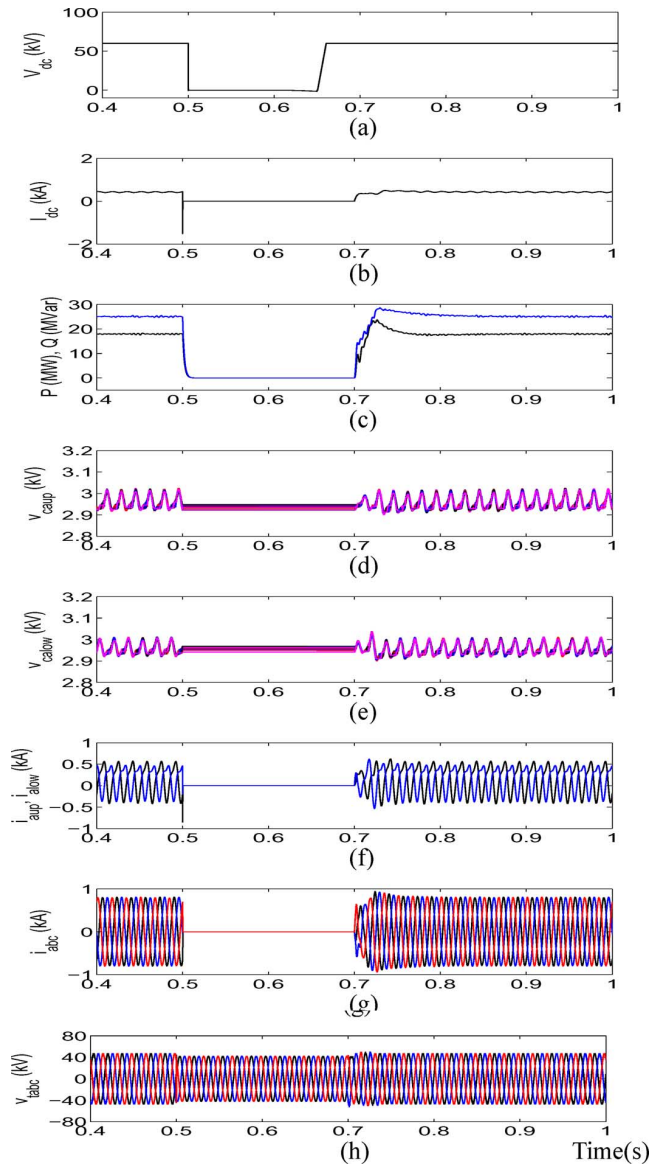

Fig. 11. DC-side short-circuit fault handling of the hybrid-designed MMC-HVDC system (hybrid design V) with the half-bridge and three-level cross-connected SMs: (a) and (b) dc voltage and current, (c) real and reactive power, (d) and (e) SM capacitor voltages of the upper and lower arms of phase-a, (f) phase-a arm currents, and (g) and (h) ac-side currents and voltages.

per arm exist during the fault. Consequently, a higher reverse voltage is generated in the full-bridge MMC-HVDC system to drive the short-circuit current to zero. Due to the same number of SM capacitors in the short-circuit loop during the fault, the hybrid MMC III and V have similar blocking time, as shown in Fig. 12(b) and (c). In addition, the blocking time in the clamp-double MMC-HVDC system is very close to those of the hybrid MMC-HVDC systems since there are 10 series-connected capacitor pairs in each arm of the clamp-double MMC-HVDC system, that is, two SM capacitors connected in parallel in each pair, as shown in Fig. 12(d). However, the hybrid MMC III and V have lower component requirements, compared to the clamp-double MMC–HVDC system.

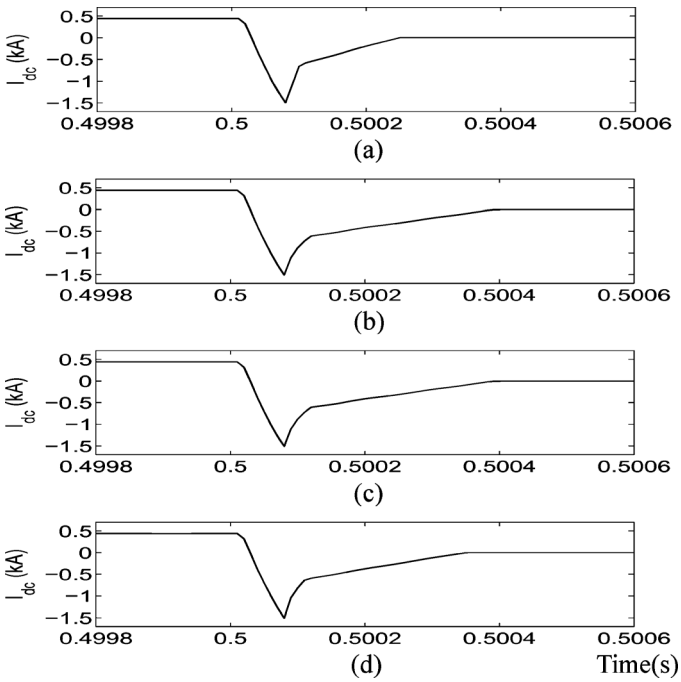

Fig. 12. Zoomed-in portion of the dc-fault current of (a) the full-bridge, (b) the hybrid design III, (c) the hybrid design V, and (d) the clamp-double MMC–HVDC system.

VI. Discussions

Currently, the MMC–HVDC systems are mainly based on the half-bridge SMs due to their low cost and high efficiency compared with the MMC-HVDC system based on any other SM circuit topology. However, the dc-fault-handling capability of the MMC-HVDC system is also a key factor that needs to be considered in the overall design of an MMC-HVDC system. To embed inherent dc-fault-handling capability, the hybrid MMC configurations, based on the combination of the half-bridge SMs (for their reduced cost and high efficiency) with the SM circuits based on the full-bridge, clamp-double, five-level cross-connected, and the proposed unipolar-voltage full-bridge and three-level cross-connected SMs (for their dc-fault-handling capability), are investigated in this paper. The hybrid-designed MMCs make a tradeoff among the dc-fault-handling capability, efficiency, and cost, and full modularity of the HVDC systems. However, due to the following reasons, the hybrid-designed MMCs can be considered as potential and viable solutions:

- Currently, the Si semiconductor devices, the IGBTs, and Si antiparallel diodes are the dominant semiconductor devices for MMC-HVDC systems. However, the development of emerging wide bandgap semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN) power devices can potentially benefit the entire Si application space, including the MMC-HVDC systems, by drastically reducing the power losses and minimizing the cooling systems. It is anticipated that in the future, high-voltage SiC devices will impact the SM circuit configurations. Although compared to the Si devices, the commercially available SiC devices have limited rating values with higher cost, and the semiconductor development and price trends reveal that high-voltage SiC devices will become available with reasonable prices [30].
- In the long run, the long-term operational cost reduction of the MMC-HVDC systems justifies their higher initial costs. The existing and future grid code requirements and the need for continuous uninterruptible power demand will also contribute to MMC design and development.

VII. Conclusion

In this paper, a unipolar-voltage full-bridge and a three-level cross-connected SM circuit topology as well as a hybrid design methodology are proposed to embed the dc-fault-handling capability in the MMC-HVDC systems. The dc-side short-circuit fault of the MMC-HVDC system is analyzed and several MMC-HVDC systems with various SM circuit topologies are evaluated and compared in terms of the dc fault-handling capability, semiconductor power losses, and component requirements. The effectiveness of the proposed hybrid design method for a 21-level MMC-HVDC system under dc fault conditions is evaluated based on simulation studies in the PSCAD/EMTDC environment. The study results demonstrate that the hybrid-designed MMC configurations based on a combination of the half-bridge and the proposed SM circuits are the optimal design among all evaluated systems in terms of dc fault-handling capability, semiconductor power losses, and semiconductor device requirements.

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