Comparison of the Modular Multilevel DC Converter and the Dual-Active Bridge Converter for Power Conversion in HVDC and MVDC Grids

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***Abstract*—It is expected that in the near future the use of high-voltage dc (HVDC) transmission and medium-voltage dc (MVDC) distribution technology will expand. This development is driven by the growing share of electrical power generation by renewable energy sources that are located far from load centers and the increased use of distributed power generators in the distribution grid. Power converters that transfer the electric energy between voltage levels and control the power flow in dc grids will be key components in these systems. The recently presented modular multilevel dc converter (M2DC) and the three-phase dual-active bridge converter (DAB) are benchmarked for this task. Three scenarios are examined: a 15 MW converter for power conversion from an HVDC grid to an MVDC grid of a university campus, a gigawatt converter for feeding the energy from an MVDC collector grid of a wind farm into the HVDC grid, and a converter that acts as a power controller between two HVDC grids with the same nominal voltage level. The operation and degrees of freedom of the M2DC are investigated in detail aiming for an optimal design of this converter. The M2DC and the DAB converter are thoroughly compared for the given scenarios in terms of efficiency, amount of semiconductor devices, and expense on capacitive storage and magnetic components.**

***Index Terms*—Costs, dc collector grid, dc–dc converter, dual-active bridge (DAB) converter, HVDC, modular multilevel dc converter (M2DC), MVDC.**

I. Introduction

DUE to the increasing installation of high-voltage dc (HVDC) transmission lines, dc–dc converters for high-voltage applications will play a decisive role in future energy grids. In this paper, two different converters suitable for high-voltage dc conversion are presented in detail and compared.

In the past years, HVDC transmission has become a mature technology to efficiently transfer large amounts of energy across far distance. In 2012, 40 HVDC point-to-point connections all over Europe with a total length of 13000 km were operational. In the future, the capacity of HVDC connections will be increased further, as for the next 10 years an additional 12600 km are planned [1]. In tomorrow's electricity grid, HVDC systems will not only be applied as point-to-point connections but also as multiterminal dc networks [2]. This requires efficient dc–dc converters to control the power flows in these networks.

Additionally, the amount of renewable energy is still increasing steadily [3]. It has been shown that large renewable energy sources such as windfarms [4], [5] and photovoltaic power plants [6], [7] operate more efficiently when they are connected to a medium-voltage dc (MVDC) collector grid instead of an ac collector grid. With the increasing amount of renewables, power fluctuation in the ac grid is becoming an issue as well [8]. Therefore, storage systems are essential for leveling out the volatility of the supply [9], [10]. These storage systems, e.g., battery energy storage systems [11], [12], electrolyzers for power-to-gas technology [13] or pumped-hydro storages [14] are medium-voltage dc sources or ac sources with variable frequency. Utilizing HVDC links, all these renewable energy sources and storages can be integrated efficiently using a dc conversion from MVDC to HVDC. Moreover, large medium-voltage industrial drives [15]–[17] can be energized more cost effectively through an HVDC link. This requires dc–dc converters to efficiently transform the electric power from the high-voltage to the medium-voltage level.

In such HVDC applications, it is pursued to build power-electronic converters in a modular manner. A modular converter, built up of a high number of smaller modules, is cost effective due to the economies of scale [19], [20]. Maintenance becomes easier, as smaller modules will be replaced in case of failure. The power rating of the system can be simply scaled with the number of modules. In addition, redundancy can be implemented by installing more modules [21]. Topologies like the modular multilevel converter (M2C), where the voltage across each module can be controlled separately, are especially interesting for high-voltage applications. These modular topologies offer easier voltage balancing across the power electronic switches. In contrast, a series connection of IGBTs leads to additional snubber components and more complex gate drive units [22]. Particularly, high-voltage applications motivate the use of modular converter systems.

In 2002, Marquardt and Lesnicar first mentioned the M2C as a promising inverter topology for a high-voltage power conversion between ac and dc voltages [23]–[26]. Since then, there is ongoing research as well as commercialization of the M2C, e.g.,

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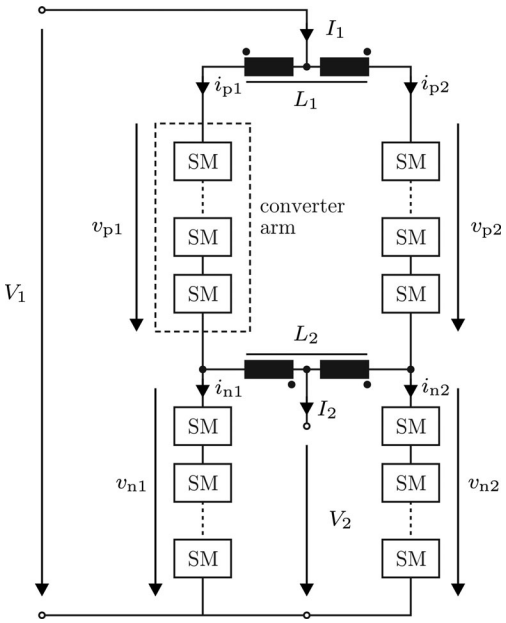

Fig. 1. Unipolar push–pull M2DC [18].

by Siemens and ABB [27]. Current research goals cover linear and model predictive control methods [28]–[30], the proper sizing of the energy storage per arm [31], or sophisticated operation schemes to balance the cell voltages [32] or to further minimize the capacitance per submodule [33], [34].

Two of these M2Cs can be connected back-to-back to achieve a high-voltage dc–dc converter. This configuration proposed by Kenzelmann realizes an efficiency of up to 99% [35], [36]. Furthermore, another dc–dc converter based on the M2C has been proposed, called modular multilevel dc converter (M2DC) [18] (cf. Fig. 1). Further alternative modular dc–dc converter systems for medium voltage applications are proposed in [37]–[41].

In the following, the operation principle and design considerations of the M2DC are introduced in detail. As an alternative, a modular dc–dc converter system is proposed that consists of multiple dual-active bridge units [42]. Subsequently, both converter types are designed for four different scenarios. For all scenarios the expense on magnetic components, capacitive storage, and amount of installed semiconductor switches are compared. Finally, the efficiency and costs of the converter systems are evaluated.

II. Case Studies

In three different scenarios, the modular multilevel dc converter and the dual-active bridge converter are compared in terms of efficiency, amount of semiconductors, and expense on magnetic devices and capacitors.

Scenario A: In *Scenario A*, the MVDC campus grid of RWTH Aachen University [2] is connected to an HVDC link. The MVDC grid is operated at a voltage $V_2 = \pm 5$ kV and the HVDC link with $V_1 = \pm 150$ kV at a nominal power of $P_\mathrm{N} = 15\,\mathrm{MW}$.

Scenario B: It has been shown that the connection of offshore wind farms via MVDC collector grids offer benefits compared to ac collector grids [4], [5]. This motivates the authors to analyze *Scenario B*, in which the converter stations transfer the wind power from the ± 10 kV MVDC collector grid to a ± 150 kV HVDC transmission line. The nominal power is $1.21\,\mathrm{GW}$.

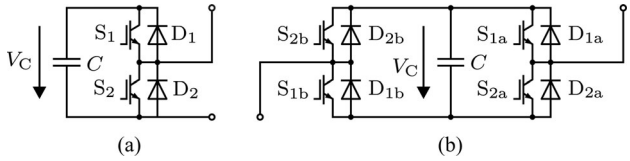

Fig. 2. Submodules (SM) of modular multilevel converters: (a) unipolar submodule, (b) bipolar submodule.

TABLE I
Investigated High-Power dc–dc Conversion Scenarios

	Scenario			
	A	B	C	D
V_1	$\pm 150\,\mathrm{kV}$	$\pm 150\,\mathrm{kV}$	$\pm 150\,\mathrm{kV}$	$\pm 300\,\mathrm{kV}$
V_2	$\pm 5\,\mathrm{kV}$	$\pm 10\,\mathrm{kV}$	$\pm 150\,\mathrm{kV}$	$\pm 150\,\mathrm{kV}$
P_N	$15\,\mathrm{MW}$	$1.21\,\mathrm{GW}$	$1.21\,\mathrm{GW}$	$1.21\,\mathrm{GW}$

Scenario C: In this scenario, a converter that controls the power flow between two interconnected HVDC grids with a nominal voltage of ± 150 kV is investigated. Voltage variations of $\pm 10\%$ must be tolerated, the nominal power is $1.21\,\mathrm{GW}$. Additionally, black-start capability of the grids is required, i.e., the converter must be capable of delivering current if either the primary or the secondary voltage is zero.

Scenario D: Scenario D describes the interconnection of two HVDC grids with different nominal voltages $V_1 = \pm 300\,\mathrm{kV}$ and $V_2 = \pm 150\,\mathrm{kV}$ with a rated power of $1.21\,\mathrm{GW}$. As with Scenario C, the converter system must be capable of black start and must be operable at voltage variations of up to $\pm 10\%$.

The scenarios are summarized in Table I.

III. Modular Multilevel DC Converter

Two different topologies of the *modular multilevel dc converter* (M2DC) were presented in [18], namely the *tuned-filter M2DC* and the *push-pull M2DC*. As the tuned-filter version requires large filter components, the push–pull M2DC, as shown in Fig. 1, is investigated in the following. The converter consists of four converter arms and two coupled inductors. Each arm contains a number of series-connected submodules (SM). The two types of submodules considered in this paper are the unipolar and the bipolar modules depicted in Fig. 2. By appropriate switching states, the unipolar and the bipolar modules can generate the voltages V_C and $\pm V_\mathrm{C}$, respectively, at the output terminals. If an inverter arm has to generate a unipolar voltage, only unidirectional modules are required. However, if an arm is required to generate a positive and a negative voltage, additional bipolar submodules are required.

By combination of two unipolar M2DC (see Fig. 1), a bipolar version as depicted in Fig. 3 can be composed.

A. Fundamental Equations

For a basic understanding of the push–pull M2DC converter, the unipolar version (see Fig. 1) is investigated. Ignoring losses, for given primary and secondary voltages V_1 and V_2 and nominal

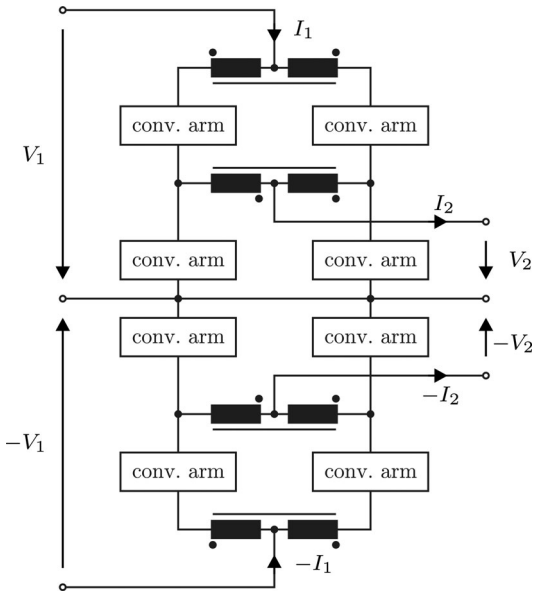

Fig. 3. Bipolar push–pull M2DC.

power P_{N}, the primary and secondary currents are

$$I_1 = \frac{P_{\mathrm{N}}}{V_1}, I_2 = \frac{P_{\mathrm{N}}}{V_2}. \tag{1}$$

In steady-state operation, the average dc component of the voltages of the left and the right branch of the converter $v_{\mathrm{p1}} + v_{\mathrm{n1}}$ and $v_{\mathrm{p2}} + v_{\mathrm{n2}}$, respectively, equals the primary-side voltage V_1. The same applies for the voltage of the lower arms, where the dc component is equal to the secondary-side voltage V_2.

Using power balancing principles, it is clear that the converter has to carry the total input power to the output thereby realizing a voltage drop $V_1 - V_2$. This is accomplished by a so-called secondary power loop that uses frequencies other than 0 Hz to transport energy [18]. The power that has to be transferred by this secondary power loop is

$$P_{\mathrm{sec}} = I_1 \cdot (V_1 - V_2). \tag{2}$$

Assuming a power loop with sinusoidal current and voltage at frequency f_{sec}, the peak value of the current for a given voltage of the secondary power loop $\hat{V}_{\mathrm{sec}}$ is

$$\hat{I}_{\mathrm{sec}} = \frac{P_{\mathrm{sec}}}{\hat{V}_{\mathrm{sec}} \cdot \cos\varphi_{\mathrm{sec}}}. \tag{3}$$

φ_{sec} is the phase shift between voltage and current of the secondary power loop. The lowest current is achieved for $\varphi_{\mathrm{sec}} = 0$.

The current of the secondary power loop is controlled by the voltage across the common-mode inductance of the primary-side coupled inductors L_1. This inductance is chosen sufficiently small, so that the voltage used to control the current of the secondary power loop is neglected for the following equations of the arm voltages.

The arm voltages are

$$v_{\mathrm{p1}}(t) = V_1 - V_2 - v_{\mathrm{sec}}(t), v_{\mathrm{n1}}(t) = V_2 + v_{\mathrm{sec}}(t) \tag{4}$$

$$v_{\mathrm{p2}}(t) = V_1 - V_2 + v_{\mathrm{sec}}(t), v_{\mathrm{n2}}(t) = V_2 - v_{\mathrm{sec}}(t) \tag{5}$$

$$\text{with} \quad v_{\mathrm{sec}}(t) = \hat{V}_{\mathrm{sec}} \sin(2\pi f_{\mathrm{sec}} t) \tag{6}$$

the arm currents are

$$i_{\mathrm{p1}}(t) = \frac{I_1}{2} + i_{\mathrm{sec}}(t), i_{\mathrm{n1}}(t) = \frac{I_1 - I_2}{2} + i_{\mathrm{sec}}(t) \tag{7}$$

$$i_{\mathrm{p2}}(t) = \frac{I_1}{2} - i_{\mathrm{sec}}(t), i_{\mathrm{n2}}(t) = \frac{I_1 - I_2}{2} - i_{\mathrm{sec}}(t) \tag{8}$$

$$\text{with } i_{\mathrm{sec}}(t) = \hat{I}_{\mathrm{sec}} \sin(2\pi f_{\mathrm{sec}} t). \tag{9}$$

B. Number of Submodules

A sufficiently high number of submodules $N_{\mathrm{sm},a}$ are needed in each converter arm a to generate the required arm voltage v_a ranging from a minimum of $V_{a,\min}$ to a maximum of $V_{a,\max}$. In the following, subscript $a \in \{\mathrm{n1}, \mathrm{p1}, \mathrm{n2}, \mathrm{p2}, \mathrm{n}, \mathrm{p}\}$, while n1, p1, n2, p2 refer to specific arms, whereas n and p refer to any lower and upper arms, respectively.

Equations (4) to (6) yield the minimum and maximum voltages of the lower and upper arms

$$V_{\mathrm{n,min}} = V_{2,\min} - \hat{V}_{\mathrm{sec}}, V_{\mathrm{n,max}} = V_{2,\max} + \hat{V}_{\mathrm{sec}} \tag{10}$$

$$V_{\mathrm{p,min}} = V_{1,\min} - V_{\mathrm{n,max}}, V_{\mathrm{p,max}} = V_{1,\max} - V_{\mathrm{n,min}} \tag{11}$$

where $V_{1,\min}, V_{1,\max}, V_{2,\min}$, and $V_{2,\max}$ are the specified limits of the primary and the secondary voltages.

It is assumed in the following that $|V_{a,\max}| > |V_{a,\min}|$. Equations (10) and (11) show that this is fulfilled if $V_{2,\max} > -V_{2,\min}$ and $V_{1,\max} - V_{2,\min} > V_{2,\max} - V_{1,\min}$, which is the case for the given scenarios.

The number of submodules $N_{\mathrm{sm},a}$ of a converter arm a can be estimated by the nominal voltage $V_{\mathrm{C},0}$ of the submodule capacitors and the maximum arm voltage $V_{a,\max}$ that has to be generated during a cycle of the secondary power loop

$$N_{\mathrm{sm},a} = \left\lceil \frac{V_{a,\max}}{V_{\mathrm{C},0}} \cdot k_{\mathrm{s}} \right\rceil \tag{12}$$

where k_{s} is an additional safety factor that acts as a buffer for the control and for the energy variations in the capacitors during operation of the converter. In the following investigations, k_{s} is set to 126%. If redundancy is required, the number of submodules increases further.

Bidirectional modules are needed only if a negative arm voltage is required. The number of required bidirectional submodules is

$$N_{\mathrm{sm,bi},a} = \begin{cases} \left\lceil -\frac{V_{a,\min}}{V_{\mathrm{C},0}} \cdot k_{\mathrm{s}} \right\rceil, & \text{if } V_{a,\min} < 0 \\ 0, & \text{else.} \end{cases} \tag{13}$$

Consequently, the number of unidirectional submodules is

$$N_{\mathrm{sm,uni},a} = N_{\mathrm{sm},a} - N_{\mathrm{sm,bi},a}. \tag{14}$$

C. Submodule Capacitance

The required capacitance in each submodule can be calculated to

$$C_{\mathrm{sm},a} = \frac{\Delta E_a}{N_{\mathrm{sm},a} V_{\mathrm{C},0}^2 \cdot \Delta v_{\mathrm{rel}}} \tag{15}$$

where $N_{\mathrm{sm},a}$ is the number of cells in the according arm, $V_{\mathrm{C},0}$ is the nominal cell voltage, Δv_{rel} is the specified relative voltage

ripple at the capacitors, and ΔE_a is the energy variation over one cycle of the secondary power loop.

This equation is derived from the minimum and maximum energy in the capacitors $\Delta E_{a,\min}$ and $\Delta E_{a,\max}$ and the corresponding minimum and maximum capacitor voltages $V_{\mathrm{C},\min}$ and $V_{\mathrm{C},\max}$:

$$\Delta E_a = \Delta E_{a,\max} - \Delta E_{a,\min} \tag{16}$$

$$= N_{\mathrm{sm},a} \cdot \frac{C_{\mathrm{sm},a}}{2}\left(V_{\mathrm{C},\max}^2 - V_{\mathrm{C},\min}^2\right) \tag{17}$$

$$\text{with } V_{\mathrm{C},\max} = V_{\mathrm{C},0} \cdot \left(1 + \frac{\Delta v_{\mathrm{rel}}}{2}\right) \tag{18}$$

$$\text{and } V_{\mathrm{C},\min} = V_{\mathrm{C},0} \cdot \left(1 - \frac{\Delta v_{\mathrm{rel}}}{2}\right). \tag{19}$$

The energy variation ΔE_a is

$$\Delta E_a = \max_{t\in[t_0,t_0+T[}(E_a(t)) - \min_{t\in[t_0,t_0+T[}(E_a(t)) \tag{20}$$

$$\text{with } T = \frac{1}{f_{\mathrm{sec}}} \tag{21}$$

where

$$E_a(t) = \int_{t_0}^{t_0+t} (v_a(t)\cdot i_a(t))\,\mathrm{d}t + E_{a,0} \tag{22}$$

for a given arm voltage $v_a(t)$, arm current $i_a(t)$, and initial energy $E_{a,0}$.

In the following, Δv_{rel} is set to 20%, corresponding to a voltage ripple of $\pm 10\%$.

D. Semiconductors

The conduction losses are estimated separately for each arm using the characteristics given in the data sheets.

For a given arm voltage and number of submodules, the average number of switches S_1 and S_2 in on-state at a given point in time t is

$$\overline{N}_{\mathrm{S1,on},a}(t) = \frac{v_a(t)}{V_{\mathrm{C},0}} + N_{\mathrm{sm,bi},a} \tag{23}$$

$$\text{and} \quad \overline{N}_{\mathrm{S2,on},a}(t) = N_{\mathrm{HB},a} - \overline{N}_{\mathrm{S1,on},a}(t) \tag{24}$$

respectively, where $N_{\mathrm{HB},a} = 2N_{\mathrm{sm,bi},a} + N_{\mathrm{sm,uni},a}$ is the number of half-bridges in the arm.

Assuming a homogeneous distribution of the losses among all half bridges of a converter arm, the average conduction losses in a single switch and diode of this arm are calculated by weighting the conduction losses with the number of devices in on-state

$$\overline{P}_{\mathrm{cond,S1},a} = \frac{1}{N_{\mathrm{HB},a}} \cdot \frac{1}{T}\int_0^T \big(v_{\mathrm{th}}(i_{a-}(t)) \cdot i_{a-}(t) \cdot \overline{N}_{\mathrm{S1,on},a}(t)\big)\mathrm{d}t \tag{25}$$

$$\overline{P}_{\mathrm{cond,D1},a} = \frac{1}{N_{\mathrm{HB},a}} \cdot \frac{1}{T}\int_0^T \big(v_{\mathrm{f}}(i_{a+}(t)) \cdot i_{a+}(t) \cdot \overline{N}_{\mathrm{S1,on},a}(t)\big)\mathrm{d}t \tag{26}$$

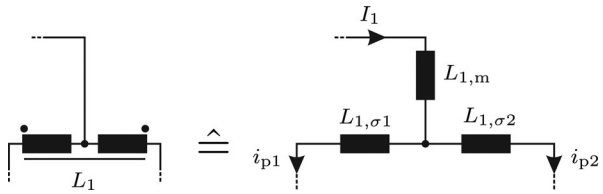

Fig. 4. Push–pull M2DC primary-side inductor.

where $v_{\mathrm{th}}(i)$ represents the on-state characteristic of the switch and $v_{\mathrm{f}}(i)$ the forward voltage of the diode at the current i, with

$$i_{a+} = \begin{cases} i_a, & \text{if } i_a > 0 \\ 0, & \text{else} \end{cases}, \tag{27}$$

$$i_{a-} = \begin{cases} -i_a, & \text{if } i_a < 0 \\ 0, & \text{else} \end{cases}. \tag{28}$$

For the estimation of the switching losses, the characteristics from the data sheets for the turn-on and turn-off energies $E_{\mathrm{S,on}}(v,i)$ and $E_{\mathrm{S,off}}(v,i)$, respectively, and the reverse recovery energy of the diode $E_{\mathrm{D,rr}}(v,i)$ for a given device current i and voltage v is used. The voltage ripple of the capacitors is neglected, that is a constant capacitor voltage $V_{\mathrm{C}} = V_{\mathrm{C},0}$ is assumed, resulting in

$$\overline{P}_{\mathrm{sw,S1},a} = \frac{\overline{f}_{\mathrm{sw},a}}{T}\int_0^T \Big(E_{\mathrm{S,on}}(V_{\mathrm{C},0}, i_{a-}(t)) + E_{\mathrm{S,off}}(V_{\mathrm{C},0}, i_{a-}(t))\Big)\mathrm{d}t \tag{29}$$

$$\text{and} \quad \overline{P}_{\mathrm{sw,D1},a} = \frac{\overline{f}_{\mathrm{sw},a}}{T}\int_0^T E_{\mathrm{D,rr}}(V_{\mathrm{C},0}, i_{a+}(t))\,\mathrm{d}t \tag{30}$$

where $\overline{f}_{\mathrm{sw},a}$ is the average switching frequency of the semiconductors. If the arm is operated in fundamental switching frequency mode (i.e., the output waveform of the arms is a stepwise sine), the average switching frequency of a half bridge is calculated to

$$\overline{f}_{\mathrm{sw},a} = k_{\mathrm{sw}} \cdot f_{\mathrm{sec}} \cdot \frac{2\hat{V}_{\mathrm{sec}}}{N_{\mathrm{HB},a} V_{\mathrm{C},0}} \tag{31}$$

where k_{sw} is an additional safety factor that accounts for additional switching action necessary for balancing of the capacitor voltages. k_{sw} is set to 1.5 for the following investigations.

The losses of S_2 and D_2 can be calculated accordingly.

E. Inductors

Two coupled inductors are used in the M2DC topology: one on the primary side L_1 and one on the secondary side L_2. In the following, the design of these inductors is discussed and the losses are estimated.

The primary-side inductor can be represented as a transformer with its well-known equivalent circuit diagram consisting of the magnetizing inductance $L_{1,\mathrm{m}}$ and the leakage inductances $L_{1,\sigma1}$ and $L_{1,\sigma2}$ (cf. Fig. 4). The primary current I_1 has to flow through the magnetizing inductance and, additionally, a considerably high effective inductance for the currents i_{p1} and

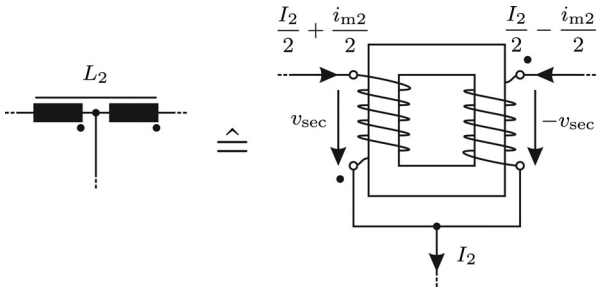

Fig. 5. Push–pull M2DC secondary-side inductor.

$i_{\mathrm{p}2}$, which is the leakage inductance of the transformer, is required. Therefore, it is advantageous to split the coupled inductors into three inductors $L_{1,\mathrm{m}}$, $L_{1,\sigma 1}$, and $L_{1,\sigma 2}$ with equivalent behavior as depicted in Fig. 4. The design of such inductors is straightforward [43].

The secondary-side coupled inductor L_2 is operated similar to an interphase transformer [44]. As illustrated in Fig. 5, the orientation of one winding is inverted. However, as the primary and secondary phase voltages are 180° phase shifted, the voltages imposed on the magnetic core are the same as for an ordinary transformer. These voltages generate the magnetization current $i_{\mathrm{m}2}$. An air gap in the transformer is not needed, as the magnetic fluxes generated by the dc components of the transformer currents cancel out. Therefore, the design of L_2 can be conducted analogously to a standard transformer [43].

The value of $L_{1,\sigma 1} = L_{1,\sigma 2}$ is selected in a way that the voltage required to control the secondary current is less than 5%. Successively, $L_{1,\mathrm{m}}$ is dimensioned such that the primary current ripple is below 5% of the maximum primary current.

To benchmark the performance of the M2DC, the copper and core losses of the inductors are calculated for the given scenarios. The generalized Steinmetz equations (GSE) are used to calculate the core losses assuming a silicon steel material with a thickness of 0.18 mm [45].

Beside the converter losses, the size of the passive components is evaluated. For the magnetic devices, the area product A_{p} is used as a figure of merit to compare the costs of the magnetic components. A_{p} is defined as product of the winding window area A_{w} and the cross section area A_{c} of the magnetic core. It relates to the apparent power of the magnetic components, i.e., to the size of a magnetic core and the size of the copper windings. As it is an important value for the design of transformers and inductors, it is usually given in the data sheets of magnetic cores. To illustrate the area product, a design of a conventional 50 Hz transformer with an apparent power of 630 kVA has been carried out. For the chosen example, the design leads to

$$A_{\mathrm{p}} = A_{\mathrm{w}} \cdot A_{\mathrm{c}} = 0.15\,\mathrm{m}^2 \cdot 0.05\,\mathrm{m}^2 = 0.0075\,\mathrm{m}^4. \quad (32)$$

F. Design Optimization

The rating of the secondary power loop, namely the choice of $\hat{V}_{\mathrm{sec}}$ and f_{sec}, significantly influences the design and the performance of the converter.

According to (3), for a given P_{sec}, a small voltage in the secondary power loop results in high $\hat{I}_{\mathrm{sec}}$. Therefore, a high $\hat{V}_{\mathrm{sec}}$ is favorable concerning the conduction losses in the semiconductors of the submodules. Furthermore, the size of capacitive storage decreases with decreasing $\hat{I}_{\mathrm{sec}}$.

TABLE II
CONVERTER CHARACTERISTICS OF THE M2DC FOR DIFFERENT SCENARIOS

	Scenario			
	A	B	C	D
f_{sec}	600 Hz	300 Hz	1000 Hz	1000 Hz
$\hat{V}_{\mathrm{sec}}$	10 kV	30 kV	50 kV	150 kV
$\hat{I}_{\mathrm{sec}}$	725 A	18 800 kA	2690 A	2020 A
$C_{\mathrm{sm,p}}$	0.68 mF	30.1 mF	0.17 mF	0.48 mF
$C_{\mathrm{sm,n}}$	0.31 mF	36.2 mF	1.25 mF	0.37 mF
$N_{\mathrm{sm,uni,p}}$	101	114	0	104
$N_{\mathrm{sm,bi,p}}$	0	0	136	199
$N_{\mathrm{sm,uni,n}}$	3	7	104	104
$N_{\mathrm{sm,bi,n}}$	7	19	32	95
$N_{\mathrm{par,p}}$	1	7	2	1
$N_{\mathrm{par,n}}$	1	16	1	2
$\overline{f}_{\mathrm{sw,p}}$	89 Hz	118 Hz	276 Hz	448 Hz
$\overline{f}_{\mathrm{sw,n}}$	529 Hz	300 Hz	446 Hz	765 Hz
$L_{1,\mathrm{m}}$	6.00 mH	59 µH	33.4 µH	36.2 µH
$L_{1,\sigma 1}$	1.37 mH	106 µH	244 µH	551 µH

Using solely unidirectional modules, i.e., $N_{\mathrm{sm,bi},a} = 0$ and, consequently, $V_{a,\min} \geq 0$, it can be verified by (10) and (11) that $\hat{V}_{\mathrm{sec}}$ is limited by $\hat{V}_{\mathrm{sec}} < V_2$ and $\hat{V}_{\mathrm{sec}} < (V_1 - V_2)$. A higher $\hat{V}_{\mathrm{sec}}$ can be gained by using bidirectional modules. However, the use of bidirectional modules results in a higher number of semiconductors. Additionally, the number of switches and diodes in the current path that produce losses increases. Consequently, increasing $\hat{V}_{\mathrm{sec}}$ above a certain value reduces the efficiency of the converter.

f_{sec} directly influences the size of the capacitors, magnetic components, and the losses of the semiconductors. From (15) to (22), it can be derived that the required capacitance is inversely proportional to f_{sec}. Furthermore, A_{p} is approximately inversely proportional to f_{sec} [43]. In these terms, it is favorable to choose a high f_{sec}. However, for a sufficiently high $\hat{V}_{\mathrm{sec}}$ many or even all submodules are required to switch during one period of the secondary power loop frequency, resulting in an increased average switching frequency [cf. (31)] and thus increased switching losses. Therefore, for a given design, the switching losses are proportional to f_{sec}.

IV. DESIGN OF THE MODULAR MULTILEVEL DC CONVERTER SYSTEMS

For the given scenarios, the design of an appropriate modular multilevel dc converter is carried out. The characteristics of the converters for all scenarios are summarized in Table II. The nominal cell voltage $V_{C,0}$ is 2 kV for all scenarios.

A. Scenario A: Linkage Between MVDC and HVDC Grids

This scenario exhibits a high conversion ratio at low power. HiPak 5SNA 0650J450300 IGBTs of ABB with a rating of 4500 V and 650 A are used for the upper arms, while StakPak 5SNA 1300K450300 IGBTs of ABB [46] rated for 4500 V and 1300 A are employed in the lower arm. Due to the low current, a parallel connection of IGBTs is not necessary. Hence, the

number of parallel semiconductors $N_{\mathrm{par,p}}$ and $N_{\mathrm{par,n}}$ in the upper and lower arms, respectively, is equal to one.

$\hat{V}_{\mathrm{sec}}$ has been set to 10 kV. Increasing $\hat{V}_{\mathrm{sec}}$ results in higher switching losses and increased losses in the magnetics, whereas a lower $\hat{V}_{\mathrm{sec}}$ would result in a higher secondary power loop current and, hence, would increase the conduction losses. f_{sec} is set to 600 Hz. A lower f_{sec} would result in lower switching losses and improved overall efficiency, however, bigger capacitors would be required.

With the formulas from Section III, the remaining quantities in the according column in Table II are derived.

As the upper arm contains many submodules ($N_{\mathrm{sm,uni,p}} = 101$) and the secondary voltage is low compared to the average voltage $V_1 - V_2$ of the arm, the average switching frequency of the upper arm semiconductors $\overline{f}_{\mathrm{sw,p}} = 89$ Hz is also low. In the submodules of the lower arm almost all half-bridges have to switch during one period of the secondary power loop. Hence, the average switching voltage of the lower arm semiconductors $\overline{f}_{\mathrm{sw,n}} = 529$ Hz is close to f_{sec}.

As the primary current ($I_1 = \frac{P_{\mathrm{N}}}{V_1} = \frac{15\,\mathrm{MW}}{300\,\mathrm{kV}} = 50$ A) and the small secondary power loop current $\hat{I}_{\mathrm{sec}}$ are small, relatively high inductances $L_{1,\mathrm{m}}$ and $L_{1,\sigma 1}$ are required for limiting the voltage ripple.

As will be detailed later, a high conversion ratio in combination with low power rating results in very poor efficiency.

B. Scenario B: Wind Farm Connection

For this system, the choice of $\hat{V}_{\mathrm{sec}} = 30$ kV results in the best efficiency and the lowest total investment costs (derivation of the costs will be covered in Section VIII). $f_{\mathrm{sec}} = 300$ Hz has been chosen for a good tradeoff between efficiency and capacitor size. A high conversion ratio and high transferred power result in a very high current of the secondary power loop $\hat{I}_{\mathrm{sec}}$. Consequently, large submodule capacitances with $C_{\mathrm{sm,p}}$ and $C_{\mathrm{sm,n}}$ exceeding 30 mF and massive paralleling of IGBT modules is necessary. Using StakPak 5SNA 2000K451300 IGBTs of ABB [46] with a rating of 4500 V and 2000 A, $N_{\mathrm{par,p}} = 7$ IGBTs and diodes have to be connected in parallel to handle the current in the submodules of the upper arm, for the lower arm $N_{\mathrm{par,n}} = 16$ parallel devices are required.

C. Scenario C: Grid Interconnection I

In this scenario, the converter should be capable of starting each grid from zero volts, that is $V_{1,\mathrm{min}} = V_{2,\mathrm{min}} = 0$ V according to Section III-B. Therefore, all upper submodules must be bidirectional ($N_{\mathrm{sm,bi,p}} = 136, N_{\mathrm{sm,uni,p}} = 0$). As in Scenario B, StakPak 5SNA 2000K451300 IGBTs are used.

$\hat{V}_{\mathrm{sec}} = 50$ kV gives the lowest cost for the semiconductors. Using a lower $\hat{V}_{\mathrm{sec}}$ would require additional paralleling due to the higher secondary power loop current. Due to the high number of submodules, the frequency of the secondary power loop can be set to $f_{\mathrm{sec}} = 1000$ Hz while the average switching frequencies $\overline{f}_{\mathrm{sw,p}}$ and $\overline{f}_{\mathrm{sw,n}}$ of the upper and lower arms, respectively, are still below 500 Hz. The comparatively high f_{sec} results in capacitors of moderate size ($C_{\mathrm{sm,p}} = 0.17\,\mathrm{mF}, C_{\mathrm{sm,n}} = 1.25\,\mathrm{mF}$).

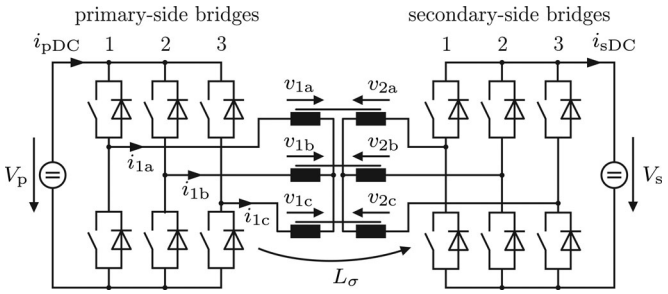

Fig. 6. Schematic of the three-phase dual-active bridge converter.

D. Scenario D: Grid Interconnection II

In this scenario, the M2DC has to connect two dc grids with nominal voltages $V_1 = \pm 300$ kV and $V_2 = \pm 150$ kV. The efficiency is maximal for the selected secondary power loop voltage $\hat{V}_{\mathrm{sec}} = 150$ kV. The required black start capability and voltage variations of $\pm 10\%$ result in the number of submodules as listed in Table II.

To gain reasonable small capacitors and magnetic components, f_{sec} is set to 1000 Hz. This results in $C_{\mathrm{sm,p}} = 0.48\,\mathrm{mF}, C_{\mathrm{sm,n}} = 0.37\,\mathrm{mF}$, and $A_{\mathrm{p}} = 0.312\,\mathrm{m}^4$.

As the current in the upper arm is lower compared to Scenario C, no paralleling of semiconductors is required, thus $N_{\mathrm{par,p}} = 1$. However, paralleling of two IGBTs and diodes is necessary in the lower arm to carry the current in the case of maximum voltage unbalance ($V_1 = \pm 330$ kV, $V_2 = \pm 135$ kV).

V. Dual-Active Bridge Converter

The three-phase dual-active bridge dc–dc converter (DAB) [5], [42], [47]–[52] consists of two full bridge converters and a medium-frequency transformer. The primary bridge converts the dc voltage into a medium-frequency ac voltage that is applied to a transformer providing galvanic isolation. The voltage at the secondary terminals of the transformer is rectified by the secondary bridge. Since two active converters are applied, bidirectional power flow is possible. The topology is depicted in Fig. 6.

A. Principle

Both bridges modulate a six-step voltage at the transformer terminals. The phase shift angle φ between the primary and secondary transformer voltage $v_{\mathrm{p,AC,rms}}$ and $v_{\mathrm{s,AC,rms}}$ results in a voltage difference across the leakage inductance of the transformer and hence in a transferred power P_{DAB}. According to [42], it is

$$P_{\mathrm{DAB}} = \frac{V_{\mathrm{p}}^2}{\omega L_\sigma} \cdot d\varphi \cdot \left(\frac{2}{3} - \frac{\varphi}{2\pi}\right) \tag{33}$$

where V_{p} gives the primary dc voltage, V_{s} the secondary dc voltage, ω the angular frequency of the ac link, L_σ the total leakage inductance of the transformer, and $d = V_{\mathrm{s}}/V_{\mathrm{p}}$ the voltage ratio.

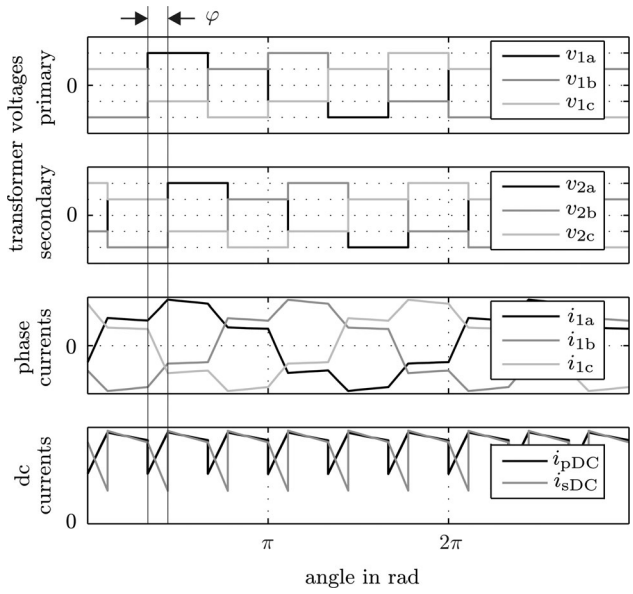

Fig. 7. Characteristic waveforms of the three-phase dual-active bridge converter.

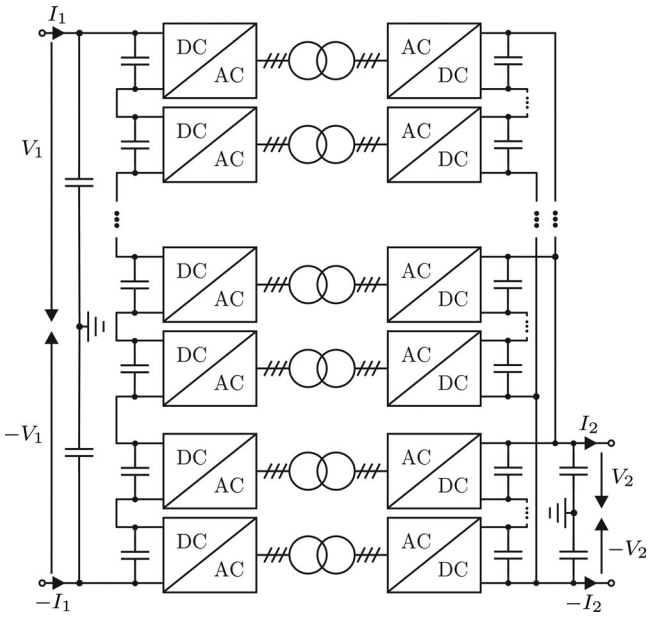

Fig. 8. Dual-active bridge converter system.

The waveforms of voltage and current are exemplary shown in Fig. 7, where φ between the input and output voltages of the first phase is indicated.

Since the ac voltage is modulated by operating the power converters with fundamental frequency switching patterns, the converter can be designed such that all devices are operating in soft-switching mode. Hence, the switching losses $P_{\mathrm{DAB,sw}}$ are lower than the losses in hard-switching converters that use pulse-width modulation strategies such as the M2DC. Furthermore, the transformer's core volume strongly depends on the frequency of the applied voltage; a medium-frequency f_{ac} leads to a significant reduction of the transformer size and weight in comparison with 50 Hz transformer in the same power range, and with the decreased core size also the core losses decrease leading to a higher transformer efficiency. Previous studies have shown that a 1000 Hz transformer, designed for same reliability as standard 50 Hz transformers, has a tenfold increase of power density [45], [48].

B. Control of the Dual-Active Bridge Converter

Fast control of the power P_{DAB} is based on the instantaneous current control presented in [49]. Also, an outer control-loop can be implemented to keep the primary or secondary voltage constant [53].

C. Design of the Dual-Active Bridge Converter

The DAB converter as the smallest unit of the DAB converter system shown in Fig. 8 uses two series-connected 4.5 kV semiconductor devices with a 100-FIT voltage of 2.6 kV to gain the required blocking capability of 5 kV. The reactance of the total leakage inductance $L_\sigma = L_{\sigma,\mathrm{p}} + L_{\sigma,\mathrm{s}}$ limits the maximum power transfer. The maximum leakage inductance

$$L_{\sigma,\max} = \frac{1}{12}\,\frac{V_{\mathrm{p}} V_{\mathrm{s}}}{f_{\mathrm{ac}} P_{\mathrm{DAB}}} \tag{34}$$

can be derived by inserting $\varphi_{\max}$ and the rated power P_{DAB} into (33). When the DAB converter is required to operate with varying input and output voltages, L_σ should be optimized.

The voltage imbalances ($d \neq 1$) increase the apparent power in the transformer. The calculation algorithms presented in [48] estimates the optimum leakage inductance $L_{\sigma,\mathrm{opt}}$ that leads to minimum transformer current in all operation points.

Hence, conduction losses of the semiconductors and of the transformer windings are reduced leading to an improvement of the efficiency.

The minimum required capacitance to limit ΔV operating at nominal power ($\varphi = \varphi_{\mathrm{nom}}$) is estimated with

$$C = \frac{V_{\mathrm{p}}}{6\,\omega^2 L_\sigma \Delta V}\,(2-d)\left(3d\varphi_{\mathrm{nom}}\left(\frac{2}{3} - \frac{\varphi_{\mathrm{nom}}}{2\pi}\right) - \varphi_{\mathrm{nom}}\right)^2. \tag{35}$$

Equation (35) takes the electric charge causing a voltage ripple ΔV across the capacitors of the DAB converter into account. The electric charge can be evaluated by integrating the dc current ripple plotted in Fig. 7.

VI. Design of the Dual-Active Bridge Converter Systems

The dual-active bridge converter system is composed of series and parallel connected DAB converters (cf. Fig. 8). The modular design of each single DAB converter allows the easy adaption of power and voltage rating of the system. If redundancy is required, additional DAB converter can be connected to the system. Note that the amount of primary bridges has to be the same as the amount of secondary bridges, because only the application of two-windings transformers is assumed within the

TABLE III
MEDIUM-FREQUENCY TRANSFORMER DESIGN PARAMETERS

	Scenario A	Scenario B & C	Scenario D
S	0.3 MVA	24.3 MVA	12.2 MVA
J	13 A/mm^2	5 A/mm^2	5 A/mm^2
L_σ	3700 µH	45.5 µH	91 µH
Number of turns	209	9	19
Turn ratio	1:1	1:1	1:1
f_{sw}	1 kHz	1 kHz	1 kHz
V_{core}	0.0146 m^3	0.5638 m^3	0.3838 m^3
A_{p}	0.0002 m^4	0.0022 m^4	0.3101 m^4

scope of this paper. The transformer designs are summarized in Table III. In the following, different application scenarios are presented and discussed.

A. Scenario A: Linkage Between MVDC and HVDC Grids

The linkage between an HVDC transmission line and an urban MVDC distribution grid according to Scenario A requires a converter system with a voltage transformation ratio from $V_1 = \pm 150$ kV to $V_2 = \pm 5$ kV. The high voltage V_1 can be realized by series-connection of 60 bridges. At the secondary side, the series-connection of two bridges is capable to connect the converter system to the 10 kV distribution grid. Consequently, 30 of these series-connected bridges are connected in parallel. Within this paper, a bidirectional power flow between these two grids of 15 MW is assumed. This leads to a secondary current I_2 of 1500 A and a comparatively small primary current I_1 at the high-voltage side of 50 A. Since the power is distributed equally among the DAB converters within the converter system, each semiconductor is loaded with the same current of $i_{\mathrm{p,AC,rms}} = i_{\mathrm{s,AC,rms}} = 36$ A. For the design of a DAB converter system for this application the characteristics of ABB 5SNG 0150P450300 IGBT modules, rated at 4.5 kV and 150 A per device [46], are taken into account. The dc link capacitance connected to each primary and secondary bridges is 1.12 µF limiting ΔV to 500 V (equivalent to a voltage ripple of ±5%). The optimized leakage inductance $L_{\sigma,\mathrm{opt}}$ in this application scenario is 3.7 mH. The DAB converters are operated with $f_{\mathrm{sw}} = 1$ kHz.

B. Scenario B: Wind Farm Connection

The DAB converter system can be used for connecting wind farms to the HVDC transmission line ($V_1 = \pm 150$ kV). Equivalent to the linkage between urban MVDC grids and HVDC lines, also in this scenario 60 bridges are connected in series to achieve the high transmission line voltage. Since the secondary-side voltage ($V_2 = \pm 10$ kV) requires four bridges in series connection, 15 of these series-connected bridges are connected in parallel. The assumed wind farm power of 1.21 GW generates a current $I_2 = 60.5$ kA in the MVDC grid. The HVDC transmission line is loaded with $I_1 = 4.03$ kA. However, the semiconductors need a current capability of $i_{\mathrm{p,AC,rms}} = i_{\mathrm{s,AC,rms}} = 2.85$ kA. The characteristics of ABB 5SHY 55L4500 asymmetrical IGCT and ABB 5SDD 11D2800 diodes [46] are applied for loss calculations. Furthermore, the influence of turn-off resonant snubbers is taken into account for the (soft-switching) loss calculation. Capacitors C_{sn} connected in parallel to the devices significantly reduce turn-off losses by up to 70% when the converter operates at rated power [48]. Within this paper, $C_{\mathrm{sn}} = 3.5$ µF is assumed.

The dc-link capacitance is 90 µF ensuring $\Delta V \leq 500$ V. The optimum leakage inductance $L_{\sigma,\mathrm{opt}}$ is calculated to 45.5 µH. Due to the thermal limits of the semiconductors, the switching frequency is limited to 1 kHz.

C. Scenario C: Grid Interconnection I

In this system, 60 primary bridges and 60 secondary bridges are connected in series to allow the connection of the converter system to ±150 kV (V_1, V_2) and a power flow of 1.21 GW. The current rating of the semiconductor devices is the same as for Scenario B. Hence, also in this scenario ABB 5SHY 55L4500 IGCT modules and ABB 5SDD 11D2800 diodes [46] are applied with $C_{\mathrm{sn}} = 3.5$ µF. In particular, this scenario takes voltage variations of ±10% of the rated voltage into account. This results into an increased dc-link capacitance of 143 µF that is required for a maximum voltage ripple at a single DAB converter of ±5%. The leakage inductances and the switching frequency are equal to the values of Scenario B: $L_{\sigma,\mathrm{opt}} = 45.5$ µH and $f_{\mathrm{sw}} = 1$ kHz.

D. Scenario D: Grid Interconnection II

This scenario investigates the linkage of two HVDC transmission systems operating on different voltage level. The secondary side that operates on ±300 kV requires 120 series-connected secondary bridges to achieve the grid voltage V_2. The primary side connected to $V_1 = \pm 150$ kV can be realized with 60 input bridges in series. Further 60 series-connected primary bridges are connected in parallel to energize all of the 120 output bridges. The power flow is also in this scenario equal to 1.21 GW. Due to the doubled number of DAB, the power rating of each converter is half compared to Scenarios B and C. Hence, the characteristic of ABB 5SHX 26L4520 reverse conducting IGCT [46] are applied with $C_{\mathrm{sn}} = 1$ µF. Due to the insufficient current capability of the monolithic diodes, ABB 5SDF 11H4505 fast recovery diodes [46] have to be applied in parallel to the IGCTs.

Also this scenario takes voltage variations of ±10% of the rated voltage into account. The dc-link capacitance limiting the maximum voltage ripple to ±5% is determined to be 72 µF. The medium-frequency transformer is designed with the optimum leakage inductance of $L_{\sigma,\mathrm{opt}} = 91$ µH for $f_{\mathrm{sw}} = 1$ kHz.

VII. SIMULATION RESULTS AND COMPARISON

In this section, the efficiencies of the two compared dc–dc converter topologies are presented. The results take switching and conduction losses of the semiconductors into account as well as winding and core losses of the transformers and inductors.

The semiconductor losses of the M2DC are estimated with the equations from Section III-D. To verify the operation principle and the analytical calculation of the semiconductor losses of the M2DC, the scenarios have been built up in MATLAB/Simulink and PLECS [54]. In Fig. 9, the simulation of the M2DC of Sce-

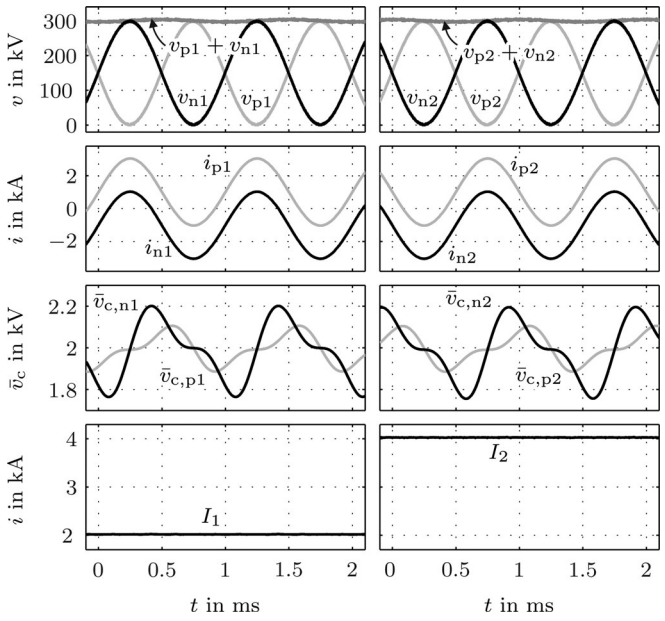

Fig. 9. Voltage and current waveforms of the upper part of the bipolar M2DC of Scenario D at nominal voltages and nominal power.

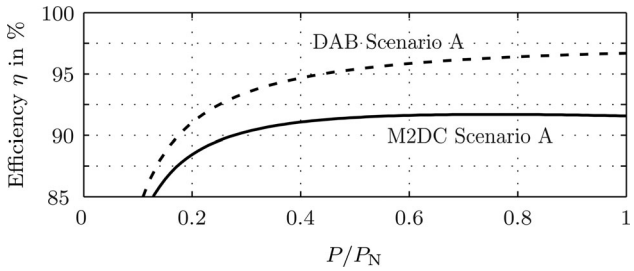

Fig. 10. Efficiency of M2DC and DAB converter for scenario A.

nario D operated at nominal voltage and nominal load is exemplary shown. PI controllers successfully control input current, output current, and the energy balance of the converter arms. The semiconductor losses of the DAB have also been simulated with PLECS.

The improved generalized Steinmetz equation (iGSE) [55] is applied for core loss calculations. The used Steinmetz parameters can be found in [45].

The efficiencies of the converter system designed for *Scenario A* are depicted in Fig. 10.

For the DAB converter, the diagram shows a slightly lower efficiency for partial load compared to the M2DC. However, the DAB converter shows a better performance if the transferred power is above 0.18 pu. At rated power, the efficiency is about 96.7%. The breakdown of the losses is given in Fig. 12(a). It can be seen that the magnetic losses (core and winding losses) decrease with transferred power. Also the influence of the switching losses becomes smaller. The conduction losses do not increase significantly.

The losses of the M2DC are higher at this point leading to a lower efficiency of 92.9%. The high transformation ratios ($V_1 = \pm 150$ kV and $V_2 = \pm 5$ kV) results in a high secondary

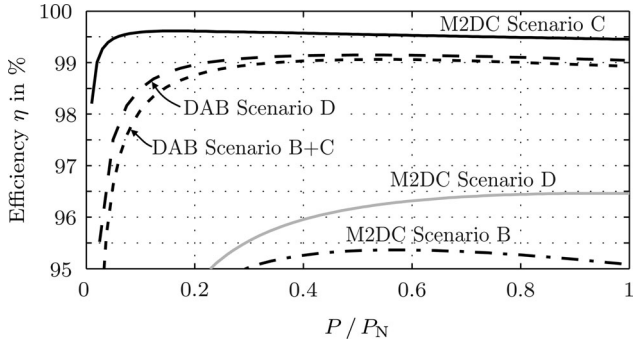

Fig. 11. Efficiency of M2DC and DAB converter for Scenarios B, C, and D.

power loop current, leading to very high conduction losses, as shown in Fig. 13(b). In this scenario, the M2DC can compete with the dual-active bridge only in low partial load conditions concerning the efficiency. However, the number of installed semiconductors is significantly higher for the M2DC, as evident from Table IV.

Scenario B investigates a converter system with a power of 1.21 GW and primary voltage V_1 of ± 150 kV and a secondary voltage V_2 of ± 10 kV. With a value of 98.93% at rated power, the efficiency of the dual-active bridge system (see Fig. 11) is significantly higher compared to Scenario A. The breakdown of losses in Fig. 12(b) shows increasing conduction and switching losses with power, whereas the share of the transformer losses becomes smaller. Due to the high voltage transformation ratio, the M2DC has poor efficiency. Its maximum efficiency of 96.5% can be observed at partial load (206 MW). The efficiency at rated power is only 95.4%. As with Scenario A, the major part of the losses are conduction losses, see Fig. 13(b). Furthermore, the converter exhibits a high amount of semiconductors and a very large secondary-side transformer. It can be stated that the DAB converter system is superior in this application scenario.

As the same bridges are used for the dual-active bridge in *Scenario C*, the components, the efficiencies, and the distribution of the losses is identical to Scenario B. The efficiency of the M2DC designed for this application scenario is significantly better compared to the other scenarios. Concerning the losses, this topology is competitive with the DAB converter system. At rated power and equal voltages at the primary and secondary side, efficiencies exceeding 99.5% can be observed.

At unity conversion ratio $V_1 = V_2$, the current only flows through the upper arms, as $I_1 = I_2$ and $\hat{I}_{\mathrm{sec}} = 0$. Therefore, the efficiency for this operating point is very high. If there is a difference $\Delta V = V_1 - V_2$ between primary and secondary-side voltages, the current of the secondary power loop builds up, resulting in increased losses in the lower submodules and a decreased efficiency. As shown in Fig. 14, the efficiency is also dependent on the sign of ΔV. The efficiency can be improved by dynamical adjustment of $\hat{V}_{\mathrm{sec}}$ dependent on the power that has to be transferred by the secondary power loop, see Fig. 14. By lowering $\hat{V}_{\mathrm{sec}}$, the magnetization losses in the secondary-side coupled inductor L_2 are decreased and the switching frequency of the semiconductors can be reduced. However, the conduction losses increase. For a given transferred power, there exists an

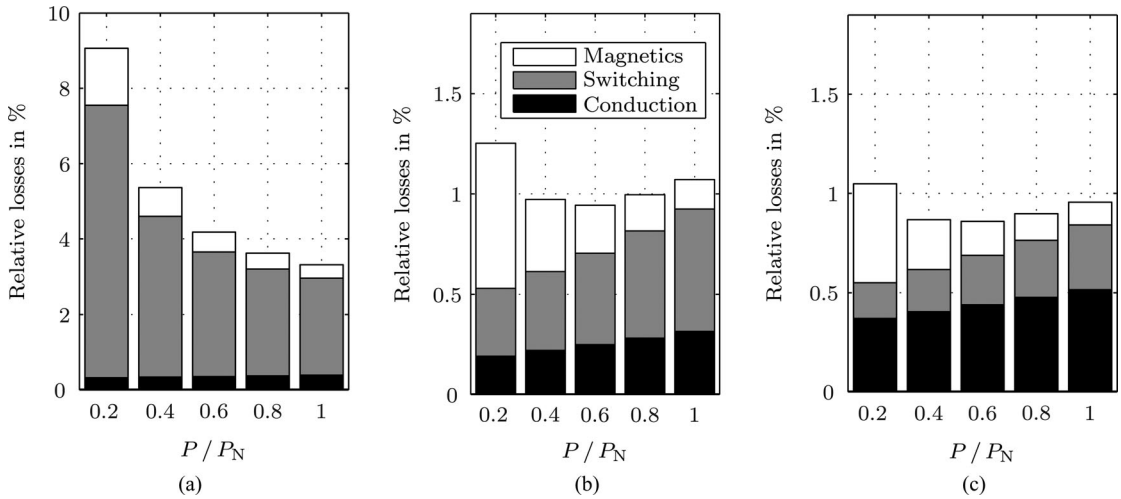

Fig. 12. Losses of the DAB converter system. (a) Scenario A. (b) Scenarios B and C. (c) Scenario D.

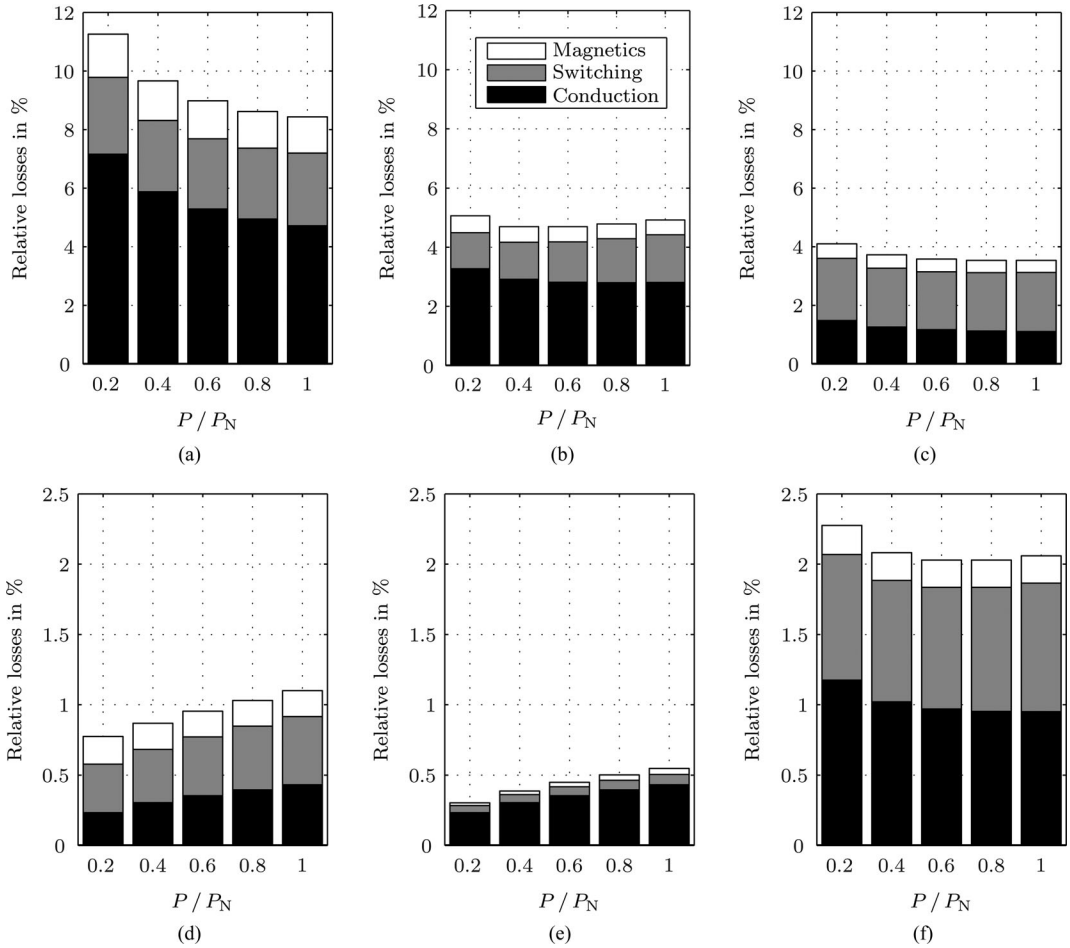

Fig. 13. Losses of the M2DC converter systems. (a) Scenario A. (b) Scenario B. (c) Scenario D. (d) Scenario C with $V_1 = V_2$. (e) Scenario C, $V_1 = V_2$, reduced $\hat{V}_{\mathrm{sec}}$. (f) Scenario C with max. unbalance.

optimum for $\hat{V}_{\mathrm{sec}}$ where the sum of magnetization, switching, and conduction losses is minimal.

Exemplary, Fig. 13(d) and (e) shows the loss distribution at nominal voltages and power for nominal $\hat{V}_{\mathrm{sec}}$ and reduced $\hat{V}_{\mathrm{sec}}$, respectively. As expected, the losses in the magnetic components (magnetization losses of the output transformer) and the switching losses are lower when $\hat{V}_{\mathrm{sec}}$ is reduced.

However, the efficiency decreases if there is a voltage difference between primary and secondary sides, see Figs. 14 and 13(f).

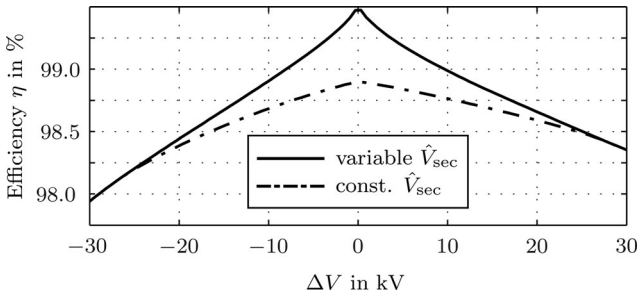

Fig. 14. Efficiency of the M2DC of Scenario C for voltage variations at nominal power.

TABLE IV
COMPARISON OF THE M2DC AND DAB CONVERTER FOR DIFFERENT SCENARIOS

Scenario	Converter	A_{p}	E_{cap}	P_{switch}
A	M2DC	0.06 m^4	582 kJ	3.16 GVA
	DAB	0.012 m^4	1.7 kJ	0.486 GVA
B	M2DC	25.1 m^4	35 MJ	109 GVA
	DAB	0.132 m^4	135 kJ	16.2 GVA
C	M2DC	0.670 m^4	1.55 MJ	51.3 GVA
	DAB	0.132 m^4	215 kJ	16.2 GVA
D	M2DC	1.71 m^4	1.75 MJ	78.5 GVA
	DAB	0.312 m^4	216 kJ	1.43 GVA

TABLE V
SCENARIO C: SYSTEM EFFICIENCY AT NOMINAL LOAD IN CASE OF VOLTAGE VARIATIONS

	V_1/ V_2		
	135 kV / 165 kV	150 kV / 150 kV	165 kV / 135 kV
M2DC	97.94 %	99.45 %	98.35 %
DAB	98.29 %	98.93 %	99.48 %

The efficiencies for a voltage variation of $\pm 10\%$ are given in Table V. If the voltages are balanced, the M2DC shows a significantly better performance than the DAB converter system. At maximum unbalance, the efficiency of the DAB converters system is higher than that of the M2DC. In case of an increase of the voltage at the input of 10% and a 10% lower output voltage, the difference of the efficiency of the two converter topologies is almost 1%.

In *Scenario D*, the DAB converter system is still highly efficient, although twice as many DAB are applied and the rated power is kept constant. The maximum efficiency of 99.15% is obtained at half of the rated power. At full power, the efficiency of 99.05% is only slightly lower. The distribution of the losses are shown in Fig. 12(c). The difference to the loss distribution within Scenarios B and C is caused by the different amount of DAB and by the selected semiconductors. However, the M2DC is not competitive with the DAB converter system due to the high voltage differences and the resulting high secondary power loop current. With a maximum efficiency of 96.46% near nominal power, it shows a very poor performance. The losses are dominated by the switching losses due to the high f_{sec}, see Fig. 13(c). As shown in Table VI, the efficiency slightly increases if the voltage difference between primary and secondary sides becomes smaller. Though, it is even worse if the voltage difference is at its maximum (330 kV / 135 kV). The variation in efficiency of the DAB converter system results from the different semiconductor characteristics. The conduction performance of the IGCTs that carry the current in the primary bridge is more efficient than the conduction performance of the diodes carrying the current in the secondary bridge.

TABLE VI
SCENARIO D: SYSTEM EFFICIENCY AT NOMINAL LOAD IN CASE OF VOLTAGE VARIATIONS

	V_1/ V_2		
	270 kV / 165 kV	300 kV / 150 kV	330 kV / 135 kV
M2DC	97.01 %	96.46 %	95.91 %
DAB	99.29 %	99.04 %	98.62 %

TABLE VII
ECONOMIC EVALUATION

		Investment costs[1] in k€			
Scenario	Converter	Capacitors	Magnetics	Power Electronics	Total
A	M2DC	87.3	58.33	11 100	11 200
	DAB	0.68	249	1700	1950
B	M2DC	5250	18 200	382 000	405 000
	DAB	54	335	56 700	57 100
C	M2DC	232	478	179 000	180 000
	DAB	86	335	56 700	57 100
D	M2DC	263	1250	275 000	276 000
	DAB	86.4	706	49 900	50 700

[1] All figures are rounded to three significant digits.

VIII. ECONOMIC EVALUATION

In this section, based on the analysis of the topologies for the different scenarios, an evaluation of the investment costs is performed. According to current market prices, the costs of the capacitors of the M2DC are approximately 150 €/kJ. In case of the DAB converter in Scenario A, the required dc link capacitance is significantly smaller, leading to higher specific costs of 400 €/kJ. To determine the correlation between the window area product A_{p} and the costs of the magnetic components, the market prices of different 50 Hz transformers between 160 kVA and 3.15 MVA have been evaluated. The cost of the magnetic devices in the different converter systems is approximately

$$K_{\mathrm{mag}} \approx A_{\mathrm{p}} \cdot 723000 \text{€}\ /\mathrm{m}^4 + N_{\mathrm{mag}} \cdot 4000\ \text{€} \tag{36}$$

where N_{mag} is the number of magnetic devices in the system. For the bipolar M2DC $N_{\mathrm{mag}} = 4$ is assumed, whereas for the DAB converter system $N_{\mathrm{mag}} = 60$ and $N_{\mathrm{mag}} = 120$, respectively.

Costs for semiconductors, wiring, cabinets, and control are estimated with 3.50 € per kVA installed switching power P_{switch}.

Table VII gives an overview of the cost distribution for the different converter systems and scenarios, Fig. 15 depicts the specific costs per nominal power. Obviously, the power electronics (including semiconductors, wiring, cabinets, and control) account for the major part of the costs. Although the M2DC topology requires a high number of capacitors, the influence on the total cost is negligible.

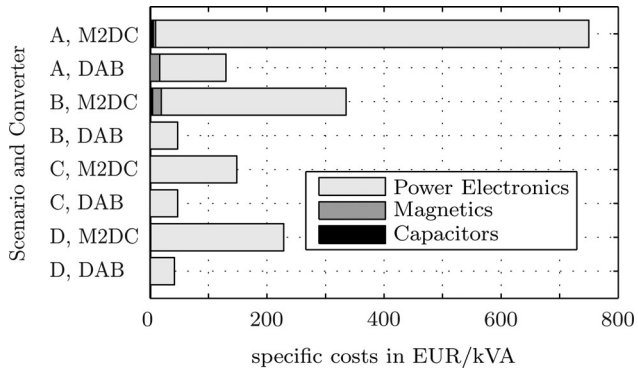

Fig. 15. Specific costs per nominal power P_N of the different converter systems and scenarios.

The cost part of the magnetic components is only noticeable in Scenario A with the DAB and in Scenario B with the M2DC. Consequently, the total costs of the M2DC are mainly determined by the semiconductor cost. The DAB converter system can be designed with a significantly lower amount of power semiconductors. Hence, based on current cost models, the M2DC is more expensive for all of the presented scenarios. In case of Scenario B, the cost for the M2DC is even seven times higher than the cost for the DAB converter system.

IX. Conclusion

The design of a modular multilevel dc converter (M2DC) and a dual-active bridge (DAB) converter system has been carried out for different scenarios employing HVDC and MVDC grids, and the systems have been compared.

The DAB converter system features an efficiency between 98.9% and 99.2% independent of the voltage transformation ratio.

In general, the M2DC requires a much higher amount of semiconductors. Consequently, compared to a converter system based on DAB converters, the investment costs for an M2DC converter system are at least by a factor of three higher. If the frequency of the secondary power loop can be increased to 1 kHz, the M2DC requires a similar amount of magnetic components compared to the soft-switching DAB converter system.

It has been shown that the M2DC is not suitable for high voltage ratios, because in this case the circulating current in the converter becomes high, which results in a poor efficiency of less than 95.5%. Furthermore, the amount of required semiconductors is immense. If primary and secondary voltages differ only by a few percent and galvanic isolation of primary and secondary sides is not required, then the M2DC is the superior topology. In this case, the maximum efficiency exceeds 99.5%.

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