Fault Detection and Interruption in an Earthed HVDC Grid Using ROCOV and Hybrid DC Breakers

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***Abstract*—Different HVDC grid types and the respective protection options are discussed. An earthed bipole HVDC grid was modeled in PSCAD, and using simulation results, the necessity of di/dt limiting inductors to contain the rise of fault currents within the capacity of current hybrid dc breakers is demonstrated. The impact of different inductor sizes on current rise was studied. A fault detection and localization scheme using the rate of change of voltage measured at the line side of the di/dt limiting reactors is proposed. The protection system was modeled and tested under different fault types and locations. The results show that the proposed method of HVDC grid protection is feasible using the current hybrid dc breaker technology. A systematic procedure for setting the necessary protection threshold values is also demonstrated.**

***Index Terms*—DC line protection, di/dt limiting inductor, fault detection with ROCOV, high-voltage direct–current (HVDC) grid, hybrid dc breaker, voltage-source converter (VSC) HVDC.**

I. Introduction

HIGH-VOLTAGE direct-current (HVDC) transmission has been used in power systems around the world, mostly as a point-to-point power delivery system. HVDC technology enables economic power delivery across long distances, is controllable, and does not suffer from excessive charging that ac cables experience when used for underground or submarine transmission systems [1]. HVDC grids are now being considered as a way to interconnect offshore wind resources, avoid overhead lines and add redundancy, flexibility, and efficiency to a widespread power delivery system [1], [2].

While the line-commutated converter (LCC) technology dominates the point-to-point HVDC schemes, the voltage-source converters (VSCs) are the preferred technology for HVDC grids. The main advantage of VSC technology is the ability to transport power in either direction without reversing polarity, which is essential in HVDC grids. The ability to operate in a weak ac system, reactive power flexibility, and a small physical footprint are the other advantages. Newer multilevel VSCs offer additional advantages over two-level VSCs in terms of lower harmonics and switching transients [3].

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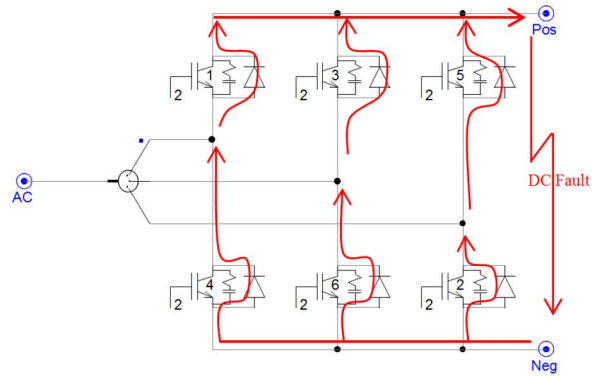

Fig. 1. IGBT-based two-level VSC showing freewheeling diodes which allow a fault current path from ac system to faults on the dc system.

However, VSCs have some inherent weaknesses in the way they respond to dc line faults. In order to ensure proper operation, each insulated-gate bipolar transistor (IGBT) in a VSC needs to be provided with an antiparallel freewheeling diode. During a dc side short circuit, these diodes provide a path for fault currents as illustrated in Fig. 1 for a basic two-level VSC. A fault on the dc side of the converter appears as a three-phase fault on the ac side. A bipolar converter based on typical half-bridge IGBT valves is unable to block this fault current [3].

The path of steady-state currents for a single-pole-to-ground fault depends on the grid configuration. An HVDC grid can have either a monopole or bipole structure and could operate with an earth return or a metallic return. Various possible configurations and earthing options are analyzed in [2]. The bipolar structure with metallic return is most likely to be the HVDC grid configuration that meets operational, reliability, flexibility, extensibility, and environmental criteria. The type of earthing, location, and number of earthing points affect the single-pole-to-ground fault current paths and the protection scheme [2]. Unearthed HVDC grids have the distinct advantage of having no steady-state fault current for single-pole-to-ground faults [2], [4], [5]; however, the cost of equipment would rise due to higher insulation requirements. Pole-to-pole faults still result in a fault current path similar to that of earthed grids. Multiple earthing of an HVDC grid could result in steady-state stray currents that lead to ground potentials and dc currents in nearby pipelines and ac lines [2] and, therefore, may not be acceptable. Thus, in this study, a bipolar HVDC grid with a metallic return and a single earthing point, which is the most likely configuration in a practical HVDC grid, is considered. The fault current paths for a single-pole-to-ground fault in such a grid are shown in Fig. 2.

An approach for fault current interruption with breakers in series with di/dt limiting inductors at the ends of each line segment will be discussed in this paper. These inductors are shown in Fig. 2.

In order to harness the benefits of networking, dc line faults need to be detected, located, and cleared with a minimum interruption to the healthy part of the HVDC grid. This requires appropriately positioned circuit interruption devices. The cost and limitations of dc breakers are major barriers for the development of HVDC grids and need to be considered in designing grids and protection methodologies [5]. Although there are a few studies that discuss the protection of HVDC grids [6]–[9], it remains a major challenge. This paper reviews the state of the art of dc circuit breakers (CBs) and identifies protection system goals. It then proposes: 1) a method to locate the faulted line elements using a local measurement within a very short time; 2) a strategy to select protection settings; and 3) a method to size the di/dt limiting series inductors to enable protection discrimination while meeting the limitations of the dc CBs.

II. Fault Response Options and Protection Goals

This section analyzes the pros and cons of different options for responding to dc line faults, discusses dc CB capabilities, and details the proposed protection system goals.

A. Fault Response Options for Earthed HVDC Grids

There are four basic options on how to respond to a dc fault in a VSC-based earthed grid as follows.

1) Trip the ac CBs at each converter on the grid. The grid would be disconnected and the fault current would be interrupted. The faulted segment could be located based on fault current direction. While this could be done with a central controller and communications, methods based on local measurements with no need for communications exist [10]. Mechanical switches could open the faulted segment and the grid could be restarted [11]. This would be adequate for small dc grids but would not be acceptable for very large systems.
2) Use full-bridge modular multilevel converter (MMC) VSC converters. Full-bridge MMC converters can block fault currents [12], [3]. Upon detection of a fault, all of the converters could block the current. The fault current would be interrupted, mechanical switches could isolate the fault, and grid operation could be restarted. This new technology would be faster than the ac breakers but would still interrupt power flow across the entire grid for a period of time.
3) DC breakers could be placed in series with each converter [13]. During a line fault, the dc breakers would block fault currents from all converters. The lines and cables would discharge into the fault, mechanical switches would be opened to clear the faulted segment, and then the dc breakers would close and restore the grid.
4) Use dc CBs in a manner similar to how ac CBs are used. Breakers would be placed at the ends of all line or cable segments. Fault currents would be interrupted and the faulted segment isolated without interrupting the operation of any of the converters or discharging the remote sections of the grid.

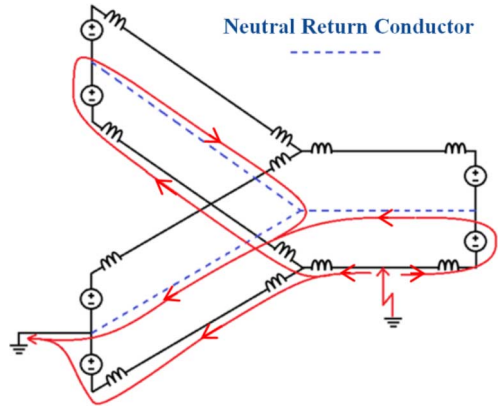

Fig. 2. Steady-state fault current path in a single-point earthed bipole grid.

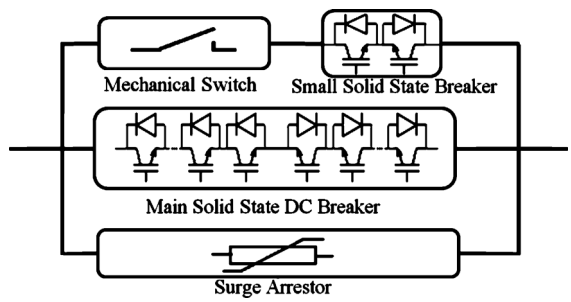

Fig. 3. Hybrid dc breaker [17].

It is the fourth approach that will be further discussed in this paper.

B. DC Breakers

It is possible to interrupt dc current with a passive commutation circuit. Such a circuit would include a resonant LC circuit in parallel with a mechanical switch in parallel with a surge arrester. Upon opening the switch, an arc would occur in parallel with the LC circuit and a current resonance would be induced [14]. Since this resonating current crosses zero, the arc would be extinguished. The arrester would absorb the energy stored in the LC circuit and the nearby lines. The operating time would be in the range of tens of milliseconds. This type of breaker is not fast enough for a large-scale HVDC grid [15]. If the clearing time is too long, the entire grid will discharge into the fault [16]. A prolonged dc fault will draw fault currents from the ac system at each converter.

Another option is to use a solid-state device, such as an IGBT, as a dc breaker. The advantage of this is that it is very fast. The operating time could be in the microseconds range. The disadvantage of this approach is that solid-state devices are expensive and lossy. With many of these breakers in the system, significant power losses would occur. Large cooling systems would be necessary. These losses would be a major factor in designing the protection scheme and the layout of the grid itself [5].

The dc breaker approach that will be considered in this paper is the hybrid dc breaker. A hybrid dc breaker consists of a small solid-state breaker in series with a very fast mechanical switch in parallel with a large solid-state breaker in parallel with a surge arrester, as shown in Fig. 3.

ABB has tested devices with an operating time of 2 ms, a maximum breaking current of 9 kA, and a transient voltage capability of more than 1.5 p.u. during current breaking. They have proposed a device with a maximum breaking current of 16 kA [17]. Alstom Grid is developing and testing a similar device [18].

During normal operation, the current is going through the small solid-state breaker; hence, the losses are low. When a fault is detected, the small solid-state device blocks and commutates the fault current into the main solid-state device. At this time, the fast mechanical switch is triggered. Opening this switch may take approximately 2 ms. Once this switch is opened, the large solid-state device blocks and the current is commutated into the surge arrester, which limits the voltage across the large solid-state device to a tolerable limit.

C. Proposed Protection System Goals

The goal of the earthed bipole dc grid protection system discussed in this paper is similar to that of an ac protection system: to detect line faults and remove the faulted sections from the grid. Any individual line or cable fault should be detected and isolated without the loss of any other element in the system (other than radially connected converters).

The fault detection and location addressed in this paper consist only of determining whether the fault is on the immediate line or cable segment for the purpose of initiating breaker action. There are established methods of determining exact fault locations on point-to-point dc lines for repair purposes [19]. A lot of good work has been done in adapting these methods to more complicated grid configurations [20]. This paper will only address the challenge of determining which segment the fault is on.

While it is important to clear the faulted section before the remaining dc and ac networks are adversely affected, in this case, the main requirement for fast fault detection is the hybrid dc breaker operating time and maximum breaking current. The peak fault currents of practical HVDC grids are likely to be much higher than the breaking capacity of the proposed dc breakers. If the fault current exceeds the maximum breaking current, then it is necessary to break the fault current before it exceeds this level while it is still in the rising phase.

Fig. 4 shows a fault detection scenario. Assuming that we have fast dc breakers at both ends of each line segment, a fault at location F1 should result in breaker B41 and B14 opening to isolate the faulted element. A fault F2 or F3 on the adjacent segments should not result in tripping of B41 or B14. The protective relays controlling the breakers at B41 and B14 need to quickly identify the faulted line segment. For bus fault F4, B14 should trip but the relay at B41 needs to determine that the fault is beyond breaker B14 and, therefore, does not trigger a trip.

Both of these challenges (detection/location of faulted segment and current rise limitation) can be achieved with properly designed di/dt limiting inductors in series with the breakers at the ends of each line segment.

III. DC Grid Test Circuit

A three-converter test grid was modeled in PSCAD to study the proposed protection concept. A grid this small could be shut down in the event of a fault; however, it is useful for testing and demonstrating the protection principals that could be applied to a larger dc grid. The larger the grid, in terms of total power transfer and numbers of converters, the less feasible it is to shut down all converters in the event of a fault.

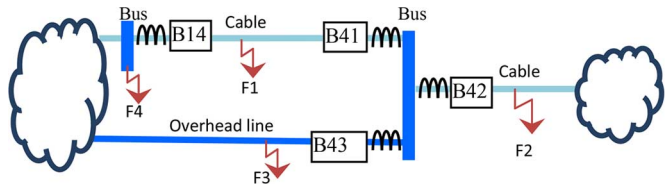

Fig. 4. Fault detection scenario.

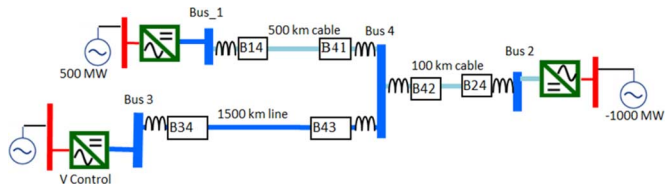

Fig. 5. Three-converter test system.

The single-line diagram (SLD) in Fig. 5 shows the layout of the test grid. Three converter buses are connected to a central bus in a radial Y configuration. All converters are connected to equivalent sources on the ac side.

The ac-to-dc converter valve and controller models used in this study were provided by the Manitoba HVDC Research Center [21]. They are generic multilevel VSC models. Two of the converters are in power-control mode and one is in voltage-control mode. This is simpler than a realistic grid steady-state power and voltage-control scheme but is adequate for simulating the operation of protection functions.

IV. Fault Detection

Considering the fast current rise in a highly capacitive dc grid, it is important to detect the fault and determine which breakers to trip as soon as possible.

It is not possible to rely on differential protection schemes that would require communication from one end of the line to the other. The propagation speed on transmission lines and cables varies according to the line or cable parameters. The fault wave on the cable models used for these simulations traveled at 110 km/ms. Waiting for a fault transient propagating at such a speed to reach the far end of the line and for a message to return (at a slightly faster fiber-optic speed) in order to determine if a fault is on the immediate line section, would add too much delay. It is necessary for each breaker to measure the fault transient and determine very quickly whether the fault is on the segment of the line that it is protecting.

Although overcurrent is a good indicator of a fault, waiting for the current to exceed a threshold before signaling a trip, especially when it is necessary to discriminate against the faults in the next line segment, adds a significant delay. The dc breakers may not be able to tolerate such a delay. Another possibility is to use the rate of change of current (ROCOC) seen by the breaker.

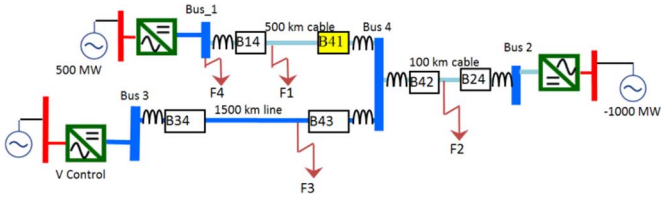

Fig. 6. Fault detection scenario.

Since each breaker necessarily has an inductor in series with it to limit the rate of rise of fault current, ROCOC is given by

$$\frac{di(t)}{dt} = \frac{v_{\text{bus}}(t) - v_{\text{line}}(t)}{L} \tag{1}$$

where L is the inductance of the di/dt limiting inductor and v_{bus} and v_{line} are the voltages on the bus and line side of the inductor. The voltage on the bus side of a di/dt limiting inductor v_{bus} remains relatively constant for the first millisecond after the fault transient arrives at the breaker. As a result, the ROCOC seen by the breaker is, in fact, approximately proportional to the voltage change on the line side of the inductor and would be of no more use in determining fault location than the line-side voltage measurement itself.

The solution proposed in this paper is to use the measured rate of change of voltage (ROCOV) at the line side of the di/dt limiting inductor to detect and locate the faults. The rationality of the protection scheme can be explained considering the three dc grid faults F1, F2, and F3 shown in Fig. 6. All line/cable sections are provided with dc breakers (and associated di/dt limiting inductors of 100 mH) at both ends so that each segment can be isolated if a fault occurs in the segment.

Consider the voltage measurement taken at the line side of breaker B41 for different pole-to-ground faults, shown in Fig. 7. All faults are initiated at t = 2.5 s. The first five plots are for fault F1, with each plot corresponding to a different fault location on cable C1–4 (0, 100, 200, 300, 400, and 500 km from Bus 4). It can be observed for the aforementioned faults that the slope (ROCOV) of the voltage wavefront is quite steep even up to 500 km down cable C1–4.

The 6th plot in Fig. 7 is the line-side voltage measured at B41 for fault F4, a pole-to-ground fault at Bus 1. This is a remote bus fault. This fault is separated from the fault at 500 km down the line by one di/dt limiting inductor. The last two plots are voltages measured at B41 (line side) for fault F2 on cable C1–2 and fault F3 on line L3–4, at locations very close to Bus 4. However, faults F2 and F3 are each separated from breaker B41 by two di/dt limiting inductors. These series inductors act as a low-pass filter and smooth out the voltage transient that is seen by B41 for faults F2, F3, and F4. Thus, the faults across the inductor from B41, on L3–4 and C2–4, and faults at the far end of the line across an inductor, produce a much more gradual voltage change as seen on the line side of B41.

Thus, the change in ROCOV (from almost zero steady state) can be used to detect the occurrence of a fault very quickly (within microseconds of the fault wave arriving at the di/dt limiting inductor). The difference in ROCOV magnitudes can be used to differentiate the faults on the protected line from the

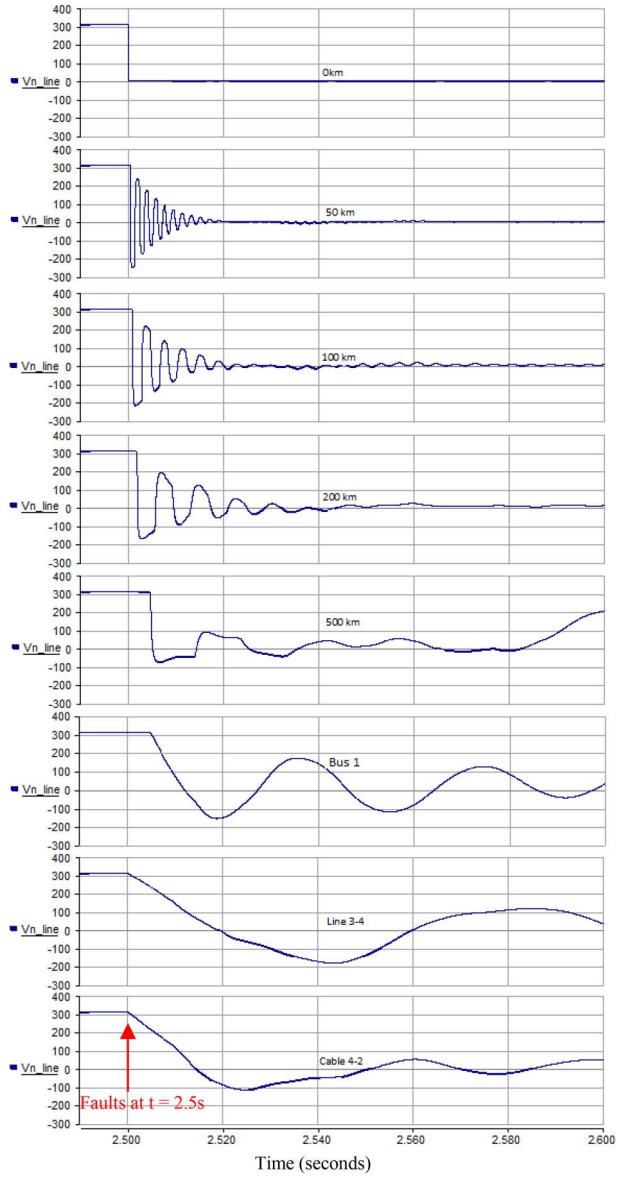

Fig. 7. Line-side negative pole voltage magnitude measured at B41 for different fault locations, faults at time = 2.5 s.

faults on adjacent lines or bus faults. It can be seen that the ROCOV does decrease as the fault moves farther away from the measurement point. The maximum ROCOV observed for each fault scenario is tabulated in Table I. In PSCAD simulations, these ROCOV values were calculated by taking the differential of the measured voltage and scaling it to kilovolts per millisecond.

When these values are plotted logarithmically (see Fig. 8), it can be seen that there is still a considerable margin between the ROCOV values observed for faults in the protected zone and those observed for faults on the adjacent zones.

Similarly, the ROCOV values observed at breaker B43 are shown in Fig. 9. In this case, the protected zone is an overhead line (L3–4) and, therefore, attenuation of ROCOV is smaller even for lengths up to 1500 km. The ROCOV observed for faults not on the segment protected by B43 (F1 and F2) is higher compared to corresponding values observed at B41, due to the

TABLE I
MAXIMUM MEASURED ROCOV AT B41 FOR DIFFERENT FAULT LOCATIONS WITH 100-mH INDUCTORS

Fault Location		ROCOV (kV/ms)
Element	Distance from Bus 4	
Cable 1-4	0	30651
	50	23874
	100	12603
	200	5490
	300	3017
	400	1872
	500	1264
Cable 2-4	0	31.85
Line 3-4	0	22.25

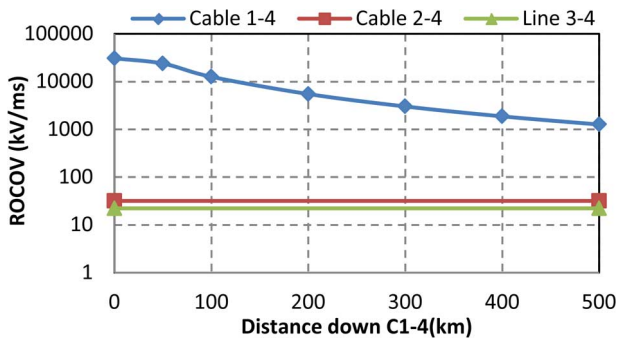

Fig. 8. ROCOV measured at B41 for faults down C1–4 toward bus 1 and for faults across the inductors on C2–4 and on L3–4.

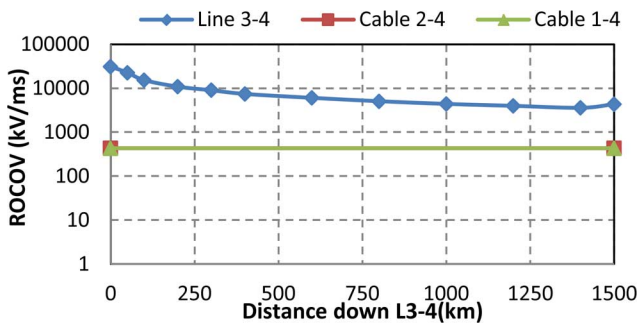

Fig. 9. ROCOV measured at B43 for faults down L3–4 toward bus 3 and for faults across the inductors on C2–4 and on C1–4

lower capacitance of the overhead line. However, for the distances studied, there is still enough margin between the ROCOV from the faults on the protected segment L3–4 and the faults on the other segments to distinguish them. This demonstrates the concept that with di/dt limiting inductors in place effectively delineating each protection zone, it is relatively easy for a relay measuring ROCOV to determine whether the fault is on the protected zone or in a remote zone.

V. IMPLEMENTATION OF ROCOV-BASED DETECTION

Setting ROCOV threshold values is a matter of determining the minimum possible ROCOV measured for a fault within the primary protection zone, for which the breaker should trip, and the maximum possible ROCOV for any fault for which the breaker should not trip.

Table II shows the results of such an effort for the three-converter test grid, with 100-mH di/dt limiting inductors. The lowest ROCOV on the protected segment can be compared to the highest possible ROCOV for a fault on a remote line or cable segment or bus or the subsequent clearing thereof. In some situations, clearing of a remote line or bus fault can create an ROCOV that is larger than that observed during the occurrence of the fault. Assuming that there is sufficient margin, an ROCOV threshold setting can be selected within the stated margin. If there is not a sufficient margin, inductor values can be revisited to further reduce the ROCOV from remote faults.

Setting these threshold values is an iterative process because the ROCOV due to clearing of faults can depend on the clearing time. The ROCOV from faults can be determined initially, and based on them, a set of preliminary threshold values can be chosen. The protection scheme can then be modeled, and the fault clearing can be simulated to determine the maximum ROCOV after fault clearing. The preliminary ROCOV thresholds can then be updated if necessary. The breakers on an overhead line and a cable feeding into the same fault will see different effects when the fault is cleared. The presence of the cable feed-in will decrease the ROCOV seen by the breaker during the fault, but will increase it during the clearing of the fault. For a fault on C1–4 (F1), breaker B43 will see a higher maximum ROCOV when breaker B41 clears the fault than during the fault. For the same fault, breaker B42 will see a higher ROCOV during the initial fault than it will during the breaker clearing.

Bus faults should result in all breakers at that bus tripping. A local bus fault can be identified by comparing the voltages on both sides of all di/dt limiting inductors at the bus. When the following condition is met for all branches at the bus, a bus fault has occurred and all local breakers should trip:

$$\frac{dv_{\text{bus}}}{dt} > \frac{dv_{\text{line}}}{dt}. \tag{2}$$

Alternatively, differential current protection could also be used to identify bus faults.

ROCOV for a fault on the bus at the far end of a line or cable ideally should not trip a breaker but this is not critical as a remote bus fault will result in tripping the breaker at the other end of the line segment so the line segment is out of service. The results in Table II and Fig. 7 show that there is still a significant margin between the ROCOV for faults on remote buses and faults on protected line segments.

VI. FAULT DI/DT LIMITING INDUCTORS

A fault on a dc grid can result in a rapid discharge of the energy in the dc capacitors of VSCs and dc cable capacitances into the fault. Thus, the current can ramp up very quickly. Any given dc CB technology will have a maximum current that it can interrupt and a maximum operating time. In the case of the hybrid dc breaker discussed in Section II-B, this operating time is mainly determined by the time necessary to open the fast mechanical disconnecter. In order to limit the current rise during the breaker operating time to a value below the maximum interruptible current of the breaker, it is necessary to place di/dt limiting inductors in series with the dc CBs as shown in Fig. 10.

TABLE II
RESULTS OF THE STUDY TO SET ROCOV-BASED PROTECTION THRESHOLDS FOR THE TEST GRID WITH 100-mH di/dt LIMITING INDUCTORS

Breaker Name	Lowest ROCOV on Protected Segment (kV/ms)	Remote Bus Fault ROCOV (kV/ms)	Remote Fault	Highest ROCOV due to Fault on RemoteSegment (kV/ms)	Highest ROCOV after Remote Fault Clearing (kV/ms)	ROCOV Trip Setting Selected (kV/ms)
B41	1264	47.38	Cable 2-4	19.11	20.35	800
			Line 3-4	19	19	
B42	12662	103.74	Line 3-4	19	19	5000
			Cable 1-4	19	19	
B43	4331	602.15	Cable 2-4	432	525.9	2000
			Cable 1-4	432	756	
B14	1256	45.46	Cable 2-4	23.48	23.48	800
			Line 3-4	16.83	16.83	
B24	12672	94.8	Line 3-4	38.76	38.76	5000
			Cable 1-4	32	32	
B34	4110	786	Cable 2-4	274	274	2000
			Cable 1-4	276	360	

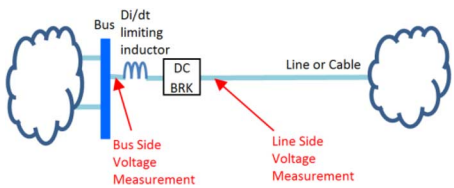

Fig. 10. Bus, inductor, breaker, and measurements.

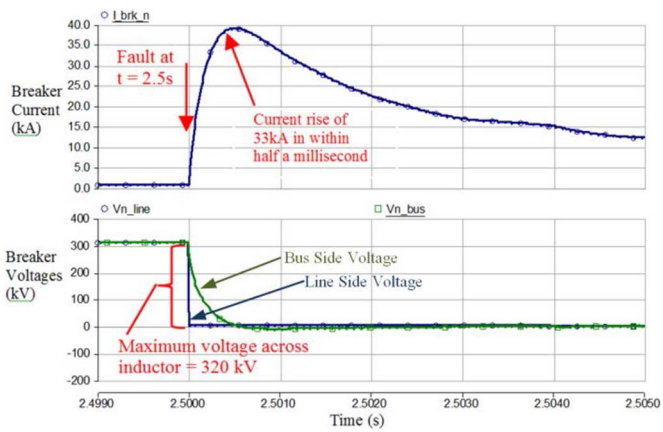

Fig. 11. Negative pole current and voltage on both line and bus side of the 1-mH di/dt limiting inductor at B14 for a fault at the terminal on the line side of the inductor at time = 2.5 s.

Fig. 11 shows simulated negative pole current and the voltages on both line and bus side of the di/dt limiting inductor at B14 for a negative pole-to-ground fault on the line side of the inductor. The fault was initiated at t = 2.5 s. For this simulation, small 1-mH inductors were placed in series with all of the CBs in the three-converter HVDC grid.

With only 1-mH di/dt limiting inductors, the current quickly rises beyond the interrupting capability of the dc breaker. When the size of inductors is increased to 100 mH, the current rises much more slowly, as seen in Fig. 12. It can be observed that the voltage on the faulted side of the breaker immediately drops

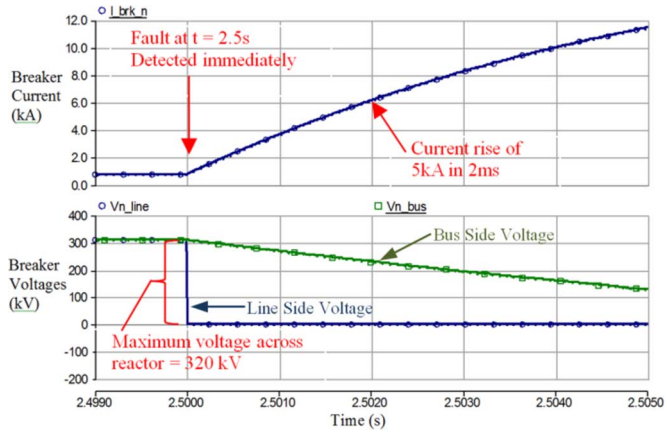

Fig. 12. Negative pole current and voltage on both line and bus side of the 100-mH di/dt limiting inductor at B14 for a terminal fault at time = 2.5 s.

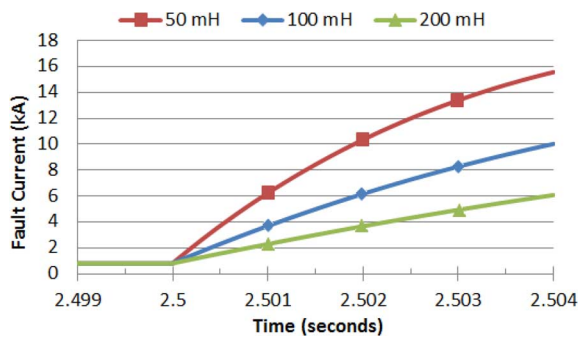

Fig. 13. Current rise at B14 with different inductor values for a terminal fault at time = 2.5 s.

to zero. The voltage on the bus side of the breaker decreases as the fault current ramps up.

The fault current increase given by (1) is directly proportional to the voltage difference across the inductor. If the di/dt limiting inductor is 100 mH, for a ±320-kV grid operating at 1.1-p.u. voltage, the maximum theoretical rate of rise of current due to a fault at the line terminals is

$$\frac{di}{dt} = \frac{\Delta V}{L} = \frac{350\ \text{kV}}{0.1\ \text{H}} = 3.5\frac{\text{kA}}{\text{ms}}. \tag{3}$$

In a case with more capacitance on the bus side of the breaker, possibly due to a larger converter or due to more cables feeding into the bus, the bus-side voltage would remain high and the current rate of rise would not taper down as quickly. Thus, the current rises almost linearly as shown in Fig. 12. In Fig. 13, the rise in current through breaker B14 for a fault on the line terminal close to the breaker is shown for different inductor values.

When choosing di/dt limiting inductor values, the breaker operating time and maximum interruptible current should be taken into account, and the inductor should be sized accordingly. It should also be noted that the terminal fault shown here does not provide the highest possible rate of rise of current. The plot in Fig. 14 shows the same quantities shown in Fig. 12, when the fault (at t = 2.5 s) is moved 150 km down the cable C1–4.

It can be observed in Fig. 14 that in this case the fault transient takes approximately 1.4 ms to reach breaker B14 and that when it arrives, the voltage on the line side of the breaker drops below

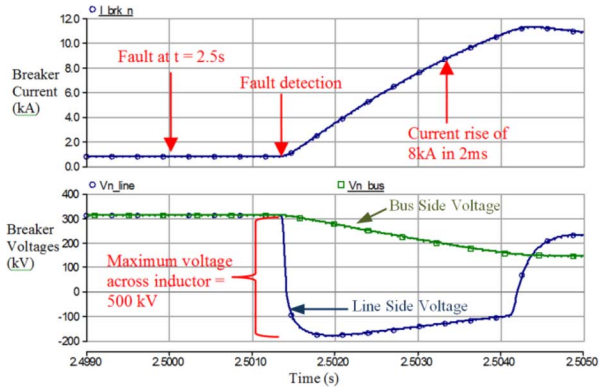

Fig. 14. Negative pole current and voltage on both line and bus side of the 100-mH di/dt limiting inductor at B14 for the fault 150 km down the cable at time = 2.5 s.

zero. The reflection of the incoming wave by the inductor results in a "voltage doubling" at the line side of the inductor terminal. Due to an increased voltage difference across the inductor (almost double), the rate of rise of current is much faster in this case. This phenomenon is most significant in cables.

The fastest rate of rise in current through a dc breaker occurs when the fault is located at a distance equal to the distance that the fault transient travels in half the operating time of the breaker. In the cable modeled in the test system, the fault transient travels at approximately 110 km/ms. For a breaker having an operating time $T_{\text{op}} = 2$ ms, this critical fault location *Dcrit* that provides the highest current that the breaker needs to be able to interrupt can be obtained as

$$Dcrit = \frac{\text{velocity} * \text{Top}}{2} = 110\frac{\text{km}}{\text{ms}} * \frac{2\text{ ms}}{2} = 110\text{ km}. \quad (4)$$

If the fault current exceeds the capability of the breaker at its maximum operating time for a fault at *Dcrit*, the size of the inductor should be adjusted to limit the rise in current. The plots in Fig. 15 show the current rise for the fault 150 km down the cable when different inductor values are considered.

The worst case current should be determined for a given breaker by simulating pole-to-pole faults at the highest possible operating voltage with the highest possible prefault operating current and the maximum breaker operating time. There should be some margin between this value and the interrupting limit of the breaker.

The worst fault location for the overhead lines modeled in this study is at the terminals of the breaker. The overhead lines have much less capacitance. The transient travel speed is significantly higher and the traveling wave has much lower current due to the lower capacitance to inductance ratio.

VII. Breaker Operation Simulations

The hybrid dc breaker was modeled as an ideal breaker with a time delay of 2 ms in parallel with a surge arrester. Upon detection of a fault on the segment protected by the breaker, the delay timer starts. When the breaker operates, the surge arrester conducts according to its voltage and current characteristics. While this does not model the exact mechanism of a hybrid HVDC breaker, it adequately represents the effects of such a breaker.

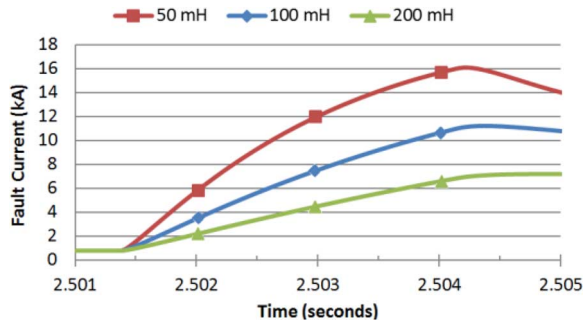

Fig. 15. Current rise at B14 with different inductor values for a fault 150 km down the cable at time = 2.5 s.

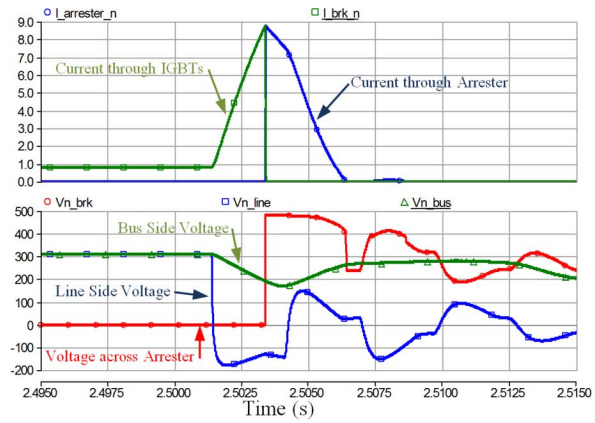

Fig. 16. Fault clearing with 100-mH inductors, the fault 150 km from B14 at t = 2.5 s, with the arrester set to 243 kV.

TABLE III
Arrester Energy With Different Arrester Ratings

Energy Absorbed by Arrester at B14 for a given Arrester Rating (LG fault 150 km down cable, 100 mH inductors)	
Arrester Rating	Arrester Energy (kJ)
320 kV	6386
243 kV	6659
184 kV	8309

The change in steady-state impedance when commutating current from the mechanical switch to the large IGBT is negligible and was not modeled.

Fig. 16 shows currents and voltages during the operation of breaker B14 for a fault 150 km down the cable C1–4 toward bus 4. The di/dt limiting inductor value is 100 mH. The surge arrester was modeled using the ac surge arrester model available in PSCAD with a default V-I characteristic and with a voltage rating of 243 kV. It should be noted that Vn_brk (red curve) is the voltage across the surge arrester [not the voltage difference between the line terminal (blue curve) and the bus (green curve)].

The arrester needs to be selected such that it will keep the voltage across the breaker below the maximum voltage that the main breaker IGBT string can handle. A lower arrester voltage rating will result in more energy being absorbed by the arrester during breaker operation. This can be seen in Table III.

The current through the breaker (green with square markers) can be seen ramping up after the fault transient reaches the

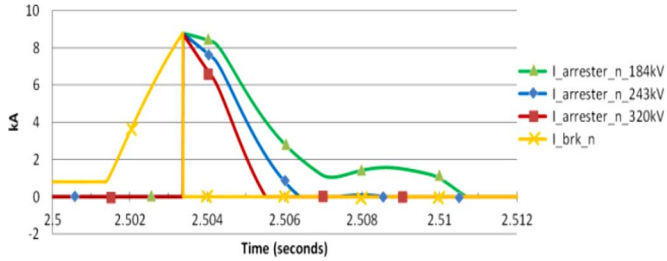

Fig. 17. Breaker currents with different arrester ratings (fault at t = 2.5 s, 150 km down cable).

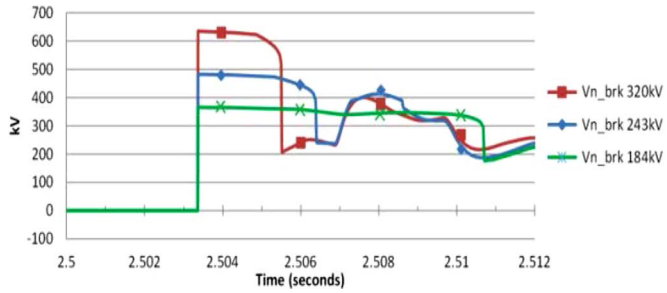

Fig. 18. Breaker voltages with different arrester ratings (fault at t = 2.5s, 150 km down cable).

breaker. After 2 ms, the breaker opens and the arrester conducts to clamp the voltage to approximately 1.5 p.u. of the line rating. Arrester current is shown by the blue curve with circle markers. The current through the arrester tapers down to 0 kA and does not cause any additional problems for the dc grid. The lower plot in Fig. 16 shows the voltages at the bus side of the breaker (green with triangles) and the line side of the breaker (blue with squares) and the voltage across the breaker (red with circles).

The impact of different arrester voltage ratings can be seen in Figs. 17 and 18. A higher voltage rating will require higher voltage withstand capability on the solid-state component of the hybrid breaker but will result in quicker current extinguishment.

VIII. Conclusion

It is feasible to use a hybrid HVDC breaker to protect a dc grid from pole-to-ground and pole-to-pole line and cable faults. Use of series di/dt limiting inductors is necessary to limit the fault currents to a level below the rated breaking current within the time required for the breaker to operate.

The highest rate of rise of fault current for a cable fault will occur for a pole-to-pole fault at a critical distance away from the cable terminal. This critical distance is equal to half of the distance travelled by the fault transient during the breaker operating time.

Since the grid is effectively segmented for the high-frequency fault transients by the di/dt limiting inductors, the ROCOV measured at the line side of the inductor can be used to quickly determine if there is a fault on the immediate line segment. There is no time delay involved since the measurements are local. Thus, the proposed protection scheme is a simple yet very practical method for protecting HVDC grids from line and bus faults, without interrupting the entire grid.

When setting ROCOV thresholds for discriminating against bus faults and faults on the adjacent lines, it is necessary to determine the minimum ROCOV that the breaker will see for a fault on the protected segment and the maximum ROCOV that the breaker will see for a fault that is not on the protected segment.

Backup protections have not been discussed in this paper due to space limitations. Backup protection could include communication-based protection or ac-side breaker operation. These topics will be addressed in future research and subsequent publications.

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