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Masterthesis

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EVOLUTION OF HEAT FLOW PREDICTION MODELS FOR FPGA DEVICES

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ABBREVIATIONS

ADC	Analog-to-Digital Converter
CLB	Configurable Logic Block
CLK	Clock Signal
CMOS	Complementary Metal-Oxide-Semiconductor
FF	Flip-Flop
FPGA	Field-Programmable Gate Array
IR	Infrared
LUT	Lookup Table
RO	Ring Oscillator
VLSI	Very Large Scale Integration

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INTRODUCTION

On today's integrated circuits there is a considerable potential of generating high temperatures, due to shrinking devices sizes and increasing frequencies. By the reason that the carrier mobility is degraded and the interconnect resistivity increases, the devices could suffer from decreased execution speed and longer interconnect delays [**?**]. Those soft (timing) errors can eventually lead to the premature occurrence of hard errors [**?**]. Finally local hot spots and higher temperature gradients can lead to a shortened device life time and a shrinked package reliability.

Especially FPGAs can generate local temperature hot spots and alarmingly high temperatures are reached within a small area. For many cases the accurate temperature monitoring and prediction is becoming increasingly important.

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HEAT MODELING OF INTEGRATED DEVICES

2.1 heat models using physical device models

2.1.1 Other Methods

RC- Networks

2.2 extension to on-line evolution of heat models

2.3 temperature measurement methods

2.3.1 Built-In Temperature Sensor

The most common way to measure temperatures on a Very Large Scale Integration (VLSI) chip is to implement a temperature sensor in Complementary Metal-Oxide-Semiconductor (CMOS). As stated in [**?**] the most effective way to achieve this goal is by using vertical bipolar transistors. This approach exploits the fact that the base-emitter voltage V_{be} of a bipolar transistor decreases approximately by $2\,mV°C$ and hence almost linearly with the temperature. Furthermore, the difference between two measured base-emitter voltages δV_{be} is almost linearly proportional to the absolute temperature T_{abs} (ptat) and can be expressed as depicted in Equation 2.1.

$$V_{ptat}(T_{abs}) = \frac{kT}{q} \cdot \ln(p) \tag{2.1}$$

The parameters for Equation **??** are the following:

- Boltzman's constant, $k = 1.38 \times 10^{-23}$
- Temperature in Kelvin, T[° K]
- Charge on an electron in coulomb, $q = 1.6 \times 10^{-19}$ C
- Emission current density ratio p

This temperature sensor achieves an accuracy of $\pm 1°C$, by calibrating V_{be} at room temperature [**?**].

Also in modern FPGAs there is a trend of providing a pre-calibrated thermal diode, which are also provided at CMOS level. These devices can for example be found at the Virtex-5 FPGA by Xilinx, where the proportionality between the voltage and die temperature is as well exploited. Xilinx specifies this correlation with Equation 2.2 [**?**].

$$V_{ptat}(T_{abs}) = 10 \cdot \frac{kT_{abs}}{q} \cdot \ln(10) \tag{2.2}$$

Note that the emission current density ratio is here set to $p = 10$. Hence, temperature coefficient of V_{ptat} is $-2\,mV/°C$.

Since the thermal diode is pre-calibrated, the temperature can be derived as depicted in Equation 2.3. To allow the further calculation it is mandatory to convert V_{ptat}, given as analog signal, into a digital number. The thermal diode on a Virtex-5 FPGA digitizes V_{abs} with the help of the built-in Analog-to-Digital Converter (ADC) and produces the 10 bit output ADC code $V_A DC$. The resulting maximum-measurement error of this on-chip temperature sensor is specified with °C [**?**].

$$T[°C] = \frac{V_{ADC} \times 503.957}{1024} - 273.15 \tag{2.3}$$

2.3.2 Infrared Cameras

Besides the above-named on-chip solutions of measuring the internal temperature, there is also the possibility to use Infrared (IR) cameras.

For instance, [?] measured a spatial thermal gradient of 2°C over 10 mm on a Xilinx Virtex II FPGA using an infrared camera. Furthermore [?].

Shortcomings of this approach are that one always needs direct view on the chip's silicon layer [?]. I.e. no heat sink, package or other material, where the emission cannot be determined. Besides the high price for these devices, IR cameras cannot be employed in actual working conditions, because of their size [?].

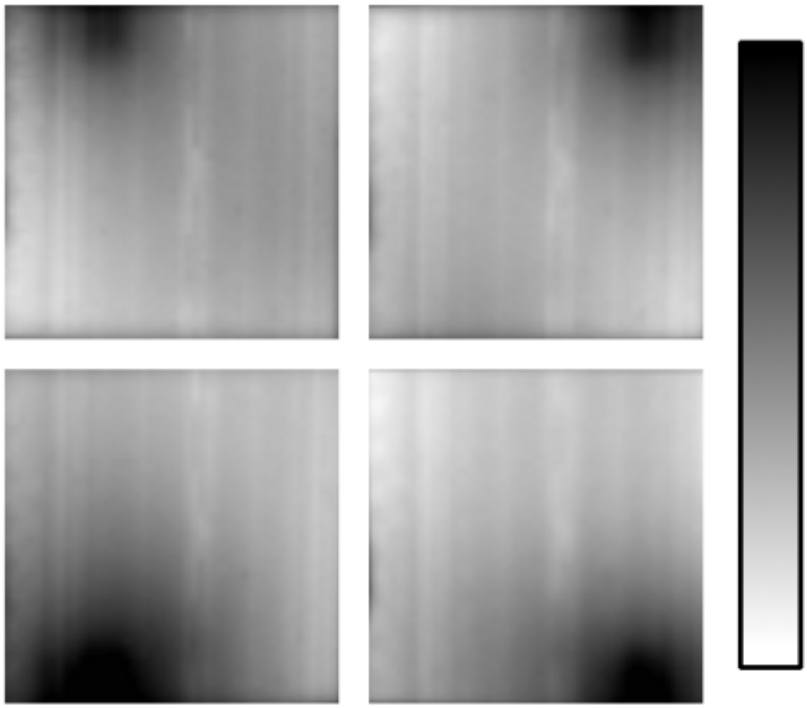

Figure 1: Four infrared images of the FPGA with temperatures from 80°C (white) to 95°C (black) cf. [?]

2.3.3 Ring Oscillators

Nowadays, a widely spread technique to measure the internal on-chip temperatures of FPGA-based systems are based on Ring Oscillators (ROs). These devices are composed of an odd number of inverters, which are connected in a chain. The endmost inverter's output is fed back to the first inverter. Figure 2 depicts such a basic RO. This leads to a device without a stable condition, causing each inverter's output to oscillate, i. e. the output Q toggles between 0 and 1 and maximum speed with frequency f_{osc}.

A longer inverter chain leads to a lower frequency and in addition to less power consumption [?]. It is because of the fact that the RO's frequency f_{osc} is inversely proportinal to the on-chip temperature [?], that ROs can be used to measure the temperature on any location on the FPGA. The output frequency f_{osc} is dependant on the curcuit's delay. Furthermore, it is also known that ROs can be used in order to measure delay, leakage and dynamic power [?].

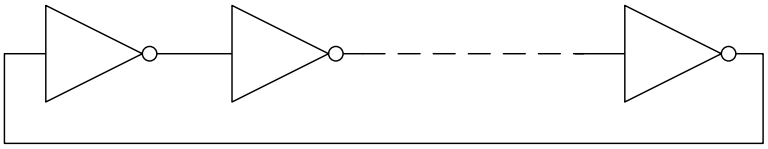

Figure 2: A basic Ring Oscillator, consisting of an odd number of inverters

Methodology

Measuring the internal on-chip temperature necessarily requires knowledge about the frequency f_{osc} of the RO. In order to estimate the frequency, several approaches [?, ?, ?, ?] make use of ROs combined with a capture counter. The counter, as depicted in Figure 3, is clocked with a system Clock Signal (CLK) and by the oscillating output Q of the RO. Q′ toggles at the speed of Q and is sampled by CLK. Put simply, the capture counter samples the number S of oscillations at the signal Q′ with the frequency clk. Afterwards the sampled number of oscillations can be derived to f_{osc}.

However, there are also differences in implementing the RO-based temperature sensor. These variable parameters are: number of inverters, system routing, length of measurement period t_m and the possible use of latches between the inverters. The use of latches was proposed in order to minimize the impact of routing [?]. For FPGAs designs, it is advisable to use latches instead of the additional wiring between the inverters.

The benefits of designing on an FPGA are the reconfigurability. This possible due to the Configurable Logic Blocks (CLBs) of which the FPGA is composed. The CLB however comprises slices, which contain Lookup Tables (LUTs) and Flip-Flops (FFs). Hence,

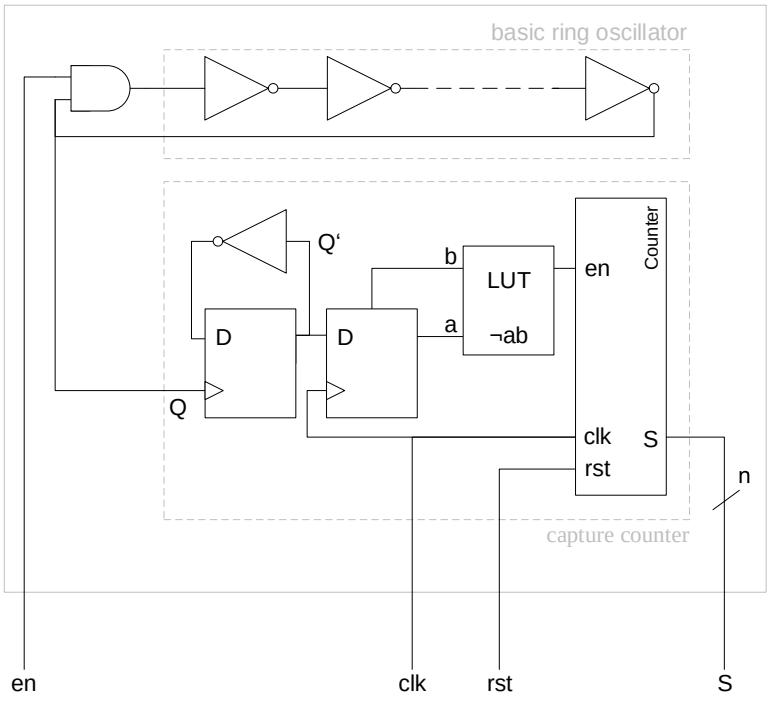

Figure 3: Simplified schematic of a temperature sensor with capture counter cf. [?]

by using LUTs for the RO's inverters, the FFs can be used as latches without significant additional wiring.

In contrast to previous approaches, which used seven [?] or eleven inverters [?, ?] and no latches, a high-performance RO-based temperature sensor comprises 23 inverters and 24 latches [?]. The quality of the RO is derived by sensor resolution and sensor noise/deviation. In addition to the utilization, the optimal measurement period t_m should not exceed the maximum length of 2^{16} clock cycles, which is 655 µs, when the counter samples with 100 MHz. For longer measurement periods, there is a risk of self-heating, since ROs may lead to considerable temperature gradients [?].

As previously pointed out, the optimal measurement with the proposed temperature sensor includes the following steps [?]:

- Enable RO with 23 inverters and 24 latches
- Wait $2^{12} - 2^{16}$ clock cycles so that the RO can gain a constant frequency

- Sample Q′ for t_m clock cycles
- Disable the RO
- Read out the counter value S.

Calibration Methods

Given the sensor count S of RO-based temperature sensors, it is not possible to predict a function that maps S to a temperature T. Instead, the sensors need to be calibrated with an pre-calibrated device, such as the built-in thermal diode, a temperature-controlled oven or an IR camera. While the device is heated up and cooled down afterwards, S is counted and the temperature is read in regular time intervals. For each sensor placed on the chip the linear mapping function is then determined by partial regression [**?**, **?**].

The following approaches request for a temporal temperature gradients equally distributed on the chip. Section 2.4 will give an overview of most common and useful methods for heating up the sensors, e.g. the RO-based temperature sensors.

As proposed in [**?**] the sensors were calibrated by an iron-constantan (Fe-CuNi) thermocouple which is placed in the center of the package exactly measure the on-chip temperature T.

Section 2.3.2 already illustrated that IR cameras are able to exactly measure the on-chip temperature T [**?**], provided that the camera is pointing directly on the silicon and the emission value is known. Additionally of course, they can be used for calibrating the RO-based temperature sensors with high accuracy.

Another way to calibrate the sensors is to make use of the built-in thermal diode, which was presented in Section 2.3.1.

VCC and temperature proportionally ! [**?**]

2.3.4 Discussion on Accuracy

table? - +4°C diode (where? no hot spot detection) - ROTS (calibrated with +4°C acc and where?!) - IR Cam (expensive, no usage in field, silicon view, knowledge about emission)

2.4 temperature generation methods

As said earlier RO temperature sensors have to be calibrated before use. For example, this can be done by There are several approaches[**?**, **?**, **?**]

Several approaches are using a temperature-controlled oven in order to heat up the chip [**?**, **?**, **?**]. Either the sensors are calibrated by surrounding temperature or

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ONLINE EVOLUTION OF HEAT MODELS

- Methodology
  - Definition of Heat Model
  - Measurement modes and Accuracy
- Learning and Optimizing Algorithms
  - Methodology of used Algorithms

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EXPERIMENTS AND EVALUATION

- Experiments on RC-network
- Results for several Learning Algorithms
- Discussion of Convergence
- Discussion of Accuracy
- Discussion of On-Line Suitability
- Discussion of Embedded Implementation

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CONCLUSION

In this thesis I have presented crazy shit!

A

APPENDIX

The implementation of the temperature measurement system and all other files can be found on the appended CD. The folder structure is as follows.

EIDESSTATTLICHE ERKLÄRUNG

Hiermit versichere ich, die vorliegende Diplomarbeit ohne Hilfe Dritter und nur mit den angegebenen Quellen und Hilfsmitteln angefertigt zu haben. Alle Stellen, die aus den Quellen entnommen wurden, sind als solche kenntlich gemacht worden. Diese Arbeit hat in gleicher oder ähnlicher Form noch keiner Prüfungsbehörde vorgelegen.

Paderborn, February 20, 2015

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