Evolution of Heat Flow Prediction Models for FPGA Devices

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November 12, 2014

1 Introduction for Heat Monitoring and Prediction for VLSI Devices

On today's integrated circuits there is a considerable potential of generating high temperatures, due to shrinking devices and increasing frequencies. Especially FPGAs can generate local hotspots and alarmingly high temperature increases with only a rather small resource utilization. For many cases the accurate temperature monitoring and prediction is becoming increasingly important. Many FPGAs, like the Xilinx Virtex-5 or Virtex-6, provide the opportunity to measure the thermal effects of a circuit with the help of a built-in temperature sensor. As [5] pointed out, the outputs of the System Monitor, offered by Xilinx FPGAs, may be inaccurate. Hence [2] proposed a grid of several thermal sensors, consisting of ring oscillators and counters, rather than the single temperature diode. This approach uses the built-in temperature sensor in order to calibrate its sensors, as the correlation between measured temperatures and sensor frequencies is almost linear. Beside the temperature sensor grid, the system also contains heat-generating circuits. These heat-cores generate spatial thermal gradients up to $6,5°$C and are used to calibrate the sensors. Besides the importance of monitoring the temperature of VLSI, the prediction of temperature distributions may also be crucial. Especially for FPGAs, the obtained temperature models may lead to a pro-active thread remapping. In general there are two possibilities for temperature prediction. First, the temperature distribution can be predicted at design time, by regarding the die?s structure and several layers. This approach will be introduced in Section 2. Furthermore, it is possible to predict the temperature distribution on-line at runtime, which may be crucial for reconfigurable FPGA devices. This approach will be introduced at Section 3.

2 Post-Fabrication Heat Flow Modeling Approaches

One popular approach to model heat flow on VLSI is to make use of the duality between thermal and electrical phenomena. HotSpot [3] for example is a tool, that simulate temperature of VLSI designs by modeling the die by an resistance capacitance (RC) network, which is an electric circuit consisting of (thermal) resistors and capacitors (heat

absorption capability). Many of the post-fabrication heat flow modeling approaches know precisely about several layers' properties of the chip, like the layers' thickness and temperature conductivity. Figure 1 depicts a simple RC network with only two layers, heat sources and a heat sink. Usually a chip contains about nine layers, such as heat sink, heat spreader, silicon bulk, interconnect layer, etc. Each of these layers is divided in to an arbitrary number of block, which are laterally and vertically interconnected. The temperature distribution is then derived out of the calculated vertical and lateral resistances.

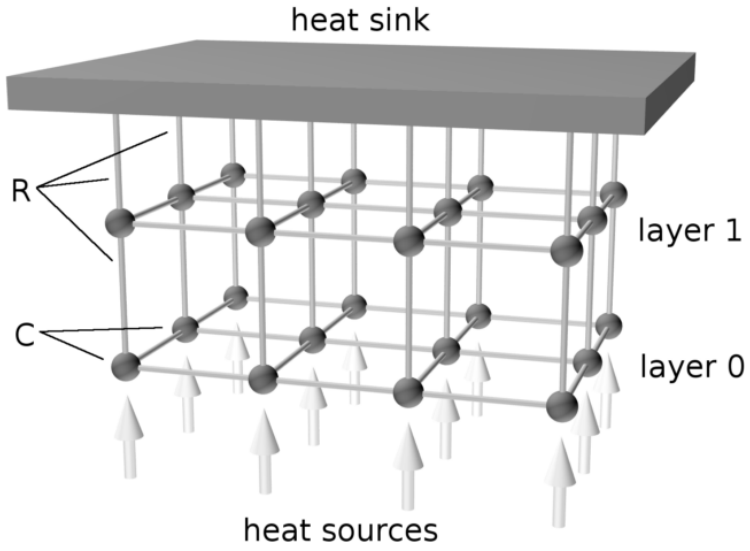

Figure 1: RC-Network with two layers [2]

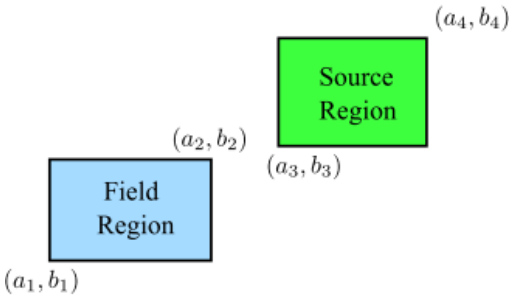

Figure 2: The temperature in the field region is calculated from the power of the source field [4]

Another approach for post-fabrication heat flow modeling is proposed in [4]. Just as HotSpot, this approach requires knowledge about the chip's structure, the layers' thickness and thermal conductivity. However, it does not model the thermal behavior as an RC network. On the contrary, the temperature distribution in a field region located between the chip's coordinates (a_1, b_1) and (a_2, b_2) is derived from the power source located between (a_3, b_3) and (a_4, b_4). Figure 2 depicts these regions located on the chip.

This approach faces the problem of solving the heat diffusion equation, which is the differential equation

$$\rho c_p \frac{\partial T(x,y,z,t)}{\partial t} = \nabla \cdot [k(x,y,z,T)\nabla T(x,y,z,t)] + g(x,y,z,t) \tag{1}$$

where ρ is the density of the material ($\frac{kg}{m^3}$), c_p is the specific heat ($\frac{J}{kg \cdot ^\circ C}$), T is the temperature ($^\circ C$) , k is the thermal conductivity ($\frac{W}{m \cdot ^\circ C}$), g is the volume power density ($\frac{W}{m^3}$) and (x, y, z) are the die's coordinates [4].

3 Goals of the Thesis

3.1 On-line Heat Flow Modeling Approach

In contrary to the post-fabrication heat flow modeling approaches, the on-line approach benefits from not necessarily knowing the properties of the several layers of the chip, such as heat conductivity. However, the proposed system [2] also takes advantage of an RC network. But, for the sake of performance, the accuracy is decreased in this model. That is, the number of layers is reduced to two, as Figure 1 depicts. This trade-off reduces the complexity of the system in order to be executed efficiently on embedded devices.

Instead of having fixed parameters for the thermal model, the on-line approach contains a set of free parameters P, which are chosen arbitrarily at the start of a learning algorithm and improved at each step t_i. In order to improve the thermal model, the actual temperature of the die $T_m(t_i, i)$ and the predicted temperature $T_s(P, t_i, j)$ is are compared for each node j. The learning is done by randomized hill climbing in this approach. The goal is the minimization of the mean square error mse dependent on the parameters P.

$$mse(P) = \frac{1}{|N||M|} \cdot \sum_{i \in M} \sum_{j \in N} (T_s(P, t_i, j) - T_m(t_i, j))^2 \tag{2}$$

3.2 Thesis Objectives

The main goal of the thesis is to improve the on-line prediction proposed in [2]. With help of more efficient heat-generating cores, which were introduced in [1], the model shall be improved. Furthermore, the on-line learning algorithm used in the approach given in Section 3.1 will be replaced by other algorithms, which might be more efficient, for example by Simulated Annealing or Evolutionary Algorithms. The result's quality will be evaluated by comparing it to conventional heat flow modeling approaches, which were briefly introduced above.

In order to enable that the temperature sensor grid including several heat-generating cores need to be implemented on the an Xilinx Virtex-5 FPGA (XUPV5-LX110T). In addition to that, there will be a host PC connected to the FPGA, which controls the experiments and adjusts the model's parameters.

4 Structure of the Thesis

The thesis will be structured as follows:

- **Introduction**
- **Heat Flow Modeling Approaches**

  Post-Fabrication
  A detailed overview over post-fabrication heat flow approaches

  On-Line
  Based on [2], the on-line approach is introduced in detail
- **Evolution of On-Line Heat Flow Modeling Approach**

  Learning Algorithms
  Different learning algorithms are introduced in this section

  Methodology
  Methodology and experimental design of the evolutionary on-line learning algorithm
- **Evaluation** The thermal model is evaluated by comparison with conventional temperature models
- **Conclusion**

5 Time Schedule

Figure 3 depicts the intended time schedule of the thesis.

6 Thesis Organization

Besides the thesis' contents, there are several organizational tasks which will be performed during the thesis.

- **Kick-Off Presentation** The thesis' topic and time schedule will be introduced in a 15 minutes presentation.
- **Frequent Meetings** Every (second) week there will be a meeting with the supervisor, in order to keep track of the thesis' progress and potential issues.
- **Documentation** The thesis will be documented accurately. Care is given to clarity and completeness.
- **Final Presentation** Referring to the target agreement, the obtained results will be presented after the submission of the thesis.
- **Submission** The complete compilable and synthesizable code, experimental data, slides of both presentation and the thesis itself will be submitted in digital form.

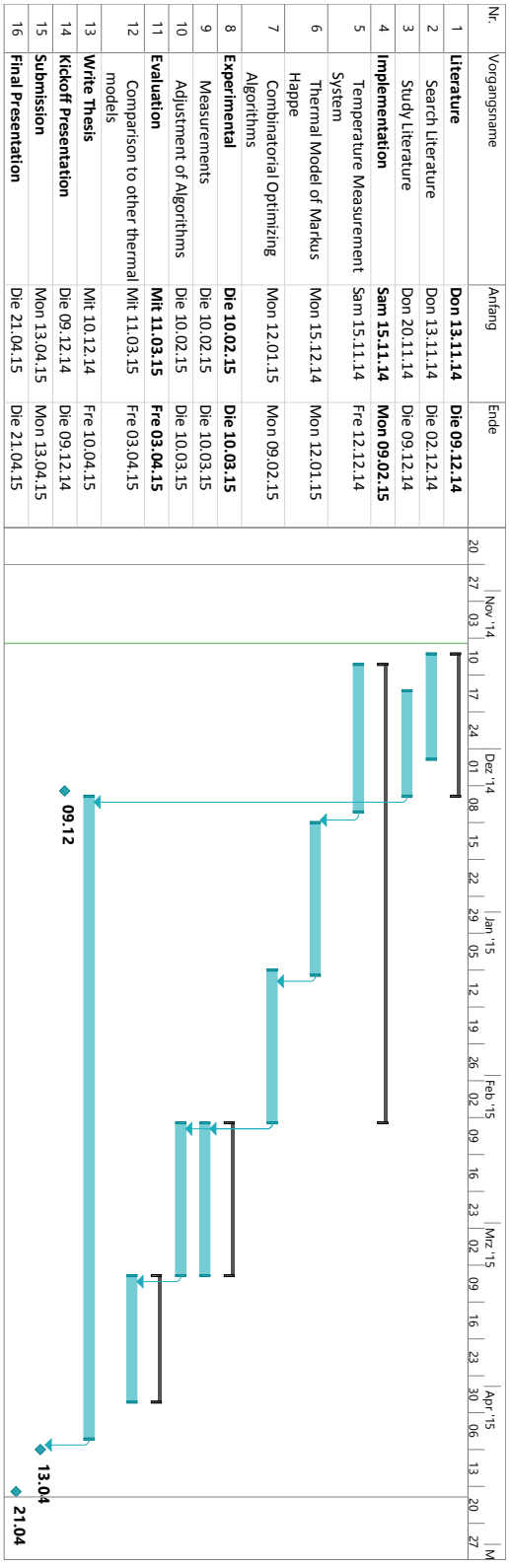

Figure 3: Time schedule

References

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