CS 271
Creating a Makefile

- You can download the files used in this handout from Canvas. They are in the Chapter 5 Module.

A makefile can simplify the task of compiling and linking multiple files. The default file name can be "makefile" or "Makefile".

Each segment of a makefile has this format:

target: dependencies (file(s) needed to produce this target)
→ *optional* Linux command to execute
Tab

The default target is "all".

You must press the tab key before each Linux command. Spaces won't work!!!

The make command checks to see if any of the dependency files have been updated since the date/time on the target.

You should have only one makefile in a directory.

To execute the entire makefile, all you have to do is type

make

To execute only one target within a makefile,

make *targetname*

Here's the makefile I used:

```
all: myprogram

myprogram: somefunctions.o myprogram.o
	gcc somefunctions.o myprogram.o -o myprogram

myprogram.o: myprogram.c somefunctions.h
	gcc -c myprogram.c

somefunctions.o: somefunctions.c somefunctions.h
	gcc -c somefunctions.c

clean:
	rm -rf *.o
```

The "clean" target is a quick way to remove the object files. They're not needed after the executable has been created.

To use this target, just type the command

make clean