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COLD PLATE DESIGN COMPETITION GUIDELINES

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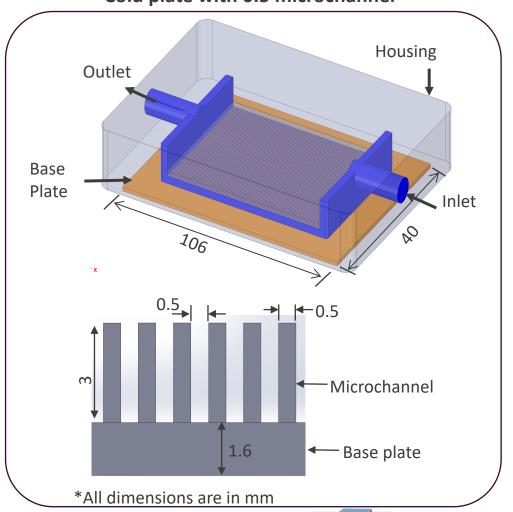
kyogi@purdue.edu



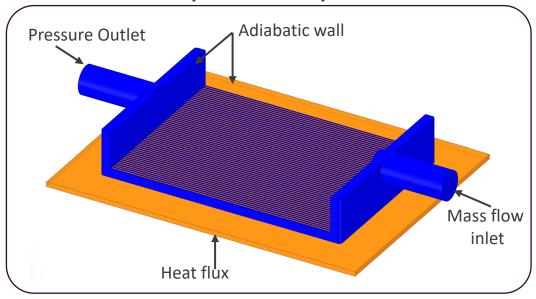




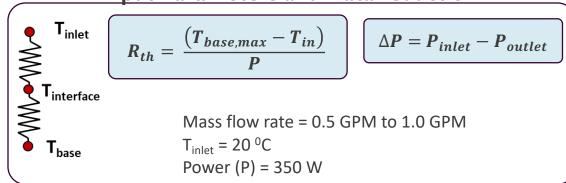
Cold plate with 0.5 microchannel



Geometry and boundary conditions



Input Parameters and Data reduction



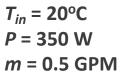


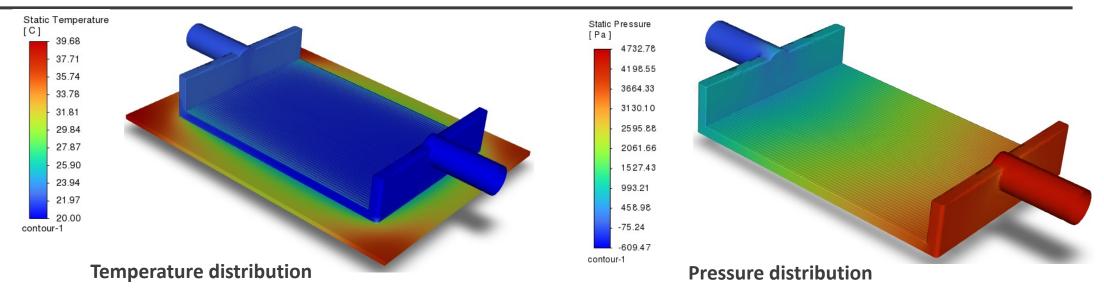


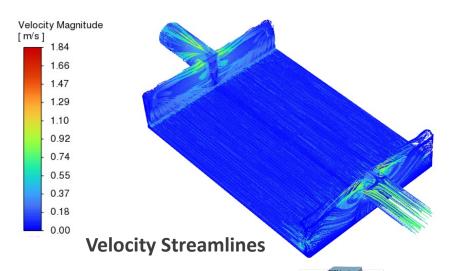
Semiconductor Packaging Laboratory

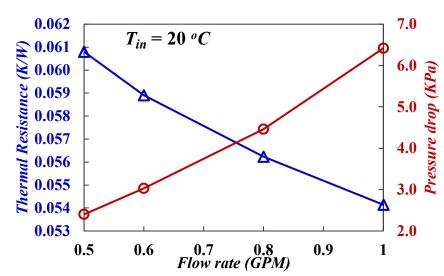
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Simulation performed by Dr. Ketan Yogi from Purdue University.











Semiconductor Packaging Laboratory

(<u>Al</u>l-in-one for Semiconductor <u>P</u>ackaging, <u>H</u>eat transfer, and <u>A</u>ssembly Lab)

