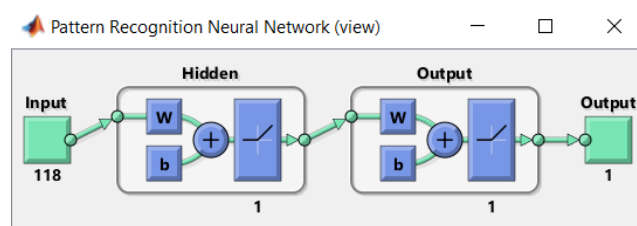
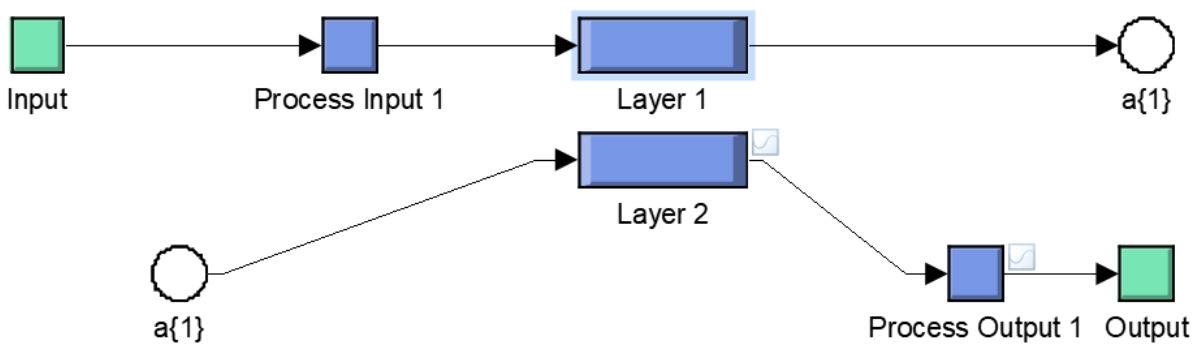


17/8/2020 – pattern recognition neural network_v1

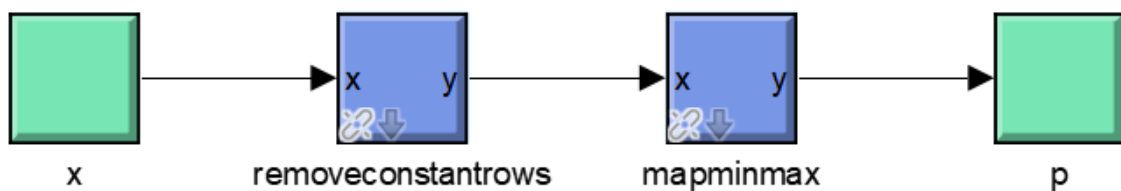
This block diagrams were generated by Simulink from the NN_relu function coding as the NN architecture below. However, this Verilog code reads 'double' value input.



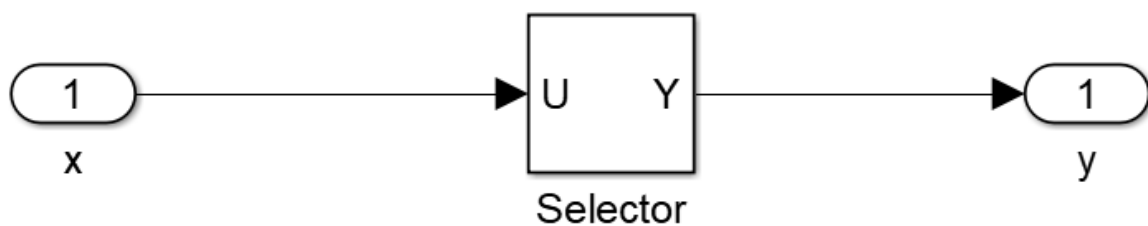
Top – pattern recognition NN



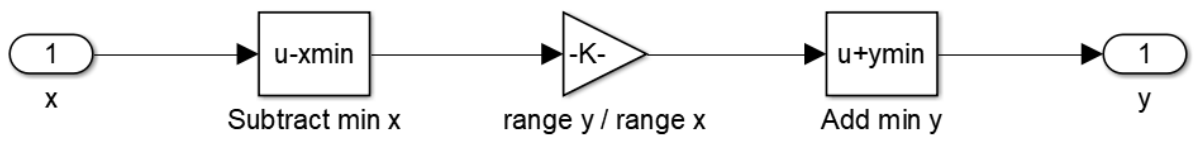
Process Input 1



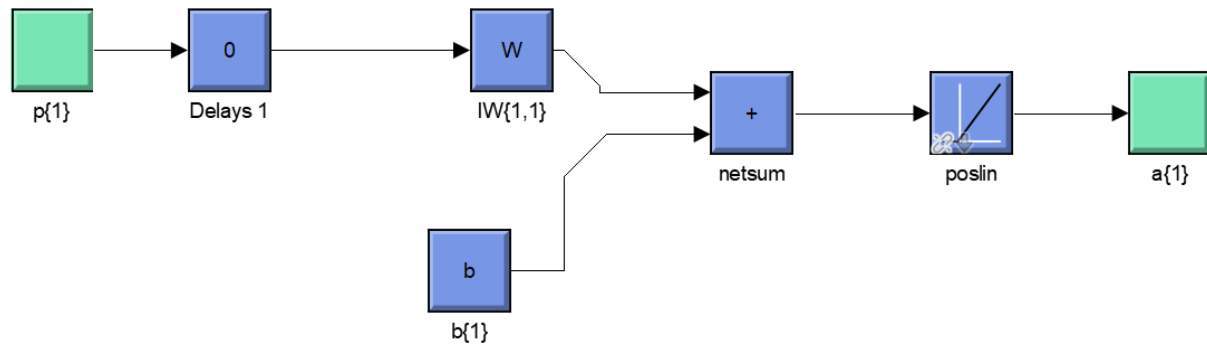
Remove constant row



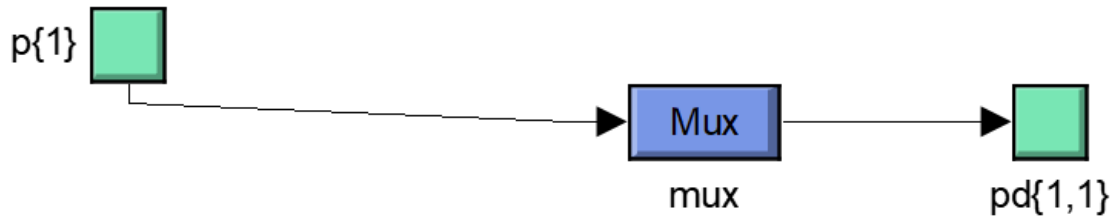
Mapminmax



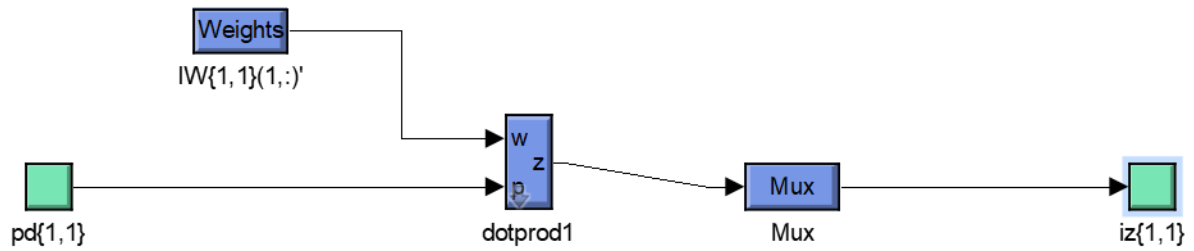
Layer 1



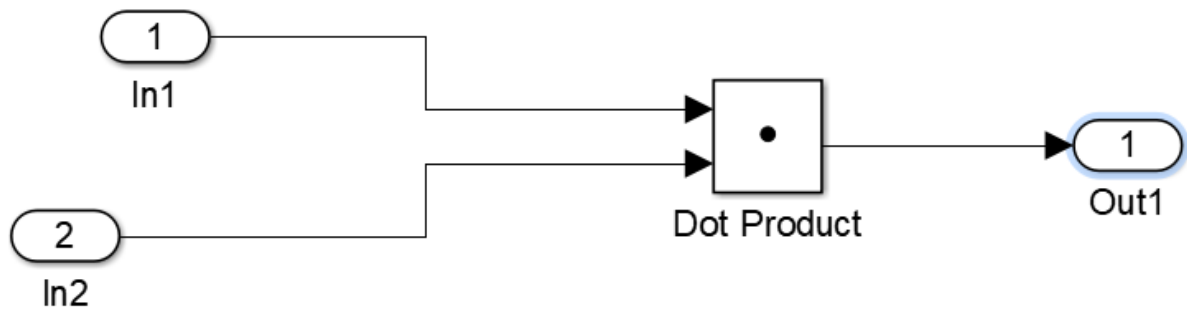
Delays 1



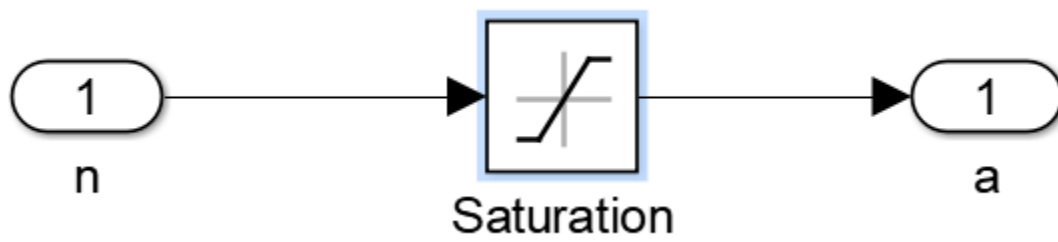
IW{1,1}



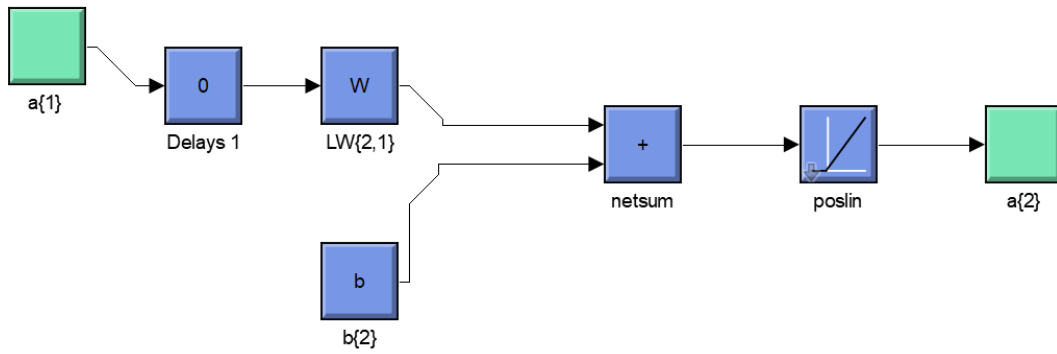
Dotprod1



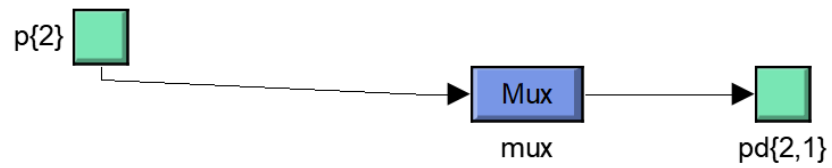
Poslin



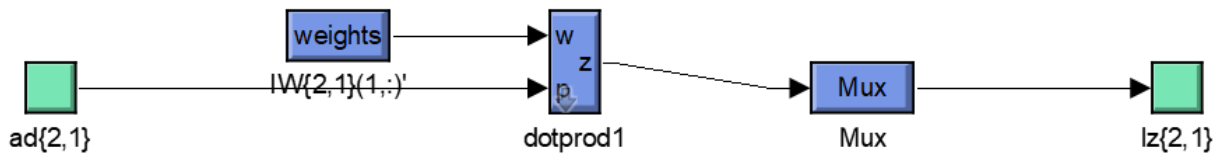
Layer 2



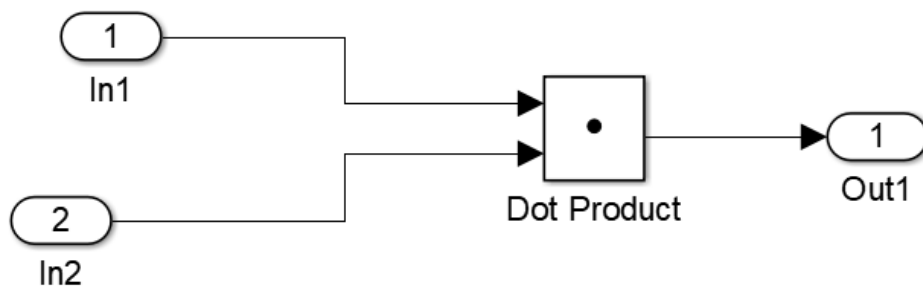
Delays 1



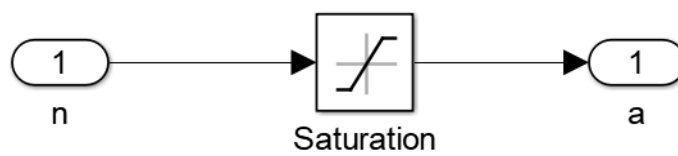
LW{2,1}



Dotprod1



Poslin



Process output 1

