Team04_lab3_report

1. File structure

team04_lab3

|-team04_lab3_report.pdf

|-src

  |-DE2_115

    |-DE2_115.sv

    |-ModeDecoder.sv

    |-SevenHexDecoder.sv

    |-SpeedDecoder.sv

    |-StateDecoder.sv

    |-Debounce.sv

  |-Top.sv

  |-I2C.sv

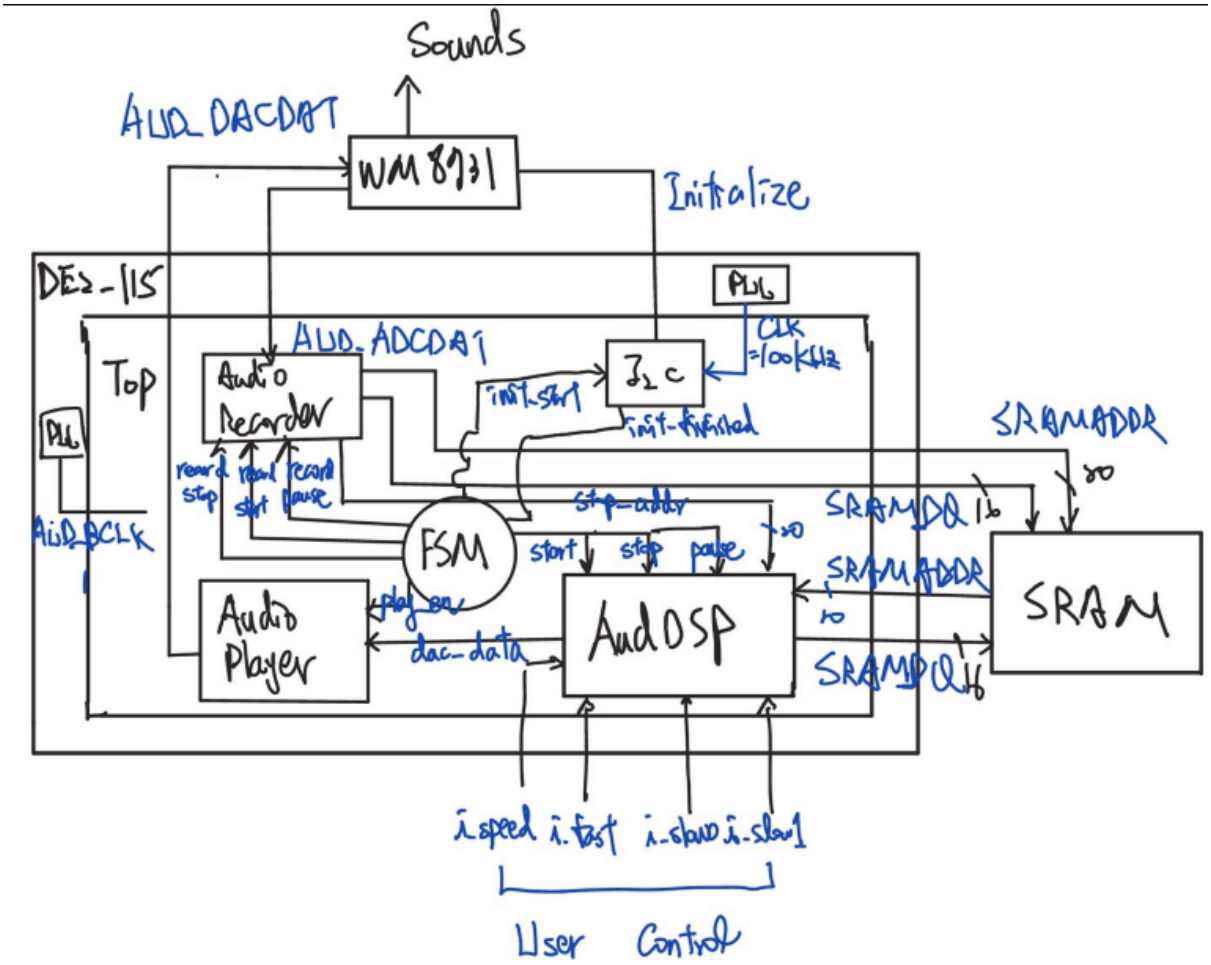
  |-AudioRecorder.sv

  |-AudioPlayer.sv

  |-AudioDSP.v

2. Block Diagram

Top



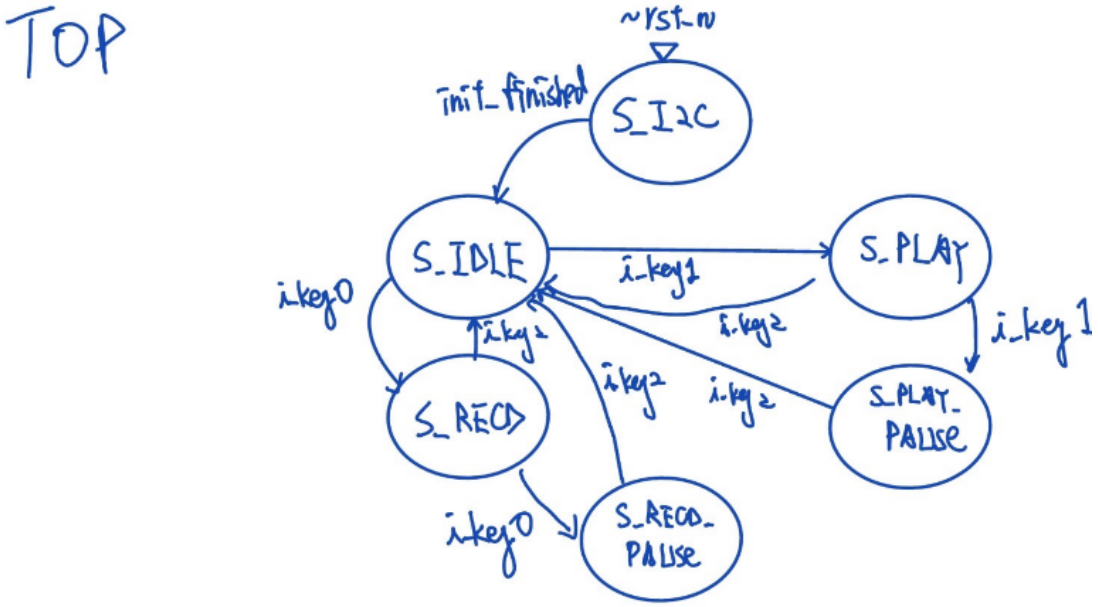
3. FSM and Hardware Scheduling

Top:

Top為錄音機的主要操控模組。包括透過I2C模組來initialize WM8731，並透過控制訊號去執行錄音和撥放的操作。錄音過程，需要透過Top模組，去控制AudioRecorder，並將AUD_ADCDAT存到指定SRAM的address(SRAMADDR)。此外，播放過程也會需要透過Top模組的控制訊號，去控制DSP去access SRAM的data，經過訊號處理後，把16bit資料傳給AudioPlayer，最後將AUD_DACDAT傳給WM8731。

如下圖所示，Top總共有6個state。當**state_r == S_I2C**，init_start會拉成high，這時I2C模組會開始初始化WM8731，直到初始化完成，init_finished會變成1；同時，**state_r**變成 **S_IDLE**，等待i_key_0或i_key_1拉高，才會開始錄音或撥放。當**state_r == S_IDLE**且使用者按下key[0](i_key_0拉高)，這時state_r會進入到S_RECD，並拉高record_start，開

始錄音。倘若在S_RECD時再按下key[0](i_key_0拉高), 則會進入**S_RECD_PAUSE**, 並停止錄音。要再次按下key[0](i_key_0拉高), 才會重新開始錄音。反之, 當**state_r == S_IDLE**且使用者按下key[1](i_key_1拉高), 這時state_r會進入到**S_PLAY**, 並拉高play_start , 並開始播放錄音結果。倘若在S_PLAY時再按下key[1](i_key_1拉高), 則會進入**S_PLAY_PAUSE**, 並停止播放。要再次按下key[1](i_key_1拉高), 才會重新開始錄音。此外, 當**state_r == S_RECD**、**state_r == S_RECD_PAUSE**、**state_r == S_PLAY** 或 **state_r == S_PLAY_PAUSE**, 使用者按下key[2](i_key_2拉高) , 則會進入**S_IDLE**, 等待使用者輸入錄音或撥放指令。



Top 控制訊號:

init_start = (state_r == S_I2C)

record_start = i_key_0 && ((state_r == S_IDLE) || state_r == S_RECD_PAUSE)

record_pause = i_key_0 && (state_r == S_RECD);

record_stop = i_key_2 && ((state_r == S_RECD) || (state_r == S_RECD_PAUSE));

play_en = (state_r == S_PLAY);

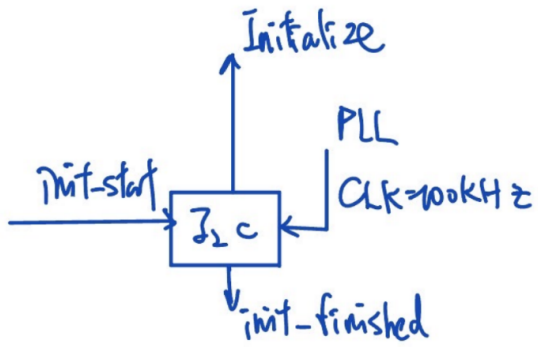
play_start = i_key_1 && (state_r == S_IDLE || state_r == S_PLAY_PAUSE);

play_pause = i_key_1 && (state_r == S_PLAY);

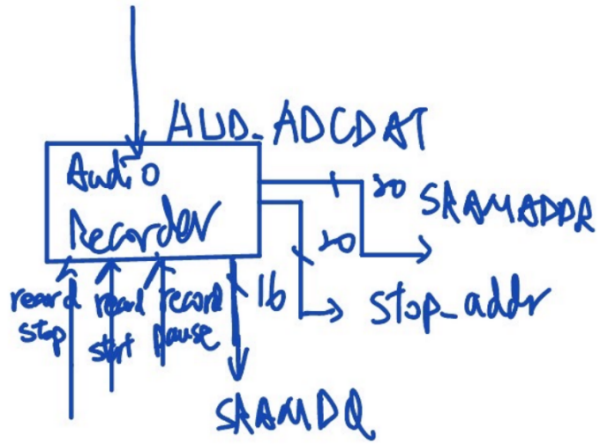
play_stop = i_key_2 && (state_r == S_PLAY || state_r == S_PLAY_PAUSE);

此外, Top模組有許多控制訊號, 分別控制I2C、DSP、AudioRecorder、AudioPlayer等模組。

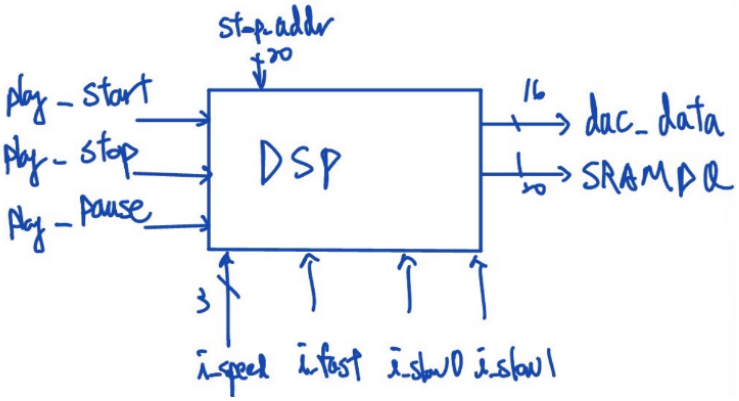
如透過PLL產生的100kHZ的CLK，TOP會用init_start去控制I2C模組，並等待init_finished拉高後，變換state。



此外，當record_start == 1，開始錄音；record_pause == 1，停止錄音；record_stop == 1，暫停錄音，同時 state進入**S_IDLE**。



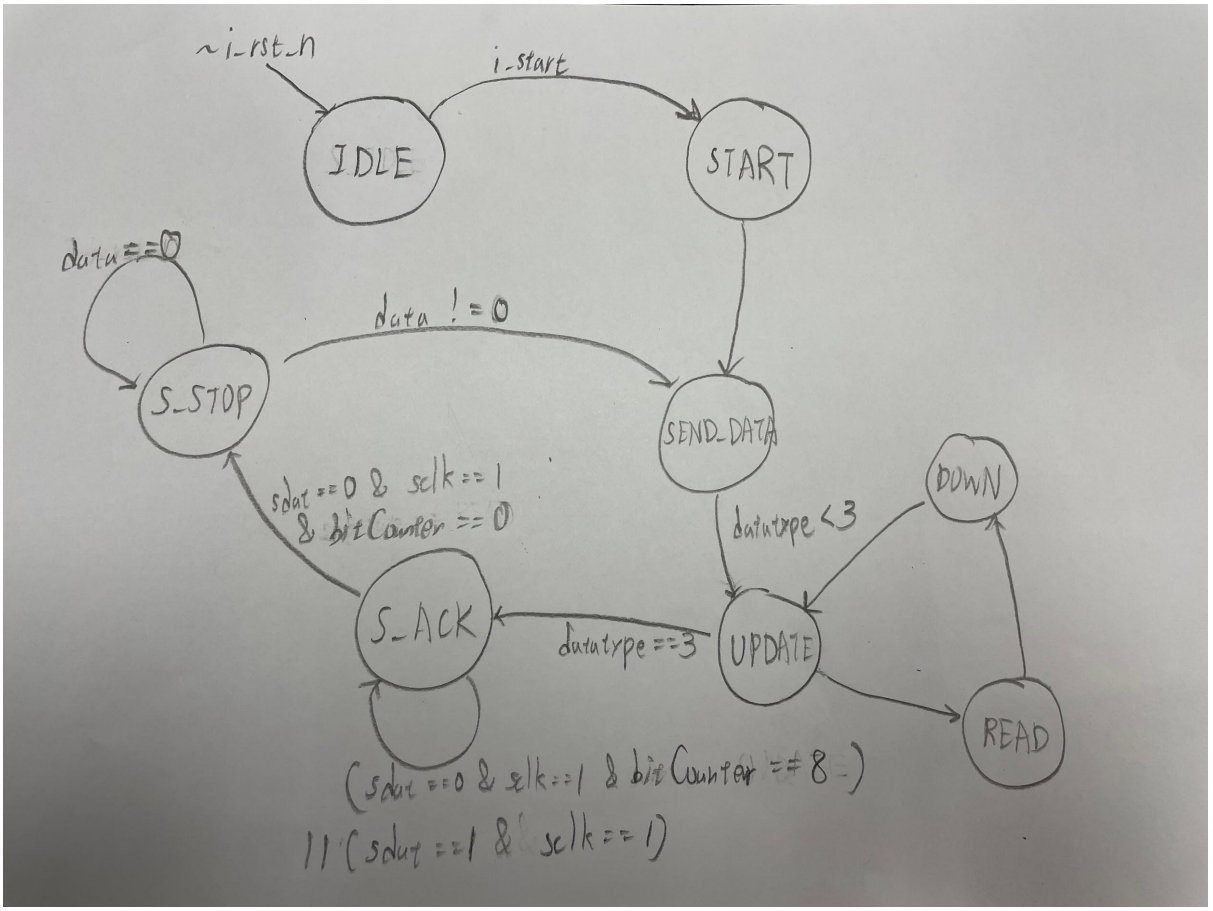
再者，當play_start == 1，DSP開始訊號處理，並從SRAM拿資料，並做完音訊處理後，交給AudioPlayer播放；play_pause == 1，停止信號處理；play_stop == 1，暫停訊號處理，同時 state進入**S_IDLE**。



再者，當play_en == 1，開始播放聲音，將AUD_DAC_DAT傳給WM8731。

I2C:

在**I2C**裡面，會進行Initialize WM8731的動作，總共有5個state: **IDLE, START, SEND_DATA, FINISH, S_STOP**，而在**SEND_DATA**裡又有3個substate: **UPDATE, READ, DOWN**。當按下rst鍵時，會進入**IDLE**，當i_start拉高時，state會跳到**START**，準備開始initialize。在**START**的時候，會對sclk和sdat做符合I2C protocol的改變，並在下一個cycle時state自動跳到**SEND_DATA**。在**SEND_DATA**時，因為每個要初始化的setting都有24bit，我們切三段來傳送，用一個datatype從0~3來記錄，當datatype < 3時，才會去看substate的狀態，substate在**UPDATE**時將sclk拉高，並自動跳到**READ**。在**READ**時，將sclk拉低，並自動跳到**DOWN**。在**DOWN**時，再更新傳出去的sdat，如此即完成1bit的傳送，並會用bitCounter從0跑到8，來看這8bit傳完與否，等到bitCounter == 8，datatype就會加一。等datatype == 3時，state就會跳到**FINISH**。在**FINISH**的時候，會進行sdat拉高，sdat拉滴，sclk拉低的一連串動作，以符合I2C protocol去stop或是準備下一組setting資料，當sdat == 0 && sclk == 1 && bitCounter == 0時，state就會跳到**S_STOP**。在**S_STOP**時，若data != 0，也就是10組setting 資料還沒全部initialize，則跳回**SEND_DATA**，繼續傳送資料，否則就繼續待在**S_STOP**，並將o_finish拉高，傳給**TOP** module表示已initialize結束。



控制訊號

i_start:

⇒ 控制開始進行Initialize, state將從IDLE跳到LEFT_WAIT。

datatype:

⇒ 控制一組24bit setting中, 第幾份8bit資料正在傳送。

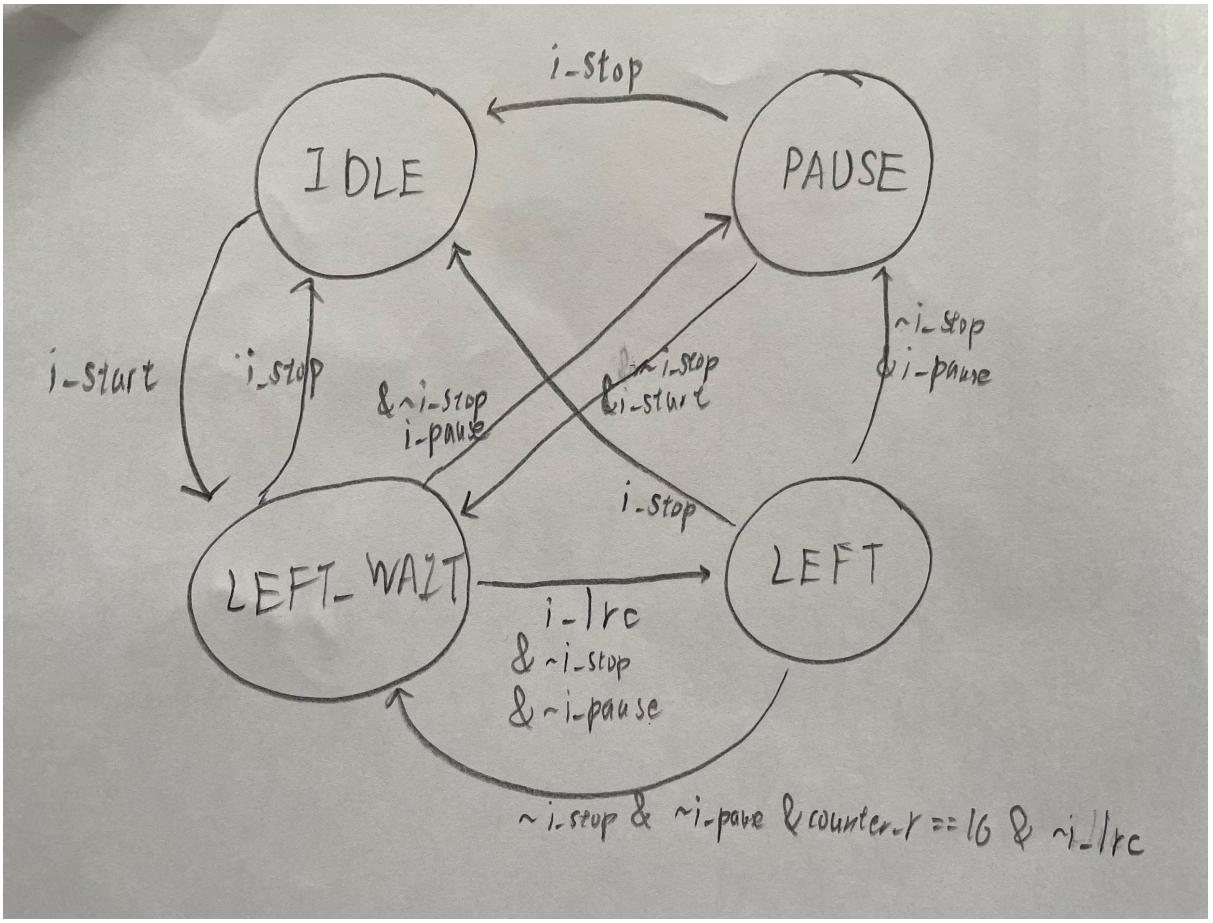
bitCounter:

⇒ 控制一份8bit資料中, 第幾個bit正在傳送。

AudioRecorder:

在**AudioRecorder**裡面有4個state: **IDLE, PAUSE, LEFT**, 和**LEFT_WAIT**。當按下rst鍵時, 就會進到**IDLE**, 接著會等待i_start拉高後, 就會進到**LEFT_WAIT**, 因為我們只存單聲道的音訊, 將會等待i_lrc拉高。當state在**LEFT_WAIT**時, 如果i_stop拉高, 則會停止錄音回到**IDLE**;如果i_pause拉高, state則會跳到**PAUSE**;否則若i_lrc拉剛以後, state就會跳到**LEFT**, 以開始接收音訊。當state在**LEFT**時候, AudioPlayer會接收來自WM8731的音訊i_data, 並藉由傳送o_address給SRAM, 把音訊存到SRAM裡面。如果i_stop或是i_pause拉高時, 也是會分別進入**IDLE**以及**PAUSE**。因為我們要符合I2S

protocol的傳輸協定, 我們用一個counter 從0跑到16, 一次存一個bit, 將要傳出去給SRAM的o_data存成一個16b個要存進SRAM的資料, 當counter == 16時, 等到i_lrc拉低後, 因為進入存另一聲道的期間, state就會回到**LEFT_WAIT**, 並同時更新o_address。當在PAUSE時, 則是錄音暫停的階段, 若i_stop拉高, 則會跳回IDLE, 否則, 若i_start拉高, 則跳到LEFT_WAIT, 錄音繼續。



控制訊號

i_lrc:

⇒從WM8731進來的Audio CODEC DAC LR Clock, 用來控制正在儲存音訊給左聲道或是右聲道。

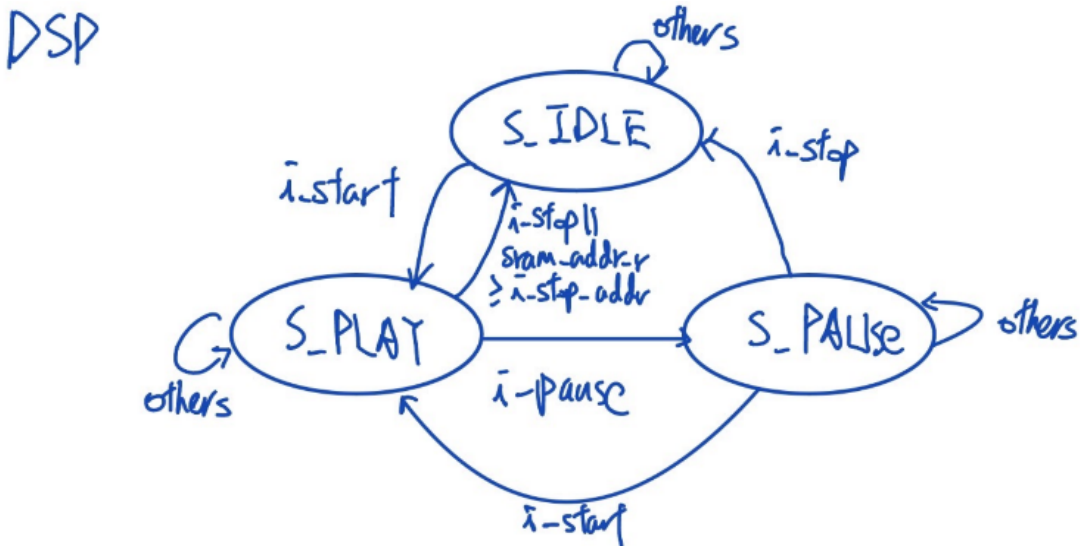
counter_r, counter_w:

⇒用來控制存入o_data第幾個bit, 從0跑到16, 每次存入來自WM8731的1bit資料i_data

AudioDSP:

DSP主要有3個state, 當reset完之後, **state_r = S_IDLE**。DSP會等待i_start == 1時, 進入**S_PLAY**。如果遇到i_stop == 1或是sram_addr_r >= i_stop_addr(i.e DSP準備要access的address超過錄音錄到的address), state會進入**S_IDLE**。倘若i_pause == 1, state則

會從**S_PLAY** 進入 **S_PAUSE**。在**S_PAUSE**的狀態，倘若i_start 又被拉高，則state 進入 **S_PLAY**；倘若i_stop == 1，則進入**S_IDLE**。



控制訊號

prev_daclrck_w = i_daclrck , prev_daclrck_r

⇒用來記錄前一個cycle是屬於甚麼聲道傳輸。

prev_data_w, prev_data_r

⇒用來記錄前一次傳輸的資料，可以用在一次內插法。

speed = i_speed + 1

⇒用來記錄實際加速倍數。

counter_r, counter_w

⇒ 用在慢速撥放，計算要在同一個sram address停留幾個cycle。

DSP主要做的事情是根據傳進來的i_sram_data，以及各種速度模式的訊號(normal, i_fast, i_slow_0, i_slow_1, i_speed [2:0])去做音訊處理，並傳出處理完的數位訊號o_dac_data以及下一筆data的sram's address (o_sram_addr)。值得注意的是，我們要確保當切換至左聲道時(prev_daclrck && ~i_daclrck)，再更新sram_addr_w。

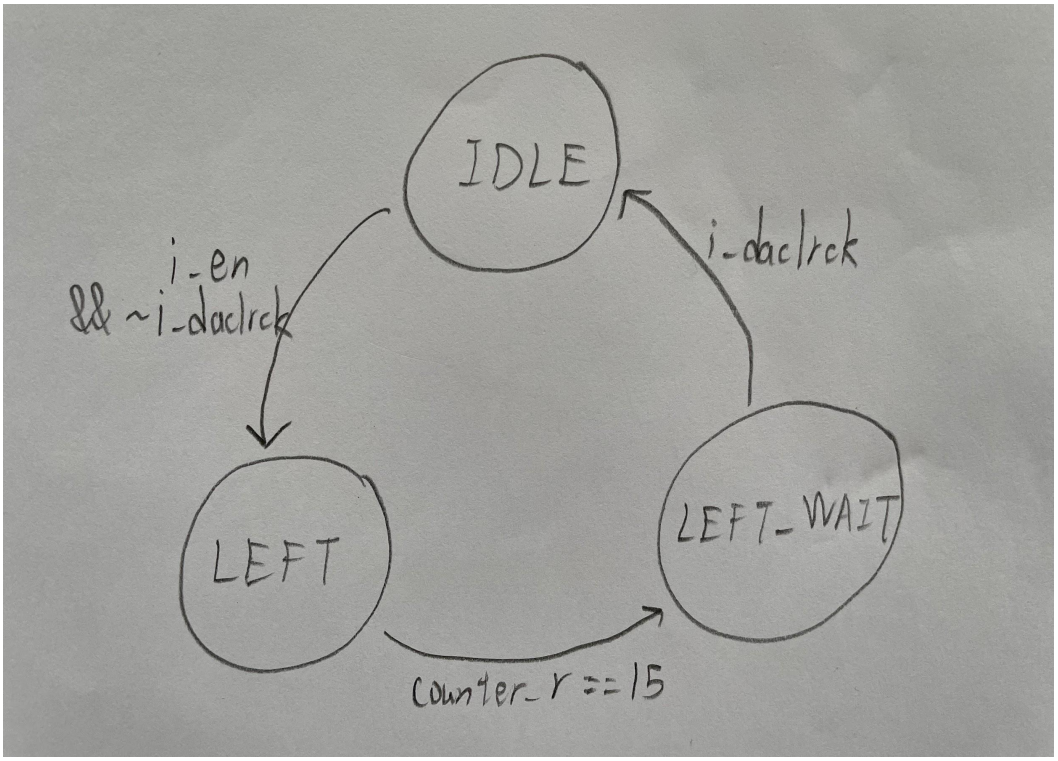
以下是o_dac_data和o_sram_addr更新的rule。

Mode	o_dac_data	o_sram_addr
Normal	o_dac_data_w = i_sram_data	sram_addr_r + 1
Fast	o_dac_data_w = i_sram_data	sram_addr_r + speed
Slow0(constant	o_dac_data_w = i_sram_data	(counter_r > i_speed) ?

interpolation)		sram_addr_r + 1: sram_add_r
Slow1(linear interpolation)	o_dac_data_w = (prev_data_r*(speed - counter_r) + i_sram_data*(counter_r)) / speed	(counter_r > i_speed) ? sram_addr_r + 1: sram_add_r

AudioPlayer:

AudioPlayer 共有3個state: **IDLE**, **LEFT**, 和 **LEFT_WAIT**。當按下rst鍵時state會進入**IDLE**, 接著等待從**DSP**進入的控制訊號i_en拉高, 以及i_daclrck拉低以後, state就會進入**LEFT**。由於我們是在只傳送左聲道音訊給WM8731, 故會在i_daclrck為0時傳送資料。在**LEFT**的時候就會開始傳送資料, 為了傳送16bit資料, 需要符合I2S的protocol, 故利用counter從0跑到15, 一次傳1bit, 等到counter == 15時即傳送完該筆16bit資料, 於是state就跳到**LEFT_WAIT**。由於我們不會傳送右聲道的音訊, 所以在i_daclrck拉高時, state會跳到**IDLE**, 等到下一筆從DSP的資料進來後, 再等待傳送左聲道資料。



控制訊號

i_en:

⇒ 從DSP傳進來, 決定當state在**IDLE**時, 資料是否已收到, 可以準備送左聲道音訊。

i_daclrck:

⇒ 從WM8731進來的Audio CODEC DAC LR Clock, 用來控制正在傳送音訊給左聲道或是右聲道。

counter_r, counter_w:

⇒ 每當一筆16bit data進來時, counter從0跑到15, 傳送data的第(15-**counter_r**)個bit, 重複16次。

4. Bonus

A. 我們可以不用暫停就可以切換播放速度**(fast, slow_0, slow_1)**。

由於我們速度控制都是在DSP裡的**S_PLAY**的 state做判斷, 因此我們只要在播放狀態時切換速度, 就可以隨時切換播放速度, 不用按暫停調整或是reset後調整。

B. 我們有利用七段顯示器去顯示錄音和播放的秒數

在Top裡面我們用一個counter, 從0跑到12M, 以及一個傳出去給七段顯示器的秒數訊號o_time。若是在Top的state為**S_RECD**或是**S_PLAY**時, counter 每過一個cycle就會加一, 直到counter等於12M後, o_time就會加一, 最多跑到32為止, 表示只能錄到或播到32秒。

C.我們利用七段顯示器去顯示現在**Top**在哪個**state**以及顯示播放速度、播放模式

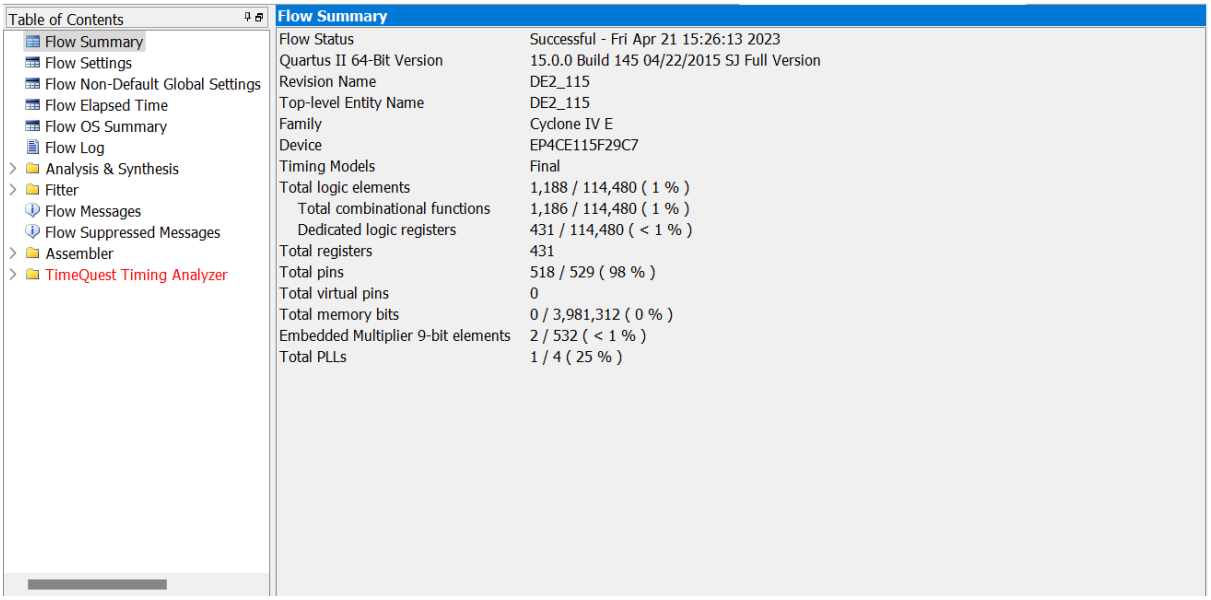
透過把top的state接出去給**DE2_115**的模組, 我們可以把現在的工作狀態(**S_INIT(0), S_IDLE(1), S_RECD(2), S_RECD_PAUSE(3), S_PLAY(4), S_PLAY_PAUSE(5)**)印在七段顯示器。

我們透過把SW[2:0](switch), 接到七段顯示器, 以顯示正在播放的速度(0~7) i_speed 。此外, 把SW[5:3], 接到七段顯示器, 去顯示speed mode。

D.我們利用**LEDR**來顯示錄音以及撥放進度條, **LEDG**顯示閒置及暫停狀態

我們讓每當o_time加二時, LEDR就會多增加一個燈, 總共利用其中16個燈來記錄32秒的錄音或播放進度。另外, 當state == **IDLE** 或是**S_RECD_PAUSE**或是**S_PLAY_PAUSE**時, LEDG就會全亮。

5. Fitter Summary



6. Time analyer

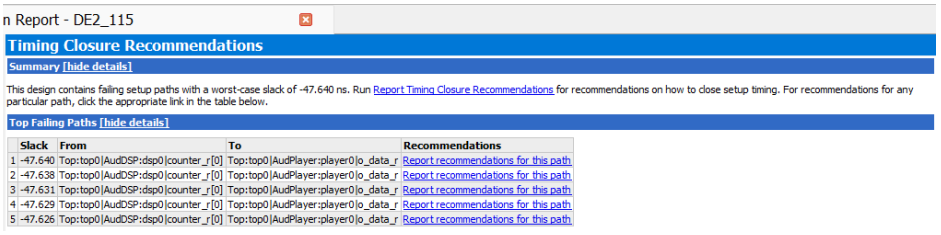
Timing Closure Recommendations

Summary [hide details]

This design contains failing setup paths with a worst-case slack of -47.640 ns. Run Report Timing Closure Recommendations for recommendations on how to clo particular path, click the appropriate link in the table below.

Top Failing Paths [hide details]

	Slack	From	To	Recommendations
1	-47.640	Top:top0|AudDSP:dsp0|counter_r[0]	Top:top0|AudPlayer:player0|o_data_r	Report recommendations for this path
2	-47.638	Top:top0|AudDSP:dsp0|counter_r[0]	Top:top0|AudPlayer:player0|o_data_r	Report recommendations for this path
3	-47.631	Top:top0|AudDSP:dsp0|counter_r[0]	Top:top0|AudPlayer:player0|o_data_r	Report recommendations for this path
4	-47.629	Top:top0|AudDSP:dsp0|counter_r[0]	Top:top0|AudPlayer:player0|o_data_r	Report recommendations for this path
5	-47.626	Top:top0|AudDSP:dsp0|counter_r[0]	Top:top0|AudPlayer:player0|o_data_r	Report recommendations for this path



n Report - DE2_115

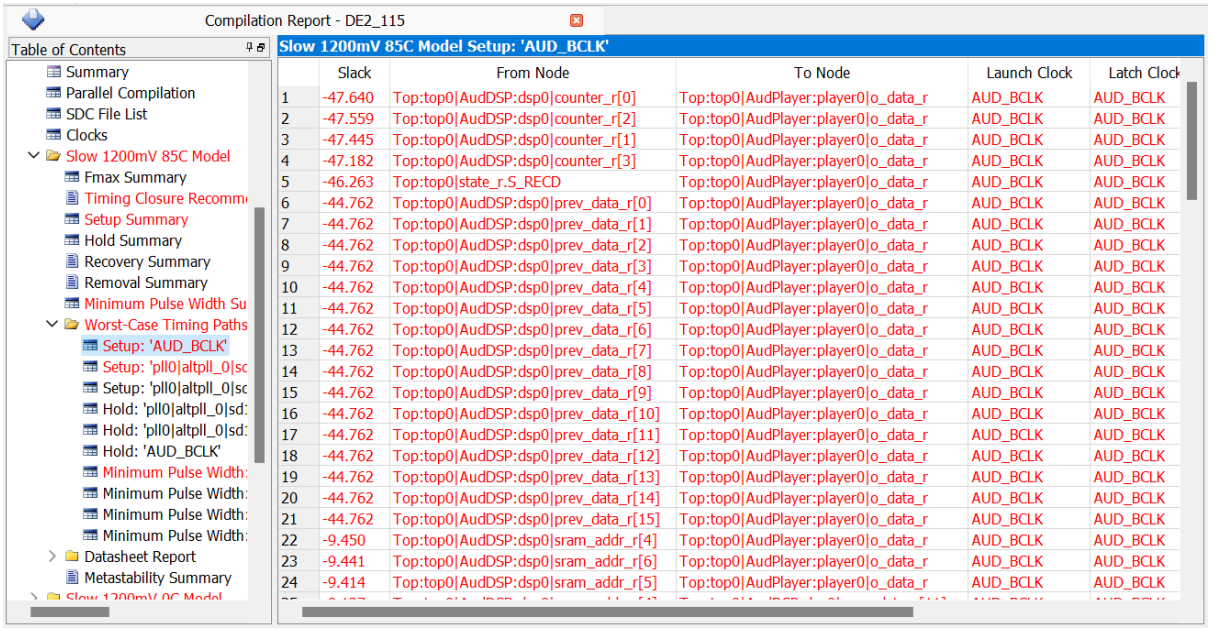
Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-47.640	-1265.137
2	pll0|altpll_0|sd1|pll7|clk[1]	-6.016	-1422.040
3	pll0|altpll_0|sd1|pll7|clk[0]	80.641	0.000

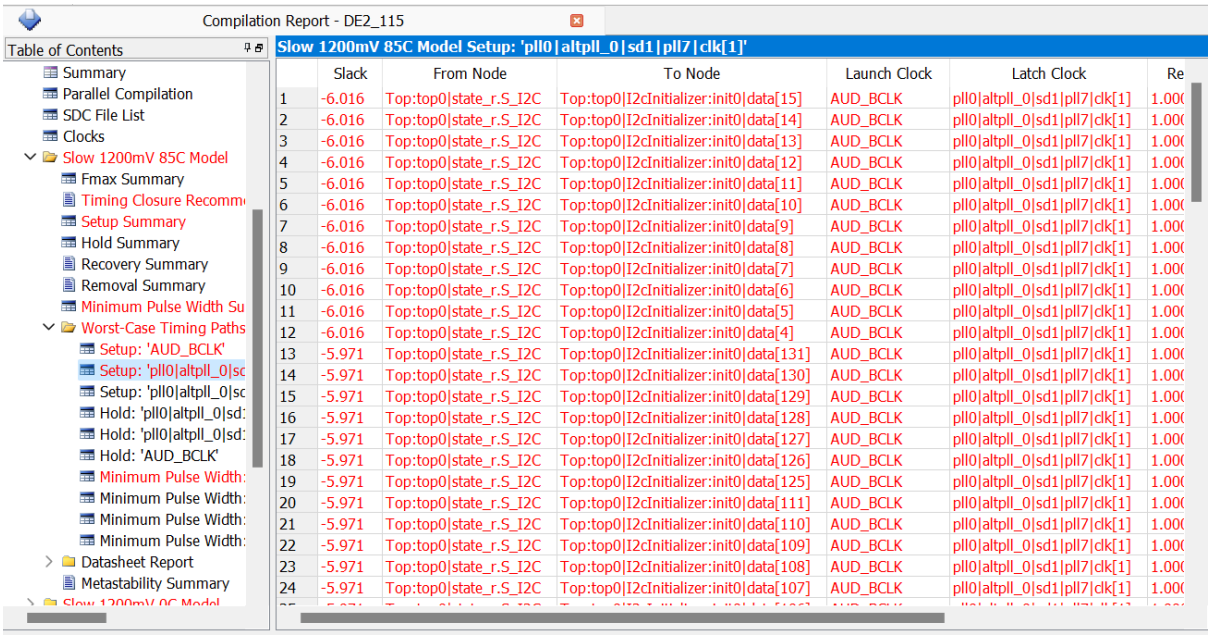
n Report - DE2_115

Slow 1200mV 85C Model Minimum Pulse Width Summary

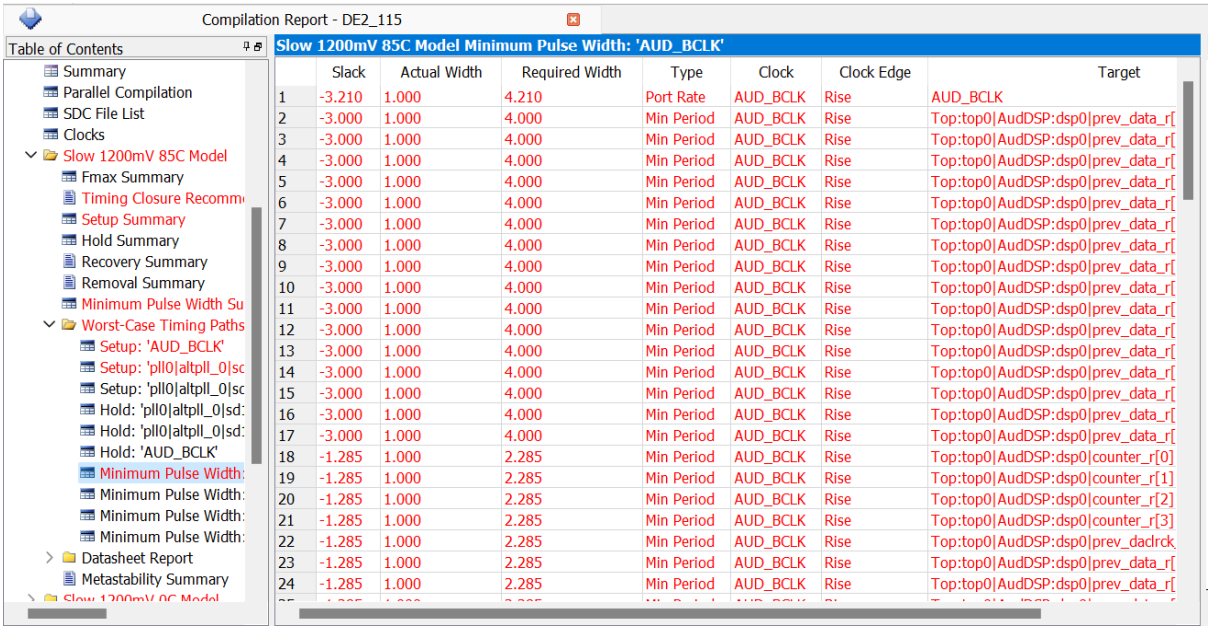
	Clock	Slack	End Point TNS
1	AUD_BCLK	-3.210	-252.721
2	CLOCK_50	9.819	0.000
3	pll0|altpll_0|sd1|pll7|clk[0]	41.374	0.000
4	pll0|altpll_0|sd1|pll7|clk[1]	4999.699	0.000



	Slack	From Node	To Node	Launch Clock	Latch Clock
1	-47.640	Top:top0|AudDSP:dsp0|counter_r[0]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
2	-47.559	Top:top0|AudDSP:dsp0|counter_r[2]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
3	-47.445	Top:top0|AudDSP:dsp0|counter_r[1]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
4	-47.182	Top:top0|AudDSP:dsp0|counter_r[3]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
5	-46.263	Top:top0|state_r.S_RECD	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
6	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[0]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
7	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[1]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
8	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[2]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
9	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[3]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
10	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[4]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
11	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[5]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
12	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[6]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
13	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[7]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
14	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[8]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
15	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[9]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
16	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[10]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
17	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[11]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
18	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[12]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
19	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[13]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
20	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[14]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
21	-44.762	Top:top0|AudDSP:dsp0|prev_data_r[15]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
22	-9.450	Top:top0|AudDSP:dsp0|sram_addr_r[4]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
23	-9.441	Top:top0|AudDSP:dsp0|sram_addr_r[6]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
24	-9.414	Top:top0|AudDSP:dsp0|sram_addr_r[5]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK



	Slack	From Node	To Node	Launch Clock	Latch Clock	Re
1	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[15]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
2	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[14]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
3	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[13]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
4	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[12]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
5	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[11]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
6	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[10]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
7	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[9]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
8	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[8]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
9	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[7]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
10	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[6]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
11	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[5]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
12	-6.016	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[4]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
13	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[131]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
14	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[130]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
15	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[129]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
16	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[128]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
17	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[127]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
18	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[126]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
19	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[125]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
20	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[111]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
21	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[110]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
22	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[109]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
23	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[108]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
24	-5.971	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[107]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(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Hold: 'pll0|altpll_0|sd:
Hold: 'pll0|altpll_0|sd:
Hold: 'AUD_BCLK'
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Minimum Pulse Width:
Minimum Pulse Width:
Minimum Pulse Width:
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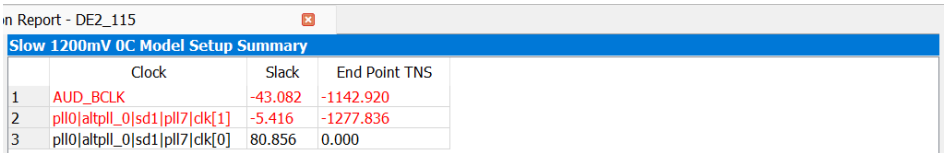
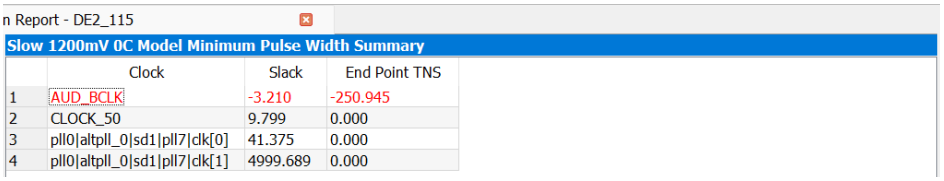
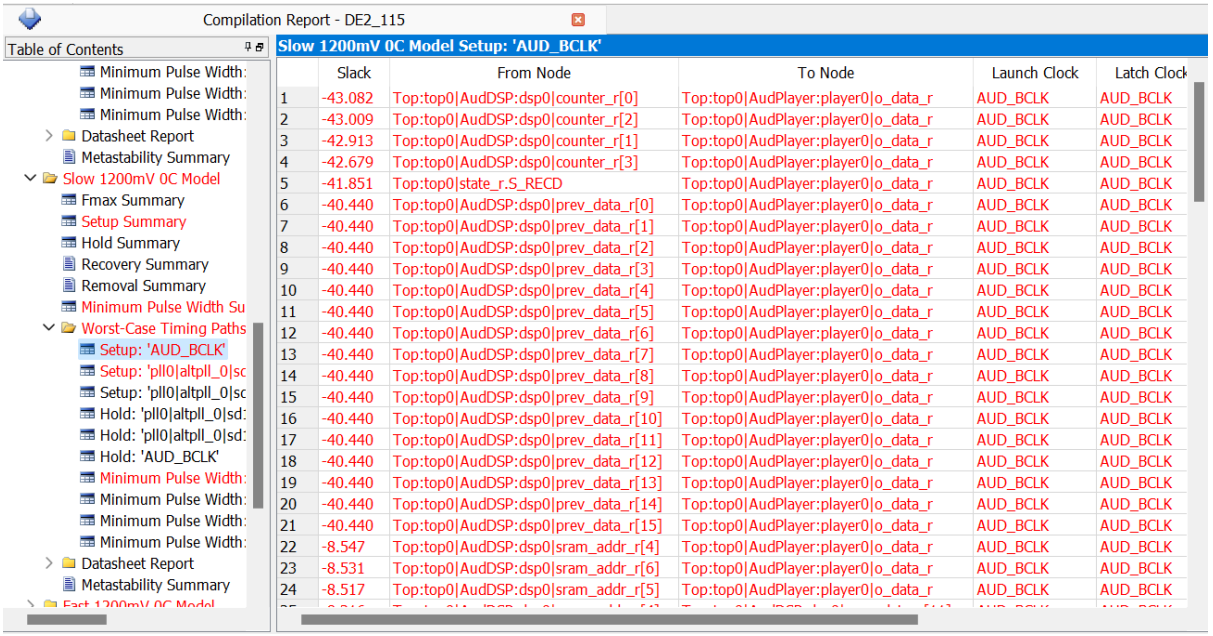
Slow 1200mV 85C Model Minimum Pulse Width: 'AUD_BCLK'
Slack
Actual Width
Required Width
Type
Clock
Clock Edge
Target
1 -3.210 1.000 4.210 Port Rate AUD_BCLK Rise AUD_BCLK
2 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
3 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
4 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
5 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
6 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
7 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
8 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
9 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
10 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
11 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
12 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
13 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
14 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
15 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
16 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
17 -3.000 1.000 4.000 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
18 -1.285 1.000 2.285 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|counter_r[0]
19 -1.285 1.000 2.285 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|counter_r[1]
20 -1.285 1.000 2.285 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|counter_r[2]
21 -1.285 1.000 2.285 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|counter_r[3]
22 -1.285 1.000 2.285 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_daclrck
23 -1.285 1.000 2.285 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[
24 -1.285 1.000 2.285 Min Period AUD_BCLK Rise Top:top0|AudDSP:dsp0|prev_data_r[


n Report - DE2_115
Slow 1200mV 0C Model Setup Summary
Clock
Slack
End Point TNS
1 AUD_BCLK -43.082 -1142.920
2 pll0|altpll_0|sd1|pll7|clk[1] -5.416 -1277.836
3 pll0|altpll_0|sd1|pll7|clk[0] 80.856 0.000


n Report - DE2_115
Slow 1200mV 0C Model Minimum Pulse Width Summary
Clock
Slack
End Point TNS
1 AUD_BCLK -3.210 -250.945
2 CLOCK_50 9.799 0.000
3 pll0|altpll_0|sd1|pll7|clk[0] 41.375 0.000
4 pll0|altpll_0|sd1|pll7|clk[1] 4999.689 0.000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Setup: 'pll0|altpll_0|sc
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Hold: 'pll0|altpll_0|sd:
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Minimum Pulse Width:
Minimum Pulse Width:
Minimum Pulse Width:
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Slack
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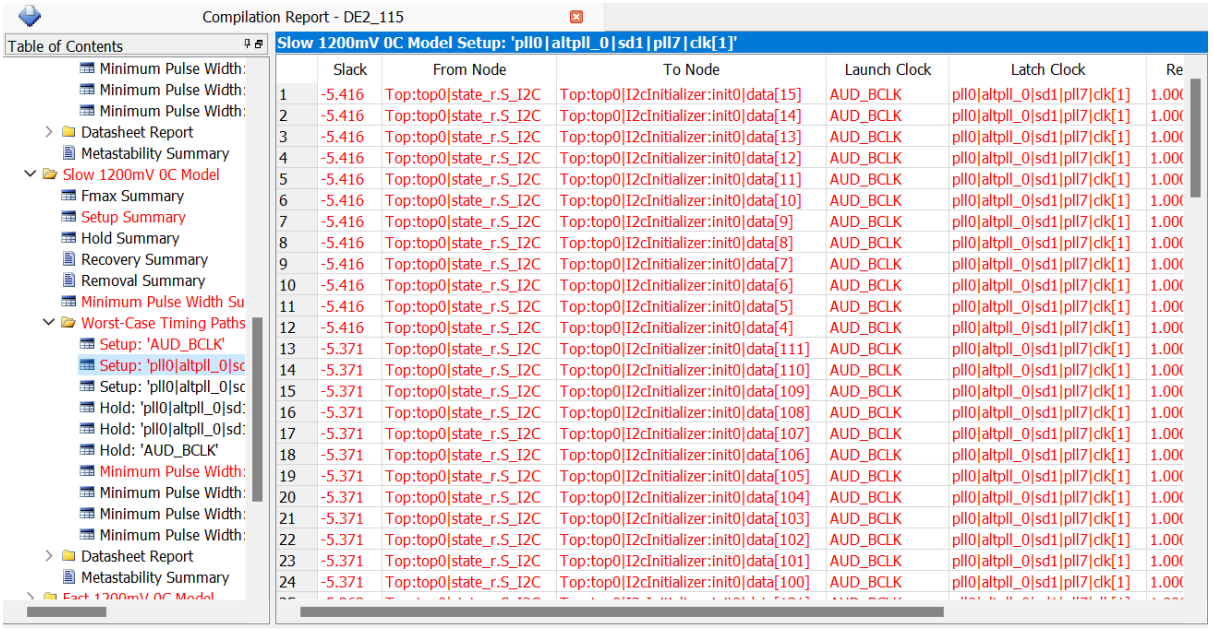
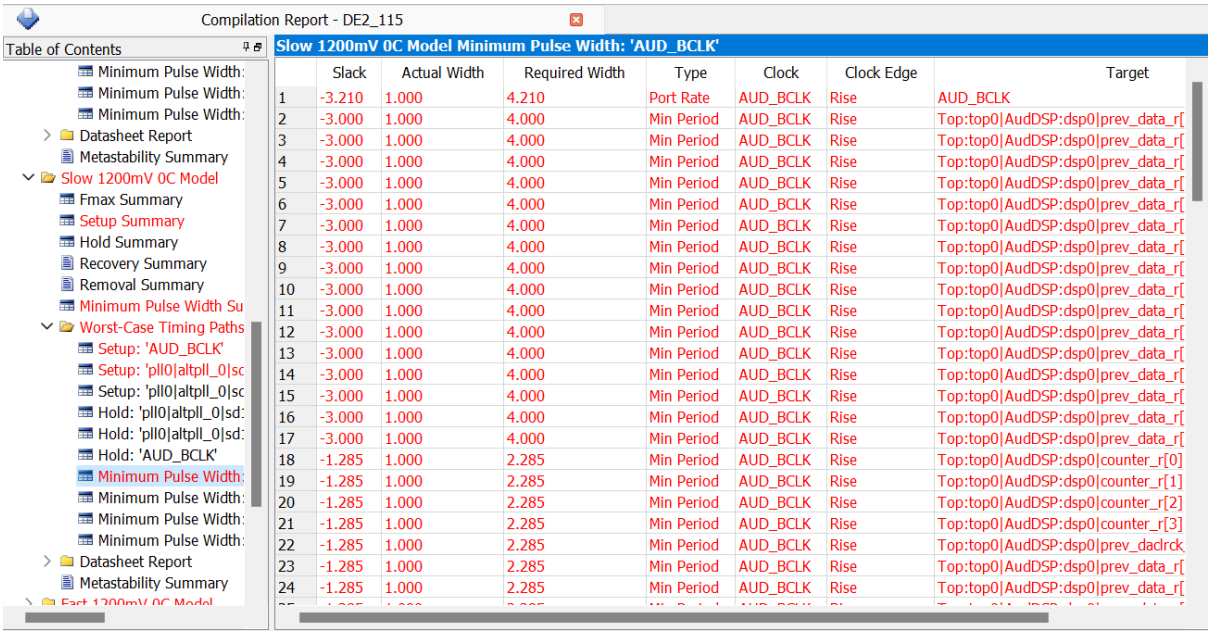
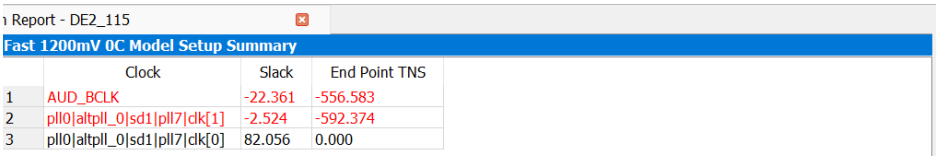
Launch Clock
Latch Clock
1 -43.082 Top:top0|AudDSP:dsp0|counter_r[0] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
2 -43.009 Top:top0|AudDSP:dsp0|counter_r[2] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
3 -42.913 Top:top0|AudDSP:dsp0|counter_r[1] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
4 -42.679 Top:top0|AudDSP:dsp0|counter_r[3] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
5 -41.851 Top:top0|state_r.S_RECD Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
6 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[0] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
7 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[1] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
8 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[2] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
9 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[3] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
10 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[4] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
11 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[5] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
12 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[6] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
13 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[7] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
14 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[8] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
15 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[9] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
16 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[10] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
17 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[11] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
18 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[12] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
19 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[13] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
20 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[14] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
21 -40.440 Top:top0|AudDSP:dsp0|prev_data_r[15] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
22 -8.547 Top:top0|AudDSP:dsp0|sram_addr_r[4] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
23 -8.531 Top:top0|AudDSP:dsp0|sram_addr_r[6] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK
24 -8.517 Top:top0|AudDSP:dsp0|sram_addr_r[5] Top:top0|AudPlayer:player0|o_data_r AUD_BCLK AUD_BCLK



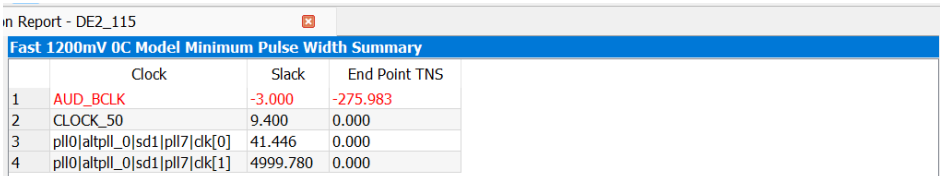
	Slack	From Node	To Node	Launch Clock	Latch Clock	Re
1	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[15]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
2	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[14]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
3	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[13]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
4	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[12]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
5	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[11]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
6	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[10]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
7	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[9]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
8	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[8]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
9	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[7]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
10	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[6]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
11	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[5]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
12	-5.416	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[4]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
13	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[111]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
14	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[110]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
15	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[109]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
16	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[108]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
17	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[107]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
18	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[106]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
19	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[105]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
20	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[104]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
21	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[103]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
22	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[102]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
23	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[101]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
24	-5.371	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[100]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(



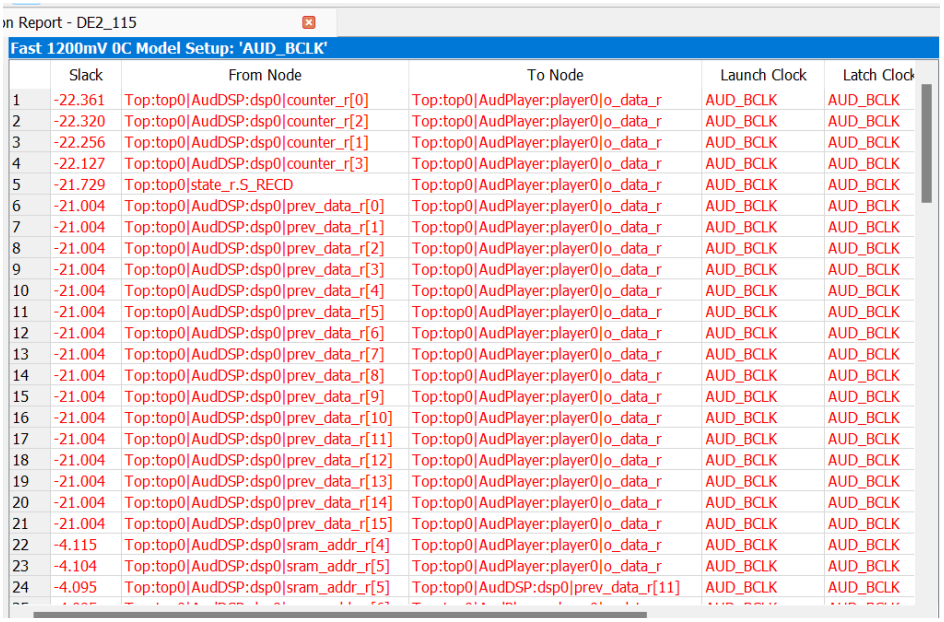
	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.210	1.000	4.210	Port Rate	AUD_BCLK	Rise	AUD_BCLK
2	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
3	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
4	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
5	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
6	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
7	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
8	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
9	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
10	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
11	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
12	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
13	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
14	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
15	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
16	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
17	-3.000	1.000	4.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
18	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[0]
19	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[1]
20	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[2]
21	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[3]
22	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_daclrck
23	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
24	-1.285	1.000	2.285	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[



	Clock	Slack	End Point TNS
1	AUD_BCLK	-22.361	-556.583
2	pll0|altpll_0|sd1|pll7|clk[1]	-2.524	-592.374
3	pll0|altpll_0|sd1|pll7|clk[0]	82.056	0.000



	Clock	Slack	End Point TNS
1	AUD_BCLK	-3.000	-275.983
2	CLOCK_50	9.400	0.000
3	pll0|altpll_0|sd1|pll7|clk[0]	41.446	0.000
4	pll0|altpll_0|sd1|pll7|clk[1]	4999.780	0.000



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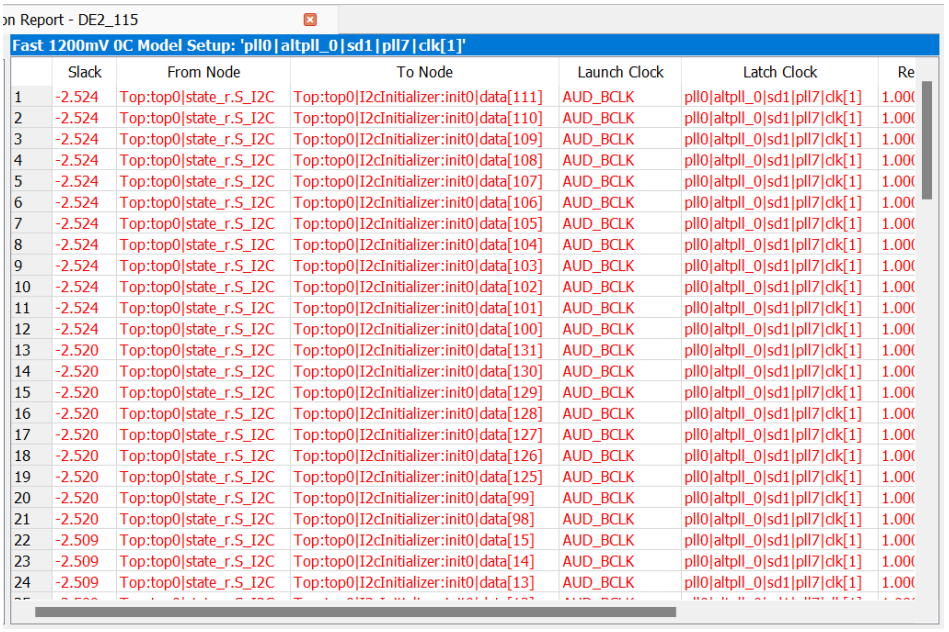
Fast 1200mV 0C Model Setup: 'AUD_BCLK'

	Slack	From Node	To Node	Launch Clock	Latch Clock
1	-22.361	Top:top0|AudDSP:dsp0|counter_r[0]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
2	-22.320	Top:top0|AudDSP:dsp0|counter_r[2]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
3	-22.256	Top:top0|AudDSP:dsp0|counter_r[1]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
4	-22.127	Top:top0|AudDSP:dsp0|counter_r[3]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
5	-21.729	Top:top0|state_r.S_RECD	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
6	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[0]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
7	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[1]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
8	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[2]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
9	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[3]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
10	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[4]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
11	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[5]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
12	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[6]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
13	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[7]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
14	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[8]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
15	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[9]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
16	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[10]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
17	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[11]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
18	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[12]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
19	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[13]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
20	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[14]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
21	-21.004	Top:top0|AudDSP:dsp0|prev_data_r[15]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
22	-4.115	Top:top0|AudDSP:dsp0|sram_addr_r[4]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
23	-4.104	Top:top0|AudDSP:dsp0|sram_addr_r[5]	Top:top0|AudPlayer:player0|o_data_r	AUD_BCLK	AUD_BCLK
24	-4.095	Top:top0|AudDSP:dsp0|sram_addr_r[5]	Top:top0|AudDSP:dsp0|prev_data_r[11]	AUD_BCLK	AUD_BCLK



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Fast 1200mV 0C Model Setup: 'pll0\|altpll_0\|sd1\|pll7\|clk[1]'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Re
1	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[111]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
2	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[110]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
3	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[109]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
4	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[108]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
5	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[107]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
6	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[106]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
7	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[105]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
8	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[104]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
9	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[103]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
10	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[102]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
11	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[101]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
12	-2.524	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[100]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
13	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[131]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
14	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[130]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
15	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[129]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
16	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[128]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
17	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[127]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
18	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[126]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
19	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[125]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
20	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[99]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
21	-2.520	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[98]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
22	-2.509	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[15]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
23	-2.509	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[14]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(
24	-2.509	Top:top0|state_r.S_I2C	Top:top0|I2cInitializer:init0|data[13]	AUD_BCLK	pll0|altpll_0|sd1|pll7|clk[1]	1.00(

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Fast 1200mV 0C Model Minimum Pulse Width: 'AUD_BCLK'

	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.000	1.000	4.000	Port Rate	AUD_BCLK	Rise	AUD_BCLK
2	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[0]
3	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[1]
4	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[2]
5	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|counter_r[3]
6	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_daclrck
7	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
8	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
9	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
10	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
11	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
12	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
13	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
14	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
15	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
16	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
17	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
18	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
19	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
20	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
21	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
22	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
23	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[
24	-1.000	1.000	2.000	Min Period	AUD_BCLK	Rise	Top:top0|AudDSP:dsp0|prev_data_r[

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Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-47.640	0.173	N/A	N/A	-3.210
1	AUD_BCLK	-47.640	0.196	N/A	N/A	-3.210
2	CLOCK_50	N/A	N/A	N/A	N/A	9.400
3	pll0|altpll_0|sd1|pll7|clk[0]	80.641	0.182	N/A	N/A	41.374
4	pll0|altpll_0|sd1|pll7|clk[1]	-6.016	0.173	N/A	N/A	4999.689
2	Design-wide TNS	-2687.177	0.0	0.0	0.0	-275.983
1	AUD_BCLK	-1265.137	0.000	N/A	N/A	-275.983
2	CLOCK_50	N/A	N/A	N/A	N/A	0.000
3	pll0|altpll_0|sd1|pll7|clk[0]	0.000	0.000	N/A	N/A	0.000
4	pll0|altpll_0|sd1|pll7|clk[1]	-1422.040	0.000	N/A	N/A	0.000

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Unconstrained Paths

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	29	29
4	Unconstrained Input Port Paths	1071	1071
5	Unconstrained Output Ports	99	99
6	Unconstrained Output Port Paths	1546	1546

7. 問題與心得

1. 這次Lab用到比較多protocol, 像是I2C和I2S, 以及我們最後沒做出來的LCD, 都需要去了解傳輸或接收data的方式與限制。

2. 在寫DSP的時候, 要確保是左聲道時, 才傳輸訊號, 不然可能導致出去的訊號有雜訊。
3. 在top 的module 有許多重要的控制訊號, 如果沒有小心處理, 可能會導致各個模組都沒辦法運作。

4. 此外, 有時候常常會遇到, 同一份code 燒錄到FPGA上, 卻有不同的結果, 導致 debug 困難。但透過這次的lab也讓我們有很多機會練習。
5. 在寫I2C Initializer時, 因為很不了解這個protocol在幹嘛, 所以翻了很多參考資料, 最後才知道原來要怎麼設定sclk, sdat和o_en以進行start, send, acknowledge等步驟, 但就算都挺懂這些流程了, 前幾次寫完及修改程式後, 燒到FPGA上卻還是跑不了, 導致後續的錄音、播放等功能都不能測試, 經過好幾次的trial and error才成功, 但也曾一度遇上有時可以, 有時卻不行Initialize的情形, 因此光寫好I2C Initializer的時間大概比把recorder和player寫完的時間還久。