DSD Final Project Scores

1. BrPred

(1) Total execution cycles of given I_mem_BrPred:

截圖: 2187.25ns

```
------------------------- Simulation FINISH !!-------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
$finish called from file "Final_tb.v", line 159.
$finish at simulation time             2187250
          V C S   S i m u l a t i o n   R e p o r t
Time: 2187250 ps
CPU Time:      1.100 seconds;       Data structure size:   6.7Mb
Sat Jun 17 22:38:36 2023
CPU time: 3.676 seconds to compile + 1.271 seconds to elab + 1.002 seconds to l
```

(2) Total execution cycles of given I_mem_hasHazard:

截圖:12197.25ns

```
------------------------- Simulation FINISH !!-------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
$finish called from file "Final_tb.v", line 159.
$finish at simulation time            12197250
          V C S   S i m u l a t i o n   R e p o r t
Time: 12197250 ps
CPU Time:      2.710 seconds;       Data structure size:   6.7Mb
Sat Jun 17 22:40:28 2023
CPU time: 3.733 seconds to compile + 1.237 seconds to elab + .988 seconds to l
```

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um^2)

323390-238545.8 = 84844.2

2. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um^2)

截圖:

335525 - 238545.8 =96979.2

```
Number of ports:                         4210
Number of nets:                         26301
Number of cells:                        22224
Number of combinational cells:          17513
Number of sequential cells:              4609
Number of macros/black boxes:               0
Number of buf/inv:                       4239
Number of references:                      13

Combinational area:             194975.243238
Buf/Inv area:                    35243.116314
Noncombinational area:          140549.809401
Macro/Black Box area:                0.000000
Net Interconnect area:         2985281.888550

Total cell area:                335525.052639
Total area:                    3320806.941188
```

```
Number of ports:                         1525
Number of nets:                         20932
Number of cells:                        19848
Number of combinational cells:          15955
Number of sequential cells:              3887
Number of macros/black boxes:               0
Number of buf/inv:                       4392
Number of references:                     131

Combinational area:             132078.088698
Buf/Inv area:                    24332.229115
Noncombinational area:          106467.716045
Macro/Black Box area:                0.000000
Net Interconnect area:         2436525.900848

Total cell area:                238545.804743
Total area:                    2675071.705591
```

(2) Total Simulation Time of given I_mem_compression: (ns)

截圖:2081.25ns

```
--------------------------- Simulation FINISH !! ---------------------------
==============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

==============================================================================
$finish called from file "Final_tb.v", line 159.
$finish at simulation time              2081250
           V C S   S i m u l a t i o n   R e p o r t
Time: 2081250 ps
CPU Time:      1.470 seconds;       Data structure size:   6.7Mb
Mon Jun 12 19:12:29 2023
CPU time: 1.523 seconds in simulation
```

(3) Area*Total Simulation Time: (um^2 * ns)

335525 * 2081.25 = 698,311,406

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

4.5ns

3. Q_sort

(1) Area: (um^2)

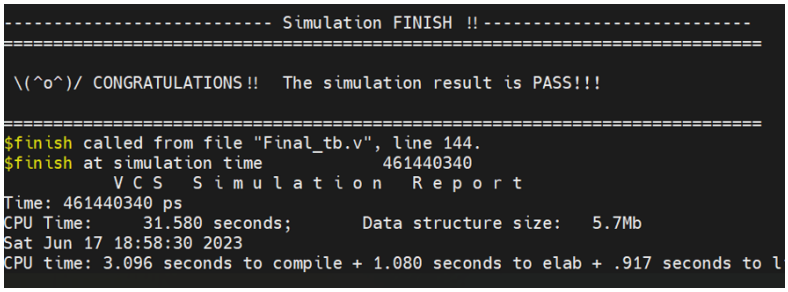
截圖:

```
Number of ports:                         1557
Number of nets:                         20239
Number of cells:                        18598
Number of combinational cells:          13989
Number of sequential cells:              4475
Number of macros/black boxes:               0
Number of buf/inv:                       3006
Number of references:                     161

Combinational area:             137514.860442
Buf/Inv area:                    20058.175772
Noncombinational area:          132996.379370
Macro/Black Box area:                0.000000
Net Interconnect area:         2549319.700989

Total cell area:                270511.239812
Total area:                    2819830.940800
```

(2) Best Total Simulation Time : (ns)

(either using compressed or uncompressed instructions)

截圖:



(3) Area*Total Simulation Time: (um^2 * ns)

270511 * 461440.3 = 1.248*E11

(4) Clock cycle for post-syn simulation (cycle in testbench, not cycle in sdc): (ns)

3.05