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Assignment 2

1.a) by adding a data buffer register on the master side of the bus, 4 bits of information can be sent over the bus at a time as packets and then reassembled at the master side.

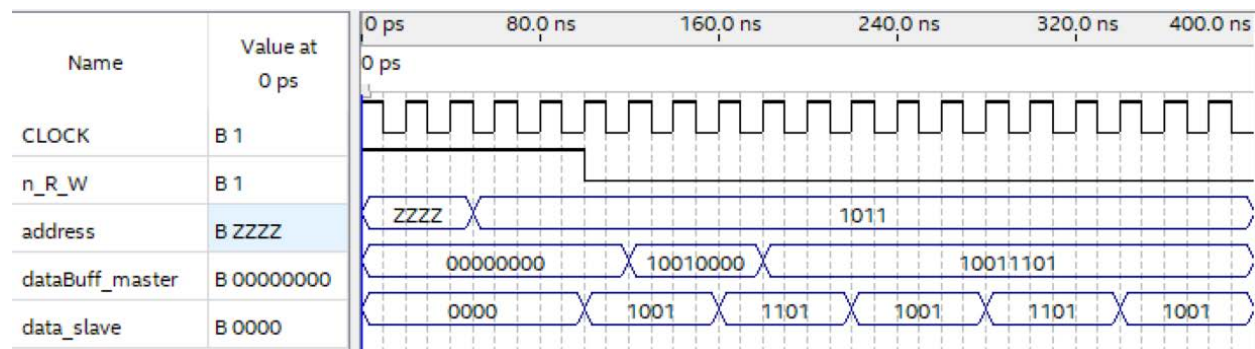| Name	Value at 0 ps							
CLOCK	B 1							
n_R_W	B 1							
address	B ZZZZ	ZZZZ				1011		
dataBuff_master	B 00000000	00000000		10010000			10011101	
data_slave	B 0000	0000		1001	1101	1001	1101	1001

Figure 1: Waveform for synchronous 4 bit bus

For asynchronous, a data buffer register is also added to the master side and an acknowledge line is put so that the master knows when to read from the data line and append it to the buffer register.

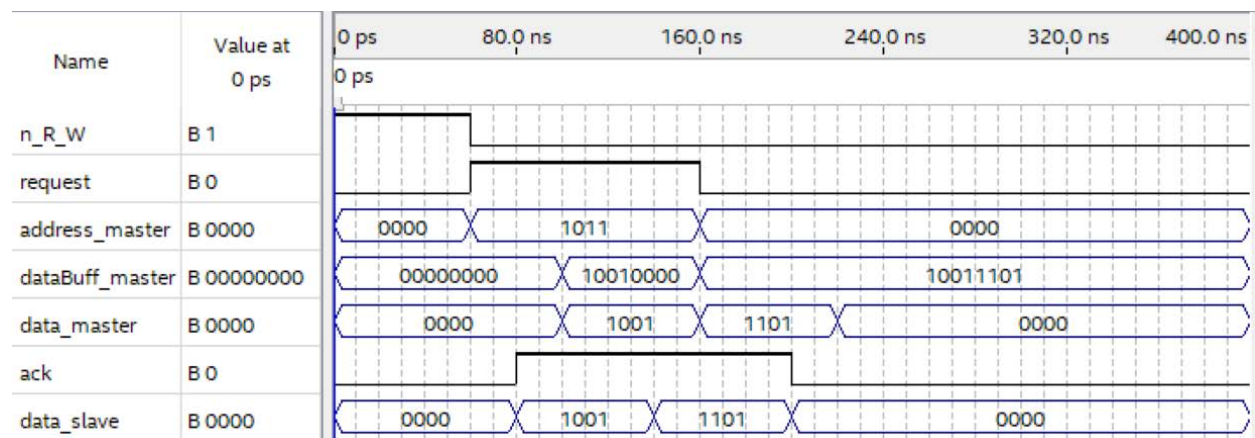| Name	Value at 0 ps					
n_R_W	B 1					
request	B 0					
address_master	B 0000	0000	1011			0000
dataBuff_master	B 00000000	00000000	10010000			10011101
data_master	B 0000	0000	1001	1101		0000
ack	B 0					
data_slave	B 0000	0000	1001	1101		0000

Figure 2: Waveform for asynchronous 4 bit bus

1.b) By asserting the second address as the first set of data is being read, the two operations can be done simultaneously instead of waiting for one full read to complete one after another. Staggering or pipelining these operations is able to accelerate the multiple operations.

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2.

Synchronous: Serial Peripheral Interface (SPI)

Asynchronous: Universal Asynchronous Receive/Transmit (UART)

3.

```
low_freq = 50;
hi_freq = 60;
sampling_freq = 400;
bound = [low_freq,hi_freq].*2/400;
b = fir1(50,bound,'stop');
fvtool(b,1);
```
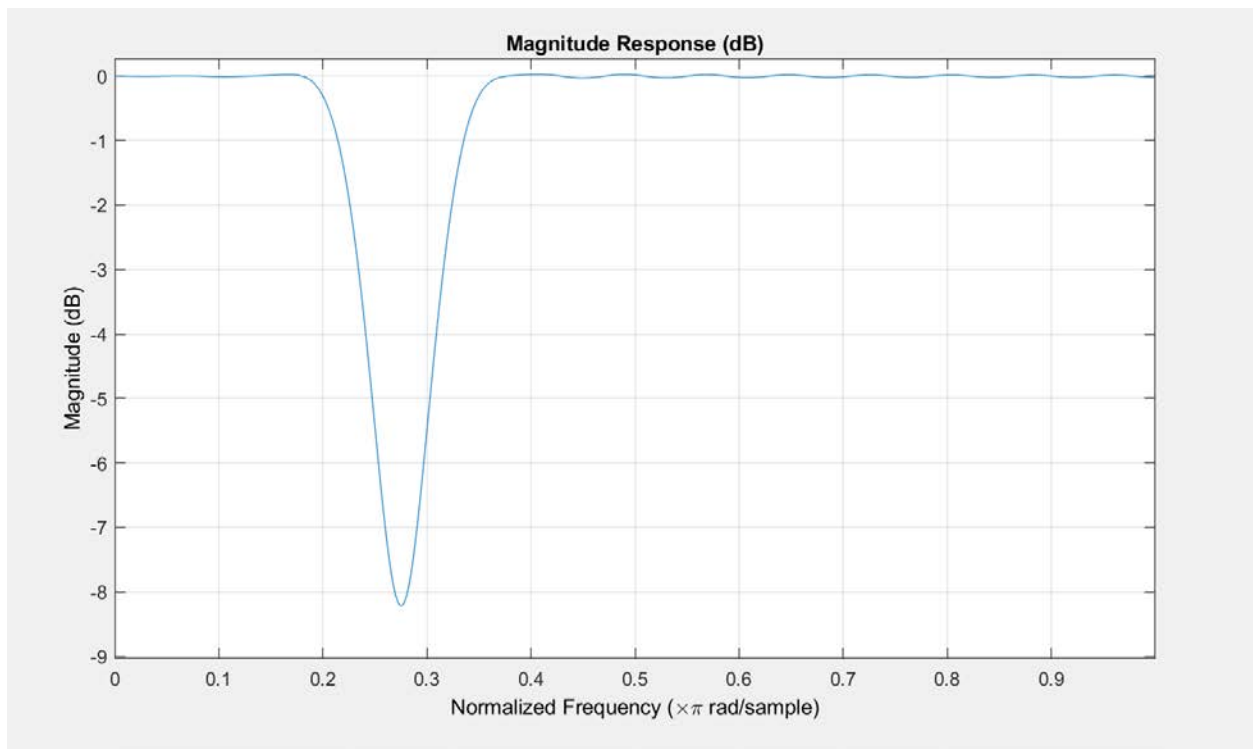

Figure 3: Frequency response of notch fitler