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**ass1.v**

module ass1(

input clk, reset,left, right,

output LA, LB, LC, RA, RB, RC

);

//All trigers are highs

reg L,R;

light right\_light(clk,R,RA,RB,RC);

light left\_light(clk,L,LA,LB,LC);

always @(posedge clk or posedge reset)

begin

if (reset) begin

L <= 1'b0;

R <= 1'b0;

end else begin

if (left == 1'b1) begin

L <= 1'b1;

R <= 1'b0;

end else if (right == 1'b1) begin

L <= 1'b0;

R <= 1'b1;

end

end

end

endmodule

**light.v**

module light(

input clk, enable,

output reg A, B, C

);

reg [1:0] light\_state;

always @(posedge clk)

begin

if (enable) begin

case (light\_state)

2'b01: begin

A <= 1'b1;

B <= 1'b0;

C <= 1'b0;

light\_state <= 2'b10;

end

2'b10: begin

A <= 1'b1;

B <= 1'b1;

C <= 1'b0;

light\_state <= 2'b11;

end

2'b11: begin

A <= 1'b1;

B <= 1'b1;

C <= 1'b1;

light\_state <= 2'b01;

end

default: begin

A <= 1'b0;

B <= 1'b0;

C <= 1'b0;

end

endcase

end else begin

A <= 1'b0;

B <= 1'b0;

C <= 1'b0;

end

end

endmodule