Assignment 2

1.a) by adding a data buffer register on the master side of the bus, 4 bits of information can be sent over the bus at a time as packets and then reassembled at the master side.

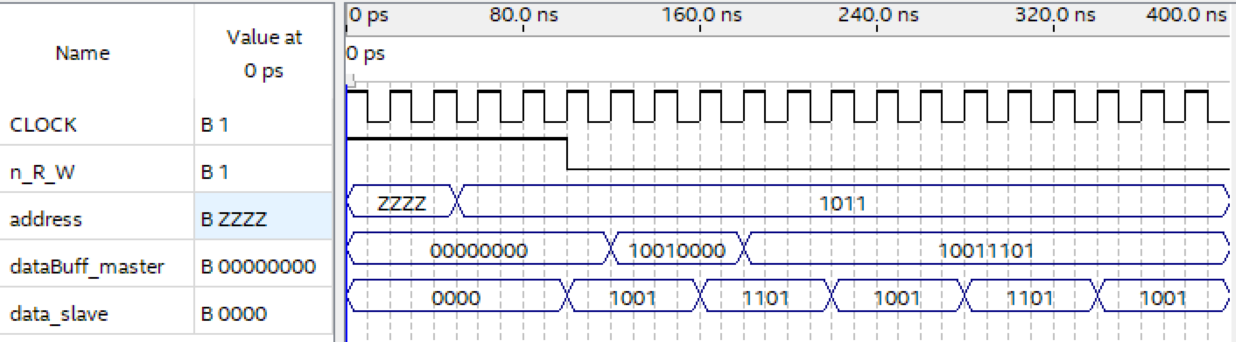


Figure 1: Waveform for synchronous 4 bit bus

For asynchronous, a data buffer register is also added to the master side and an acknowledge line is put so that the master knows when to read from the data line and append it to the buffer register.

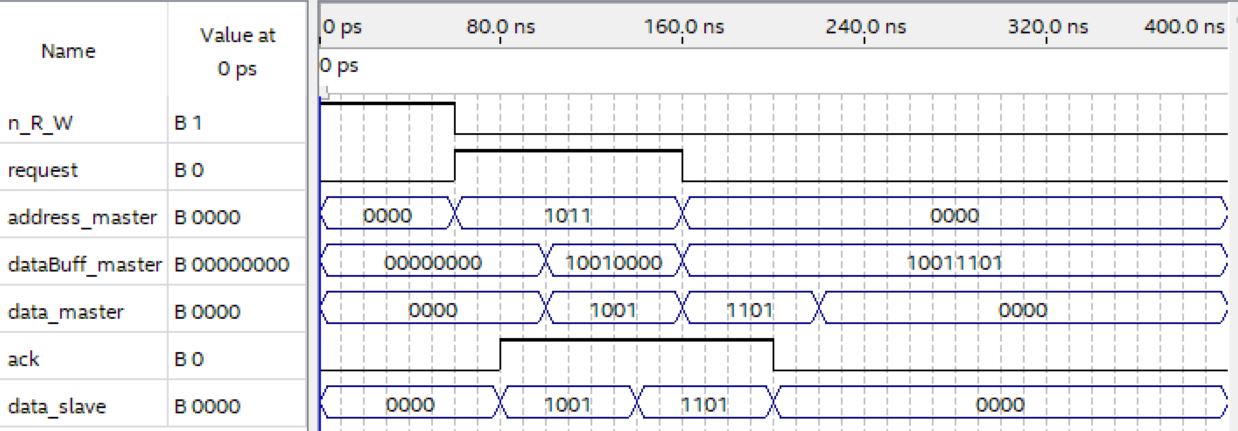


Figure 2: Waveform for asynchronous 4 bit bus

1.b) By asserting the second address as the first set of data is being read, the two operations can be done simultaneously instead of waiting for one full read to complete one after another. Staggering or pipelining these operations is able to accelerate the multiple operations.

2.

Synchronous: Serial Peripheral Interface (SPI)

Asynchronous: Universal Asynchronous Receive/Transmit (UART)

3.

low\_freq = 50;

hi\_freq = 60;

sampling\_freq = 400;

bound = [low\_freq,hi\_freq].\*2/400;

b = fir1(50,bound,'stop');

fvtool(b,1);

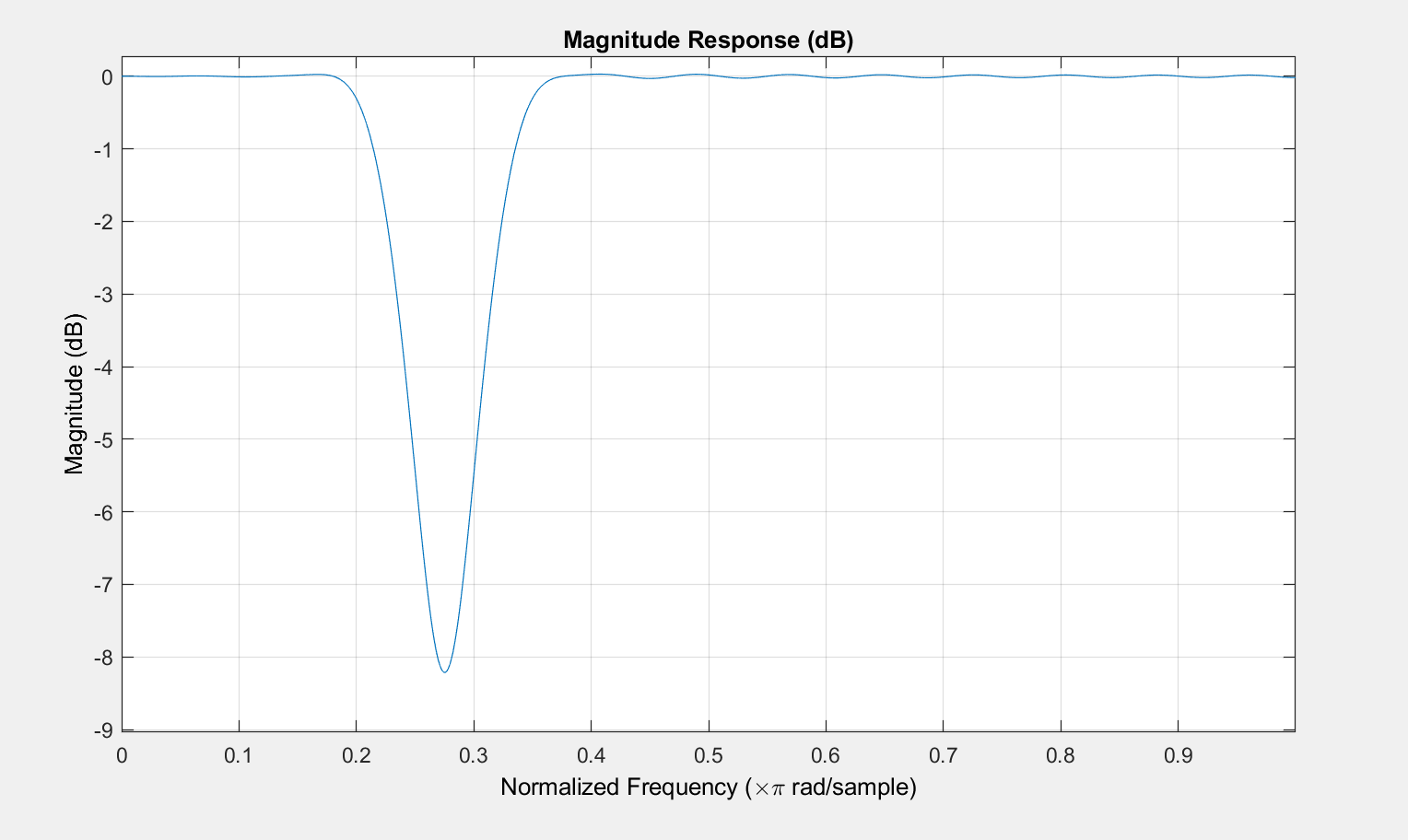


Figure 3: Frequency response of notch fitler