

Recitation #11

ENEE 313: Introduction to Device Physics

Fall, 2018

1 Week Notes Summary

Summary for preparation of 2nd mid-term exam.

1. PN junction
 - (a) built-in potential
 - (b) width of depletion region
 - (c) diode capacitance
 - (d) diode current equation
2. Generation/Recombination effects: Understand the Shockley-Read-Hall recombination equation.
3. MOS capacitors
 - (a) bulk potential of semiconductor of MOSFET
 - (b) width of MOSFET depletion region (maximum)
 - (c) Minimum capacitance
 - (d) threshold voltage for ideal and non-ideal MOSFET
4. MOS transistors Current formulas
 - (a) linear region
 - (b) saturation region

Exercise 1. Ideal PN junction

Given a Si PN junction, if the bulk resistivity of Si is $1\Omega m$,

1. find the built-in potential for the Si PN junction at room temperature
2. find the width of depletion region if the applied voltage is $1V$
3. find the maximum electric field in condition of the applied voltage is $1V$

4. What is the capacitance of the junction when the applied voltage $1V$, given the junction cross sectional area is $0.01cm^2$?
5. if the N-side has a resistivity $1\Omega m$, what should be the resistivity of the P-side so that 99% of the total width of the space charge region would be located in the N-side?
6. At room temperature under the forward bias of $0.15 V$ the current through the PN junction is $1.66 mA$. What will be the current through the junction under reverse bias?
7. Now, if we heavily doped the junction with Boron so that it become a $p^+ - n$ junction whose reverse current at room temperature is $0.9 nA/cm^2$, calculate the minority-carrier lifetime.

Note that Silicon's $\mu_n = 1500cm^2/Vs$, $\mu_p = 500cm^2/Vs$ and $n_i = 10^{10}cm^{-3}$

Solution. The built-in potential is

$$\phi_{bt} = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right)$$

To find N_a and N_d , we need to apply the fact that, on N side, $n_i \ll n \approx N_d$; on P side, $n_i \ll p \approx N_a$. Therefore, at the quasi-neutral region of both P side and N side,

$$\begin{aligned}\sigma_n &= q\mu_n n \\ \rightarrow N_d &\approx n = \frac{\sigma_n}{q\mu_n} \\ \rightarrow N_d &= 4.17 \times 10^{17} cm^{-3}\end{aligned}$$

$$\begin{aligned}\sigma_p &= q\mu_p p \\ \rightarrow N_a &\approx p = \frac{\sigma_p}{q\mu_p} \\ \rightarrow N_a &= 1.25 \times 10^{18} cm^{-3}\end{aligned}$$

Thus, $\phi_{bt} = 0.88V$.

To calculate the depletion region width,

$$x_{sc} = \sqrt{\frac{\epsilon(\phi_{bt} - V)}{q} \left(\frac{N_a N_d}{N_a + N_d}\right)} = 1.58\mu m$$

The electric field comes from, on P side,

$$E(x) = \frac{q}{\epsilon} N_a (x_p - x), 0 \leq x \leq x_p$$

So, the maximum electric field is,

$$E_{max} = E(0) = 7.58 \times 10^4 V/cm$$

where $x_p = x_{sc}N_d/(N_d + N_a)$

The capacitance of the junction is

$$C = \frac{\epsilon}{x_s c} = 6.6 \times 10^{-7} Fd/cm^2$$

$$C_{PN} = C \times area = 6.6nF$$

Since $\frac{x_p}{x_n} = \frac{N_d}{N_a}$, $x_n = 0.99x_{sc}$ and $x_p = 0.01x_{sc}$, we have $N_a = 99N_d$. Furthermore, the resistivity of the N-side is $1\Omega m$, we have

$$n = \frac{1}{q\mu_n\rho} = 4.17 \times 10^{13} cm^{-3}$$

Therefore, $N_a = 99N_d \approx 99n = 4.12 \times 10^{15} cm^{-3}$

According to the diode current equation,

$$I(V) = I_0 \exp\left(\frac{-qV}{kT} - 1\right)$$

Since $I(0.15) = 1.66mA$, we have $I_0 = 1.7\mu A$

The reverse current of a $p^+ - n$ junction is

$$I_0 = \frac{qD_p n_i^2}{N_d L_p} = \frac{q n_i^2}{N_d} \sqrt{\frac{D_p}{\tau_p}}$$

Since $\mu = qD/kT$, we can obtain $\tau_p = 0.66ps$

□

Exercise 2. MOS capacitor and transistors

For an ideal $SiO_2 - Si$ MOS capacitor on p substrate at room temperature with $d = 10nm$, $N_a = 5 \times 10^{17} cm^{-3}$, and dielectric permittivities of Si and SiO_2 are 11.8 and 3.9.

1. Find the applied voltage at the interface required to make the silicon surface intrinsic
2. Again, Find it to bring about a strong inversion
3. Find the turn-on(threshold) voltage under high-frequency condition
4. Find the minimum capacitance under high-frequency regime

Solution. The applied voltage appears partially across the insulator, V_i and the semiconductor, ϕ_s is

$$V = V_i + \phi_s$$

The voltage across the insulator is

$$V_i = \frac{-Q_s}{C_i}, \text{ where } C_i = \frac{\epsilon_i}{d}$$

If the voltage across the semiconductor is less than the one needed to bring about a strong inversion, Q_s is

$$Q_s = -qN_aW, \text{ where } W = \sqrt{\frac{\epsilon_s\phi_s}{qN_a}}$$

Thus, we have

$$V = \phi_s + \frac{d}{\epsilon_i} \sqrt{q\epsilon_s N_a \phi_s}$$

To make the surface intrinsic, we need

$$\phi_s = \phi_F = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)$$

To make the surface strong inversion, we need

$$\phi_s = 2\phi_F = 2\frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)$$

where ϕ_F is the bulk potential of the semiconductor. Therefore, the surface becomes intrinsic when $V = 1.03V$; strong inversion when $V = 1.73V$.

To find the minimum capacitance, we already have C_i and need to find C_d , which is $C_d = \frac{\epsilon_s}{W_{max}}$. W is the maximum width of the depletion region.

$$W_{max} = \sqrt{\frac{2\epsilon_s 2\phi_F}{qN_a}} = 4.9\mu m$$

Thus, $C_d = 0.21\mu F$. We know $C_i = \frac{\epsilon_i}{d} = 0.34\mu F$. By the minimum capacitance formula,

$$C_{min} = \frac{C_i C_d}{C_i + C_d} = 0.13\mu F$$

On the other hand, since $V_{TH} = 2\phi_F - \frac{Q_d}{C_i}$ and $Q_d = -qN_aW_{max}$, we have $V_{TH} = 2.05V$ □

Exercise 3. SRH recombination

An N type Silicon substrate with $N_d = 7 \times 10^{15} cm^{-3}$ contains the trap energy level located at the Fermi level and the relaxation time $\tau = 10^{-7} s$.

1. Calculate the recombination rate if n and p are much lower than the equilibrium value
2. if only p is less than n_i , what's the recombination rate?

Solution. According to the SRH recombination equation,

$$R = \frac{1}{\tau} \frac{np - n_i^2}{n + p + 2n_i \cosh\left(\frac{E_t - E_F}{kT}\right)}$$

And the trap energy level locates at the Fermi level. If $n < n_i$ and $p < n_i$, we have

$$R = \frac{1}{\tau} \frac{np - n_i^2}{n + p + 2n_i \cosh(\frac{E_t - E_F}{kT})} = -\frac{n_i}{2\tau} = -5.3 \times 10^{16} \text{cm}^{-3}/s$$

Since $p < n_i$, $n \approx N_d \gg n_i$,

$$R = -\frac{n_i^2}{\tau N_d} = -1.4 \times 10^{11} \text{cm}^{-3}$$

□