

Alexander Hankin

Curriculum Vitae

Contact Information

Email: alexander.hankin@tufts.edu

EDUCATION

Ph.D., M.S. Electrical Engineering
Tufts University, Medford, MA, USA
Advisor: Prof. Mark Hempstead

expected 2021, 2017

B.S. Computer Engineering
Tufts University, Medford, MA, USA

2016

PUBLICATIONS

L. Pentecost*, **A. Hankin***, M. Donato, M. Hempstead, G. Y. Wei, and D. Brooks (***joint first authors**), “NVMEplorer: A Framework for Cross-Stack Comparisonsof Embedded Non-Volatile Memory Solutions,” **under review at MICRO 2021**.

A. Hankin, D. Werner, J. Sebot, K. Vaidyanathan, M. Amiraski, and M. Hempstead, “HotGauge: A Methodology for Characterizing Hotspots in Next Generation Processors,” **under review at MICRO 2021**.

A. Hankin and M. Hempstead, “Proposal for a Timing Model of Ion Trap Quantum Architectures,” *to appear in I too can Quantum! at ISCA 2021*.

A. Hankin, M. Amiraski, K. Sangaiah, and M. Hempstead, “Toward Faster and More Efficient Training on CPUs Using STT-RAM-based Last Level Cache,” 12th Annual Non-Volatile Memories Workshop (NVMW), San Diego, CA, USA, 2021.

A. Hankin, T. Shapira, K. Sangaiah, M. Lui and M. Hempstead, “Evaluation of Non-Volatile Memory Based Last Level Cache Given Modern Use Case Behavior,” 2019 IEEE International Symposium on Workload Characterization (IISWC), Orlando, FL, USA, 2019, pp. 143-154, doi: 10.1109/IISWC47752-2019.9042051.

PROFESSIONAL EXPERIENCE

Teaching and Research Assistant
Tufts University

June 2017 - Present
Medford, MA, USA

Research Intern
Intel

June 2020 - Aug 2020
Hillsboro, OR, USA

Research Intern
Google

Jan 2019 - July 2019
Mountain View, CA, USA

TEACHING EXPERIENCE

Tufts University

Medford, MA, USA

Teaching Assistant, Advanced Computer Architecture

Spring 2021

Teaching Assistant, Electronics

Spring 2020

Teaching Assistant, Object-Oriented Programming for Graduate Students

Fall 2019

Teaching Assistant, Advanced Computer Architecture

Spring 2019

Teaching Assistant, Computer Engineering

Fall 2018

CONFERENCE TALKS

“Evaluation of Non-Volatile Memory Based Last Level Cache Given Modern Use Case Behavior,” 2019 IEEE International Symposium on Workload Characterization (IISWC), Orlando, FL, USA, 2019.

WORKSHOP TALKS

“Proposal for a Timing Model of Ion Trap Quantum Architectures,” *to happen at I too can Quantum! at ISCA 2021*.

POSTER PRESENTATIONS

“Toward Faster and More Efficient Training on CPUs Using STT-RAM-based Last Level Cache,” 12th Annual Non-Volatile Memories Workshop (NVMW), San Diego, CA, USA, 2021.