CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
ITT204	COMPUTER ORGANIZATION	PCC	3	1	0	4

Preamble

This syllabus has been prepared to meet the following objectives.

1. To impart an understanding of the internal organization and operations of a computer.
2. To introduce the concepts of processor logic design.
3. To introduce the concept of pipe-lining and its hazards.
4. To understand and analyze various issues related to memory hierarchy.
5. To introduce the various modes of data transfer between CPU and I/O devices.

Prerequisite: ITT201 Digital System Design

Course Outcomes: After the completion of the course the student will be able to

CO No	Course Outcome(CO)	Bloom's Category
CO 1	Describe the basic organization of computer and different instruction formats and addressing modes.	Understand
CO 2	Analyze the basic operations and sequencing of control signals	Analyze
CO 3	Represent the design of registers and arithmetic logic unit	Understand
CO 4	Examine the concept of pipe-lining and various hazards associated with it	Analyze
CO 5	Compare the performance of memory systems like cache and DRAM and Select appropriate interfacing standards for I/O devices.	Analyze

Mapping of course outcomes with program outcomes

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	-	-	-	-	-	-	-	-	1	1
CO2	3	3	3	2	-	-	-	-	-	-	1	1
CO3	3	2	3	-	-	-	-	-	-	-	1	1
CO4	3	3	3	3	2	-	-	-	-	-	1	2
CO5	3	3	3	3	1	-	-	-	-	-	1	2

3/2/1: high/medium/low

Assessment Pattern

Bloom's Category	Continuous Assessment Test		End-Semester Examination
	1	2	
Remember	12	8	16
Understand	10	12	24
Apply	20	20	40
Analyse	8	10	20
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance : 10 marks
Continuous Assessment Test (2 numbers) : 25 marks
Assignment/Quiz/Course project : 15 marks

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks.

Sample Course Level Assessment Questions

Course Outcome 1 (CO1):
1.Explain the importance of different addressing modes in computer architecture with suitable example
2.How is the operation X = (A + B) * (C + D) / (E+F) is performed using:
a) Three address instruction
b) Two address instruction
c) One address instruction

Course Outcome 2 (CO2):

1. Enumerate the sequence of actions involved in executing an unconditional branch instruction.
2.Write down the sequence of actions needed to fetch and execute the instruction:
Store R6, X(R8).

Course Outcome 3 (CO3):

1.Draw the block diagram for the hardware that implements the following statement x + yz: AR ← AR + BR where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function. (The symbol + designates an OR operation in a control or Boolean function and an arithmetic plus in a micro operation.)
2. Illustrate the difference in performance of an Arithmetic Right Shifter & a Logical Right Shifter

Course Outcome 4 (CO4):

1.A5-stage pipelined processor has Instruction Fetch(IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
I1 :MUL R2 ,R0 ,R1	R2 = R0 *R1
I1 :DIV R5 ,R3 ,R4	R5 = R3/R4
I2 :ADD R2 ,R5 ,R2	R2 = R5+R2
I3 :SUB R5 ,R2 ,R6	R5 = R2-R6

2. The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. How many clock cycles are required for completion of execution of the sequence of instruction?

Course Outcome 5 (CO5):

1. A computer has a 256 KByte, 4-way set associative, write-back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. How many bits are there in the tag,set and word field of an address?
2. Discuss DRAM scheduling policies.

Course Outcome 6 (CO6):

1. What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt? What is asynchronous data transfer? Explain in detail.
2. Explain the working of Universal Serial Bus (USB).

Model Question Paper

PART A **(10*3=30)**

(Each question carries 3 Marks)

1. What are fundamental phases of the instruction cycle?
2. The register R1 = 12, and R2= 13. The instruction ADD R1, R2 is in memory location 2000H. After the execution of the instruction, what will be the value of PC, MAR, IR and R1?.
3. What do you meant by logic micro operations?
4. Design a 4bit combination logic shifter.
5. "Increasing the number of pipeline stages will decrease the execution time of the program". True or False? Justify your answer.
6. What is operand forwarding? What is its significance?
7. For a 16KB, 4-way associative cache with block size 16 bytes, what is the number of tag bits per block if the physical address capacity is 16MB?
8. List the advantages of memory interleaving
9. Compare Polling and Vectored Interrupts.
10. What is DMA? What do you meant by Burst mode?

PART B **(5*14=70)**

(Each full question carries 14 marks)

11.a) Discuss the sequencing of control signals for the following instructions.

i) Load R1,10(R2) ii) Add R1, R2 (8 marks)

b) Compare and contrast memory mapped IO over programmed IO. (6 marks)

OR

12.a) Illustrate with example, explain the different types of addressing modes in a RISC processor. (9 marks)

b) Discuss how stack used for subroutine call. (5 marks)

13.a) Design a 4 bit arithmetic unit with two selection variables s0 and s1 and two n-bit data inputs A&B and input carry Cin

s1	s2	Cin=0	Cin=1	
0	0	F=A	F=A+1	
0	1	F=A+B	F=A+B+1	
1	0	F=A+B'	F=A+B'+1	
1	1	F=A-1	F=A	

(9 marks)

b) Explain the design of an accumulator. (5 marks)

OR

14. a) Design an adder/subtractor circuit with one selection variable s and two inputsA and B. When s=0, the circuit performs A+B and when s=1 it performs A-B, by taking 2's complement of B. (9marks)

b) Explain the design of status register. (5 marks)

15.a) Consider an instruction pipeline with four stages with the stage delays 5 nsec, 6 nsec, 11 nsec, and 8 nsec respectively. The delay of an inter-stage register stage of the pipeline is 1 nsec. What is the approximate speedup of the pipeline in the steady state underideal conditions as compared to the corresponding non-pipelined implementation? (5 marks)

b) Discuss structural hazards and control hazards with examples (9 marks)

OR

16. a) A 5-stage pipelined processor has the stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Write Operand (WO). The IF, ID, OF, and WO stages take 1 clock cycle each for any instruction. The EX stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. Operand forwarding is used in the pipeline (for data dependency, OF stage of the dependent instruction can be executed only after the previous instruction completes EX). What is the number of clock cycles needed to execute the following sequence of instructions?

MUL R2,R10,R1
DIV R5,R3,R4
ADD R2,R5,R2
SUB R5,R2,R6 (7 marks)

b) Discuss various types data hazards in a RISC Instruction pipeline with appropriate examples. (7 marks)

17. a) Consider an application running on a multiprocessor system that takes 600 cycles, (during which processors are stalled), to handle a local cache miss leading to referencing a remote memory. The CPI for all references that hit in cache is 1 cycle. If 0.2% of cache access result in a local miss, how much faster will the system run if it has a perfect cache that never miss. (5 marks)

b) Discuss organization of DRAM in detail. (9 marks)

OR

18.a) Discuss open page and closed page row buffer management policy in DRAM Controller (9 marks)

b) Given a cell array of 8K(8192), with Clock cycle=4 and Clock Rate=133MHZ. In DRAM, the period for refreshing all rows is 16ms whereas 64ms in SDRAM. Find out the Refresh Overhead of SDRAM when compared to DRAM (5 marks)

19.a) Discus different types of interrupt handling methods (7 marks)

b) Explain the working of SCSI. (7 marks)

OR

20.a)Discuss various bus arbitration methods. (7 marks)

b) Explain the working of PCI. (7 marks)

Syllabus

Module 1 (10 hours)
Basic Structure and Operation of Computers – functional units –operational concepts – memory operations – addressing modes – instruction sequencing – basic I/O – subroutine calls – execution of a complete instruction – sequencing of control signals.
Module 2 (8 hours)
Processor Logic Design and Organization – register transfer logic – micro operations – conditional control statements. Design of arithmetic unit, logic unit, ALU and shifter – Accumulator.
Module 3 (9 hours)
RISC – RISC instruction set – pipelining – hazards and mitigation.
Module 4 (11 hours)
Memory – cache memory, mapping and performance improvement. DRAM organization. Memory controllers-scheduling
Module 5 (7 hours)
Peripheral Subsystem – I/O organization – interrupts – DMA – bus arbitration – standard I/O interfaces.

Text Books:

1. Patterson D.A. and J. L. Hennessey, Computer Organization and Design, 5/e, Morgan Kauffmann Publishers, 2013.
2. Hamacher C., Z. Vranesic and S. Zaky, Computer Organization,5/e, McGraw Hill,2011.
3. M. Morris Mano, Computer System Architecture, 3/e, Pearson Education, 2007.
4. Bruce Jacob, David T. Wang, and Spencer Ng, Memory Systems: Cache, DRAM, Disk, 1/e Morgan Kauffmann Publishers, 2007.

References:

1. William Stallings, Computer Organization and Architecture: Designing forPerformance, Pearson, 9/e, 2013.
2. Computer Architecture: Pipelined and Parallel Processor Design M.J. Flynn Published byNarosa Publishing House, 2012
3. Rajaraman V. and T. Radhakrishnan, Computer Organization and Architecture,Prentice Hall, 2011.
4. Messmer H. P., The Indispensable PC Hardware Book, 4/e, Addison-Wesley, 2001

Course Content & Lecture Schedule

Module 1: Fundamentals of Computer Organization		**10 hours**
1.1	Basic Structure of computers–functional units –basic operational concepts –bus structures –software.	**2 hours**
1.2	Memory locations and addresses –memory operations – instructions and instruction sequencing – addressing modes – ARM Example (programs not required).	**4 hours**
1.3	Basic I/O operations –stacks, subroutine calls. Basic processing unit – fundamental concepts –instruction cycle - execution of a complete instruction – multiple-bus organization –sequencing of control signals.	**4 hours**
Module 2:Processor Logic Design		**8 hours**
2.1	Register transfer logic –inter register transfer – arithmetic, logic and shift micro operations –conditional control statements.	**4 hours**
2.2	Design of arithmetic unit, logic unit, arithmetic logic unit and shifter – status register –processor unit –design of accumulator.	**4 hours**
Module 3: RISC Instruction Pipelining		**9 hours**
3.1	Introduction to RISC instruction set, load store architecture	**3 hours**
3.2	Overview of pipelining, pipelined datapath and control	**2 hours**
3.3	Pipeline hazards, hazard mitigation techniques.	**4 hours**
Module 4: Memory system : Cache & DRAM		**11 hours**
4.1	Introduction to cache memory, cache mapping, block replacement techniques, measuring and improving cache performance .	**4 hours**
4.2	Introduction to DRAM system, DRAM organization-Memory interleaving.	**2 hours**
4.3	Memory controllers, Address mapping, DRAM Scheduling policies, Row Buffer management policies- DRAM Refreshing	**5 hours**

	Module 5: Peripheral Subsystem	**7 hours**
5.1	I/O organization: accessing of I/O devices –interrupts	**2 hours**
5.2	Direct memory access –buses –bus arbitration	**2 hours**
5.3	Interface circuits –standard I/O interfaces (PCI, SCSI, USB)	**3 hours**