Chamber and Recipe-Independent FDC Indicator in High-Mix Semiconductor Manufacturing

Satoshi Yasuda, Tomoya Tanaka, Masaki Kitabata, and Yuko Jisaki

***Abstract*—This paper describes a chamber and recipe-independent fault detection and classification (FDC) indicator using the example of aluminum sputtering tools. We developed this indicator to detect abnormal discharge in an aluminum sputtering chamber when using a legacy FDC system. Abnormal discharge has several modes in the sputtering chamber, with abnormal discharge to a wafer commonly causing pattern defects. The indicator has been improved to detect only this problem, and to minimize the impact of false alarms that cause a loss of equipment productivity. The indicator can be readily extended to new chambers and the control limits are easily set for all recipes. This is because the equation for the indicator is very simple, and both the equation and the control limits are common to all sputtering chambers and recipes. It can therefore significantly reduce the setup work required of engineers, which is one of the biggest challenges in high-mix semiconductor manufacturing. The indicator is easily applied to newly installed tools at start of production and restrains the number of scrap wafers at minimum level. We also describe the mechanism of trace data changes in abnormal discharge modes using equivalent electrical circuits.**

***Index Terms*—Abnormal discharge, aluminum sputtering, arcing, fault detection and classification (FDC), high-mix production, indicator, pattern defects, semiconductor manufacturing.**

I. Introduction

IN SEMICONDUCTOR manufacturing, fault detection and classification (FDC) is essential to achieve high quality and high efficiency. In high-mix production foundries, FDC is required to be adopted at start of production in newly installed equipment and newly increased process recipes. However, even for the same FDC parameters, values tend to differ between chambers due to individual differences in the sensors, the parts, and their exact positions in the chamber. Moreover, most FDC data varies according to process recipe. This requires a great deal of time and effort on the part of engineers to optimize the FDC control limits for individual chambers and recipes. To solve this challenge, several statistical strategies have been proposed to develop an indicator that is independent of the chamber or recipe (e.g., [1], [2]). It is not practical to adopt FDC based on statistical models in actual production lines if the results cause numerous false alarms that reduce productivity. Even if the false alarms can be reduced, it is still difficult to apply statistical models because identifying the nature of the failure is time-consuming, leading to loss of productivity. In mass production fabrication lines, FDC should be implemented 24 hours a day, 365 days a year. To realize this, manufacturing section operatives need to be able to judge whether a given fault detected by FDC is real or not. If they are unsure, they have to wait for an engineer. This process reduces the productivity of the process tool where faults are detected by FDC, especially at midnight and on holidays. Manufacturing operatives usually find it difficult to interpret the faults detected by statistical models. This situation prompted us to propose a chamber and recipe-independent FDC indicator that is linked directly to failure modes which are easily understood by manufacturing operatives. The term "chamber and recipe-independent" means that the indicator's equation and control limits are common to all chambers and all recipes. It therefore significantly reduces the demand on engineers for setting FDC control limits for newly installed tools and new recipes.

In this paper, a chamber and recipe-independent FDC indicator is described using the example of detecting abnormal discharge in an aluminum sputtering tool. In Section II, drawbacks to FDC implementation are explained and an aluminum sputtering tool with a monitoring tool and problems of abnormal discharge are illustrated. Section III describes how the FDC indicator has been developed, improved and extended to a newly installed tool. In addition to the previous report [3], the mechanism of the trace data changes in the abnormal discharge modes is described using equivalent electrical circuits. Finally, Section V contains our concluding remarks and describes our future research.

II. Implementation of FDC and the Issue

A. Fab-Wide FDC System

The primary purpose of FDC implemented in process chambers is to prevent scrap wafers. Wafer processing must be stopped immediately when a fault is detected by FDC for the chamber. We have had our own fab-wide FDC system in place since 2005 for our 300-mm fab (Fig. 1) [4]. Our system was originally developed to handle large volumes of FDC data in

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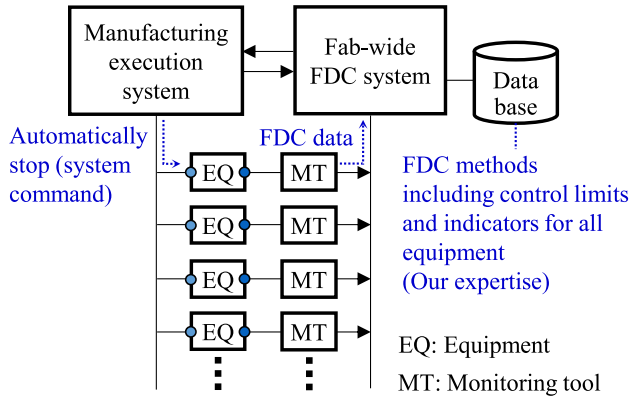


Fig. 1. Fab-wide FDC system.

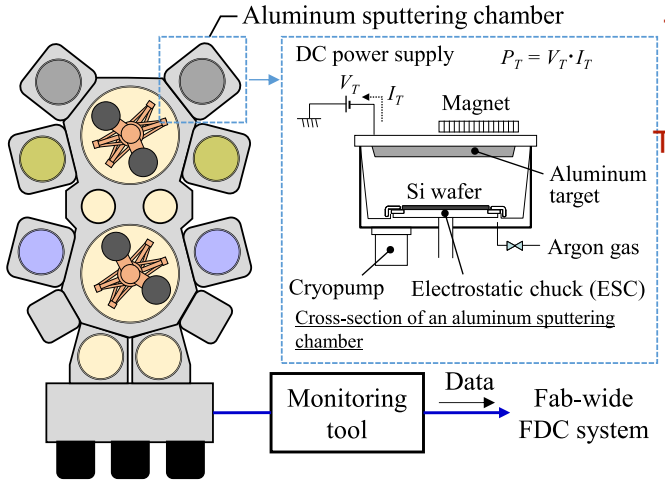


Fig. 2. Schematic drawing of an aluminum sputtering tool and a monitoring tool.

real time and to stop automatically processing the production lot when detecting a fault [5]. We have prevented the generation of huge amounts of scrap wafers by using various FDC techniques, from univariate FDC to FDC by applying virtual metrology (VM), i.e., VM-FDC [6], [7], [8], [9].

Although it is important to develop the system, it is crucial to develop and continuously improve FDC methods at the same time. Ideally, all faults should be detected before a defective wafer occurs, however, they cannot all be prevented in our fab. The key is for engineers to continuously improve the FDC methods. All the methods we developed have been accumulated in the database of the FDC system as our expertise.

B. Aluminum Sputtering Tool and Abnormal Discharge

This subsection describes an aluminum sputtering tool. The abnormal discharge problem is used to explain a case of FDC indicator development. Fig. 2 is a schematic drawing of an aluminum sputtering tool with the cross-section of a sputtering chamber and a monitoring tool. In the chamber, an aluminum target is set on the opposite side of a silicon wafer on the electrostatic chuck (ESC) on the wafer stage. After evacuating the chamber using a cryopump, argon gas is introduced into the chamber. Argon plasma is then generated by a DC

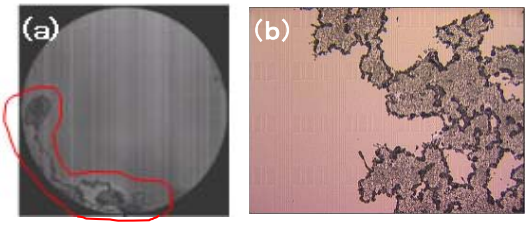


Fig. 3. (a) Pattern-defective wafer and (b) the enlarged view of the defects caused by abnormal discharge in an aluminum sputtering tool.

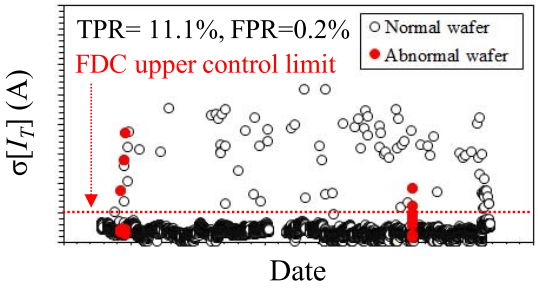


Fig. 4. Trend data for the standard deviation of the target DC current.

power supply. The power is constantly controlled. The target is sputtered by argon ions, and aluminum is deposited on the wafer. The monitoring tool collects FDC data at a sampling rate of 1 Hz. This sampling rate was recommended by the vendor when the monitoring tool was first installed. Later, the sampling rates were changed to 4Hz for some parameters as mentioned in Section III-B. The collected FDC data are the target DC power (P_T), the target DC current (I_T), the target DC voltage (V_T), and other parameters. The FDC data are sent to our fab-wide FDC system, as shown in Fig. 1. The FDC system can detect any faults in the chamber.

Fig. 3 shows pictures of a pattern-defective wafer resulting from abnormal discharge in an aluminum sputtering tool. We have implemented conventional univariate FDC using basic statistical values such as average, maximum, minimum, and standard deviation, for all process tools from the initial adoption of our fab-wide FDC. However, the defective wafers occurred because the automatic stop was not employed due to too many false alarms in spite of variations in trace data being confirmed, for example, as a change in the standard deviation of the target DC current (Fig. 4). As shown in Fig. 4, the true positive rate (TPR) is 11.1% and the false positive rate (FPR) is 0.2%. The TPR and the FPR are defined as the following equations as (1) and (2) below.

$$TPR = TP/(TP + FN) \tag{1}$$

$$FPR = FP/(FP + TN) \tag{2}$$

where TP, FP, TN, and FN stand for true positives, false positives, true negatives, and false negatives, respectively. The control limit in Fig. 4 is calculated several times the standard deviation of the data. It may also be calculated by a method using median absolute deviation and so on. The TPR of 11.1% is a low value and the FPR of 0.2% is a high value. An FDC indicator is therefore needed which is designed

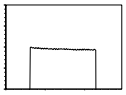
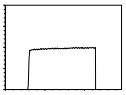
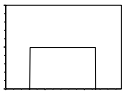
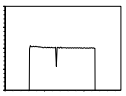
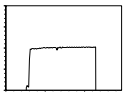
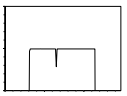
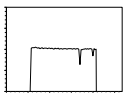
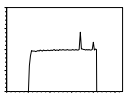
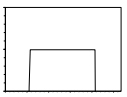
Trace data (FDC parameters vs. Process time)				Occurrence of abnormal discharge to wafer
Pattern	Target DC current (I_T) [A]	Target DC voltage (V_T) [V]	Target DC power (P_T) [W]	
A				No
B				No
C				Yes

Fig. 5. Three patterns of trace data of target DC current, voltage and power in an aluminum sputtering tool. (Sampling rate: 1 Hz.).

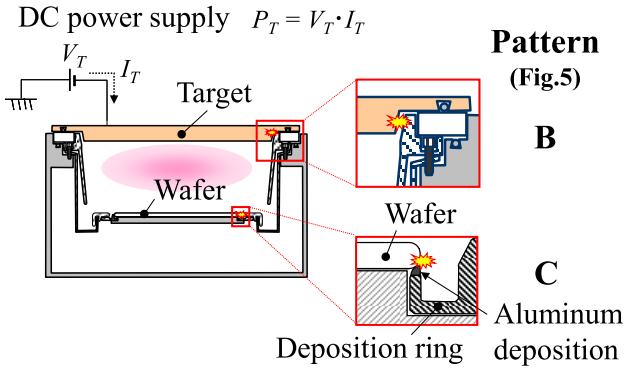


Fig. 6. Two modes of abnormal discharge in an aluminum sputtering chamber.

to be sensitive but which minimizes the impact of false alarms.

III. Development of FDC Indicator

A. Chamber and Recipe-Independent FDC Indicator

Analysis using FDC data revealed that there are two modes of abnormal discharge and the trace data of I_T, V_T, and P_T were different (Fig. 5). It was also confirmed that Patterns B and C respectively indicate the occurrences of arcing to the target and to the wafer (Fig. 6). Arcing to the wafer takes place between the edge of the wafer and the local aluminum deposition on the "deposition ring" as shown in Fig. 6.

The DC power supply is designed to turn off its own output when arcing is detected. It is thought that the DC power supply can detect arcing in Pattern B but not in Pattern C, because the arcing energy in Pattern B is larger than that in Pattern C. Therefore, a drop appears only in the data of P_T for Pattern B. We devised an FDC indicator that can detect only Pattern C as in (3) below.

$$Arcing\ Index\ 1 = \sigma\ [I_T] \cdot h_c(\sigma[P_T]) \tag{3}$$

where $h_c(x)$ is the step function as in (2),

$$h_c(x) = \begin{cases} 1, & (x < c) \\ 0, & (x \geq c) \end{cases} \tag{4}$$

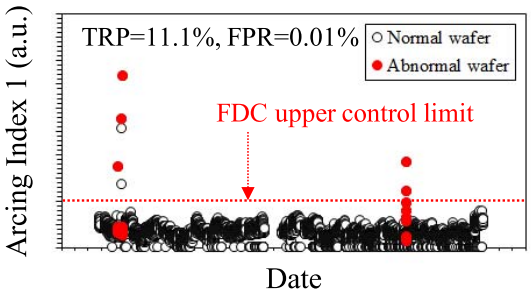


Fig. 7. Trend data for Arcing Index 1.

$\sigma[x]$ is the standard deviation of x, and c is a constant value. It is logical to use the standard deviation of I_T rather than V_T in (3), because the drop in I_T is greater than that in V_T. Fig. 7 shows the trend data of the indicator in (3). In Fig. 7, the control limit is calculated in the same way as that in Fig. 4. Since the FPR decreased from 0.2 to 0.01%, we have started the operation of the automatic stop of the processing lot when a fault is detected by Arcing Index 1 in this chamber. However, the TPR is still low.

B. Improvement of FDC Indicator

After the sampling rate had been changed from 1 to 4 Hz to improve the TPR and the indicator in (3) had been adopted in all chambers of other tools, the FPR increased to 8.3% in one of the chambers. In this case, several years after the monitoring tool were first installed, we found that 4 Hz is the maximum sampling rate for these sputtering tools without causing deterioration of data quality, such as data loss, or incurring additional costs. The maximum sampling rate depends on the processing capability of the computer in the tool and varies with each tool. Further FDC data analysis showed there to be five patterns in the trace data of I_T (Fig. 8). Patterns A, B, and C in Fig. 8 are the same as those in Fig. 5. Patterns D and E in Fig. 8 are new ones that resulted from changing the sampling rate to 4 Hz. We checked and categorized the trace data of all plots for which the value of Arcing index 1 exceeded the control limit into Pattern B to E. The instantaneous changes (drop or spike) of I_T and V_T in Pattern D are just the opposite of their changes in Pattern C. No pattern-defective wafers were found in the wafers detected as Pattern D by FDC. It appears that the drop of I_T in Pattern C occurs only with abnormal discharge to a wafer due to the high resistance of the wafer. On the other hand, it appears that the spike of I_T in Pattern D indicates abnormal discharge to a low-resistance path such as a shield, other than the wafer in the chamber. Pattern E is the mode in which the trace data of I_T and V_T show small vibration. No defective examples were found in the wafers detected as Pattern E by FDC. We therefore need to improve the indicator to detect only Pattern C, as shown in Fig. 8.

To detect Pattern C rather than Pattern D, we use the functions $f_U(x)$ and $f_L(x)$ below.

$$f_U(I_T) = Max[I_T] - Med[I_T] \tag{5}$$

$$f_L(I_T) = Med[I_T] - Min[I_T] \tag{6}$$

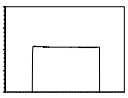
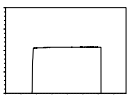
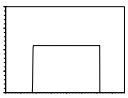
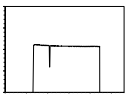
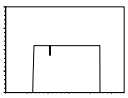
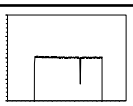
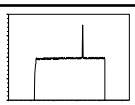
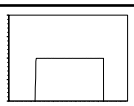
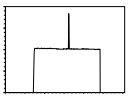
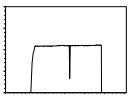
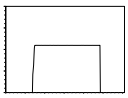
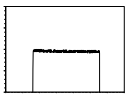
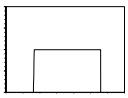
Trace data (FDC parameters vs. Process time)				Occurrence of abnormal discharge to wafer
Pattern	Target DC current (I_T) [A]	Target DC voltage (V_T) [V]	Target DC power (P_T) [W]	
A				No
B				No
C				Yes
D				No
E				No

Fig. 8. Five patterns of trace data of target DC current, voltage and power in aluminum sputtering tools. (Sampling rate: 4 Hz.).

where $Max[x]$, $Med[x]$, and $Min[x]$ are respectively the maximum, median, and minimum values of x. If a drop in I_T occurs, $f_L(x)$ is larger than $f_U(x)$. Using the step function $h_c(x)$ of (4), we improved the indicator to (7) below.

$$Arcing\ Index\ 2 = f(I_T) \cdot h_c(\sigma[P_T]) \tag{7}$$

where f(x) is the function as (8),

$$\begin{aligned} f(I_T) &= f_U(I_T) - f_L(I_T) \\ &= 2Med[I_T] - (Max[I_T] + Min[I_T]) \end{aligned} \tag{8}$$

In (8), even if the average is used instead of the median, the difference is 0.1% or less. By using (8) which is expressed by differences between maximum or minimum and median, the Arcing Index 2 is virtually independent of the set value of the target DC current. The indicator is common to not only all chambers but also to all recipes.

Fig. 9 shows the trend data of the indicator of (3) and (7) in three representative chambers in all aluminum sputtering tools. The plots on these graphs in Fig. 9 are FDC data when all wafers are processed by multiple recipes in each chamber. The control limits are determined by engineers so that the FPR was as small as possible. The TPR and the FPR depends on the control limit. The control limits were able to be determined so that the FPR decreases to 0.01% for all chambers by adopting the indicator Arcing Index 2. On the other hand, the TPR improved slightly to 16.7%. The problem of low TPR persists. However, almost all faults can fortunately be detected at lot level because they occur on multiple wafers in a lot once an abnormal discharge occurs. Thus, scrap wafers are limited to within 25 wafers per lot. It is not a major problem for the TPR to be low at wafer level if the TPR is high at lot level. Our fab-wide FDC system (Fig. 1) can command process tools

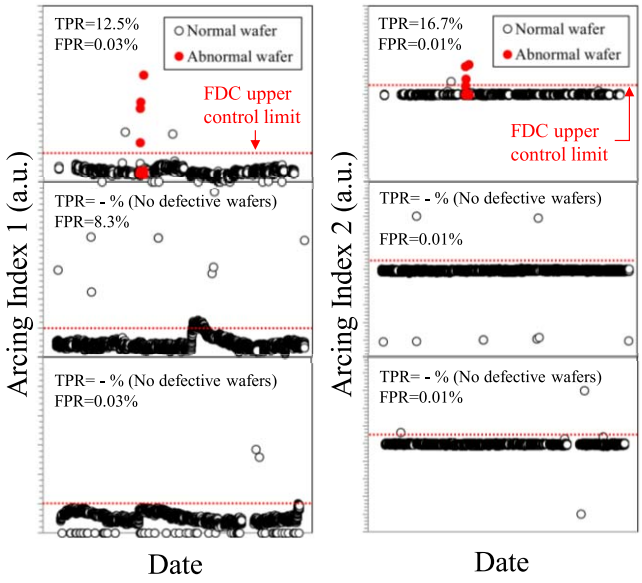


Fig. 9. Comparison of trend data for Arcing index 1 and Arcing index 2.

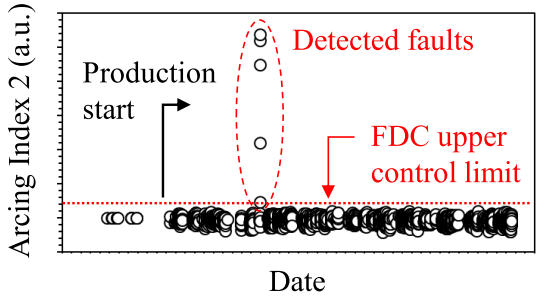


Fig. 10. Trend data of Arcing Index 2 in the chamber of a newly installed aluminum sputtering tool.

to stop processing at wafer level. However, almost no process tool software can automatically stop processing at wafer level. Conferring this capability would likely require major investment. If the number of scrap wafers increases, the investment execution should certainly be judged according to return on investment (ROI).

C. Extension of FDC Indicator to Newly Installed Tools

This subsection presents an example in which the chamber and recipe-independent FDC indicator was adopted in a newly installed tool and scrap wafers were kept to a minimum. It is normally difficult to implement FDC in a newly installed tool from the beginning of production. The chamber and recipe-independent FDC indicator we propose is, however, easily applied before the new tool begins production because it adopts the same equation and control limits for all chambers and all recipes. Fig. 10 shows the trend data of the indicator of (7) in the chamber of a newly installed aluminum sputtering tool. The plots on these graphs in Fig. 10 are FDC data when all wafers are processed by all kinds of recipes in the chamber as in Fig. 9. The FDC indicator detected a fault shortly after start of production. Pattern defects due to abnormal discharge

were confirmed in those wafers whose faults had been detected by the indicator. The root cause of the fault was the misalignment of the wafer transfer robot by the vendor during the installation of this tool. Abnormal discharge occurred between the edge of the wafer and local deposition on the deposition ring. The number of scrap wafers were restrained at minimum level by using the indicator in the FDC system. It is notable that we were able to improve the detection accuracy using the indicator, based on a simple equation using data from the legacy FDC system, without the need for an expensive arcing sensor.

D. Mechanism of Trace Data Change Using Equivalent Electrical Circuits for Abnormal Discharge

It is important when implementing FDC to clarify the relationship between changes in trace data and the changes in state that occur in the chamber. This subsection describes why, using equivalent electrical circuits, an instantaneous changes (i.e., a drop or a spike) of the trace data occurs in Patterns C and D in Fig. 8. In the DC discharge circuit, the resistance of the external circuit (R_E) excluding the resistance of the plasma (R_P) is expressed as (9).

$$R_E = P_T/I_T^2 - V_P/I_T \tag{9}$$

where V_P is the discharge voltage. Assuming that a glow discharge is kept in the DC discharge of the aluminum sputtering, V_P is constant [10]. P_T is also constantly controlled. Therefore, R_E becomes a monotonically decreasing function of I_T. In other words, R_E increases when I_T decreases, and vice versa.

Fig. 11 shows the equivalent electrical circuits and the trace data of I_T for the normal mode and the abnormal discharge modes. In Patterns C and D, the equivalent electrical circuits are shown at the moment that arcing occurs, that is, at the process times of T_d (when a drop in I_T occurs) and T_s (when a spike in I_T occurs) indicated by the arrows. The resistances of the external circuits (R_E) in Patterns A, C, and D are given by (10), (11), and (12), respectively, below.

$$R_E = R_T + R_W \equiv R_0 \tag{10}$$

$$R_E = R_T + R_D + R_W > R_0 \tag{11}$$

$$R_E = R_T + R_S/(1 + R_S/R_W) < R_0 \tag{12}$$

where R_T, R_W, R_D, and R_S are the resistances of the target, the wafer including the ESC, the deposition ring, and the shield, respectively. R_E is defined as R_0 in the normal mode in (10). In Pattern A, the normal mode, the equivalent electrical circuit is expressed as a series circuit of R_T, R_P, and R_W. Since V_P is constant, the circuit has a Zener diode added in parallel with the R_P. In Pattern C, the abnormal discharge mode to the wafer, the wafer and the deposition ring, which has the floating potential, are short-circuited when arcing occurs, so the combined impedance increases due to the series connection with the R_D. Therefore, since R_E increases ($R_E > R_0$) as shown in (11), I_T decreases, in other words, a drop in I_T occurs. On the other hand, in Pattern D, the abnormal discharge mode to other parts such as the shield, which is a grounding part other than a wafer, the combined impedance decreases due to the parallel connection with R_W. Therefore, since R_E decreases ($R_E < R_0$) as shown in (12), I_T increases, in other words, a spike in I_T occurs. Thus, the changes in the trace data and the modes of occurrence of abnormal discharge in the chamber can be directly linked. Our indicator is superior to statistical methods because it is easily understood by the manufacturing section operatives.

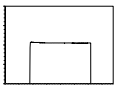
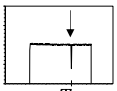
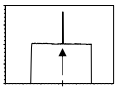
Pattern	Equivalent electrical circuit	Target DC current (I_T) [A] vs. process time	Occurrence of abnormal discharge to wafer
A	$R_E = R_T + R_W = R_0$; V_T, I_T, R_T Target, V_P, R_P Plasma, R_W Wafer, ESC		No
C	$R_E = R_T + R_D + R_W > R_0$; V_T, I_T, R_T, V_P, R_P, R_D Deposition ring (floating), R_W		Yes
D	$R_E = R_T + \frac{R_S}{1+R_S/R_W} < R_0$; V_T, I_T, R_T, V_P, R_P, R_W, R_S Shield etc. (grounding); $R_W \gg R_S$		No

Fig. 11. The equivalent electrical circuits and the trace data of the target DC current (I_T) for the normal mode (Pattern A) and the abnormal discharge modes (Pattern C and D). Patterns are shown in Fig. 8.

IV. Conclusion

In this paper, a chamber and recipe-independent FDC indicator is proposed to detect abnormal discharge in aluminum sputtering tools. Its effect was demonstrated using examples of mass production. The FPR was reduced by continuous improvement from Arcing Index 1 to Arcing Index 2. On the other hand, the TPR was only slightly improved. In this example, the fault can be detected almost completely at lot level because once an abnormal discharge takes place, it occurs on multiple wafers in the same lot. Therefore, this low TPR is not major problem. However, this is a question for future study.

The FDC indicator we propose was easily extended to a newly installed tool because the equation and the control limits are common to all chambers and all recipes. The indicator was adopted at the start of production in the tool and resulted in minimal numbers of scrap wafers. The FDC indicator does not require a lengthy and painstaking

setup by an engineer of the control limits for newly increased recipes after the control limits for a chamber have been set.

The ultimate purpose of FDC is to enhance the productivity of fabrication lines. It includes not only preventing scrap wafers but also improving the equipment's productivity and reducing equipment maintenance costs. To achieve these goals, FDC should be extended over the whole equipment, not only to process chambers. As a starting point for the FDC extension, we have developed FDC using a neural network with harmonic sensors to diagnose the degradation of wafer transfer robots for condition-based maintenance [11], [12]. In this case, statistical models are very useful for detecting failure modes, since humans cannot detect anomalies in large volumes of high-frequency trace data. It is necessary to develop FDC technologies by appropriately selecting the indicators as we proposed in this paper or the models using statistical methods such as machine learning, according to the purpose.

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