IC Lab Midterm

2020 Spring

Name: **Student ID:**

Total score: 100%

1. [10%]

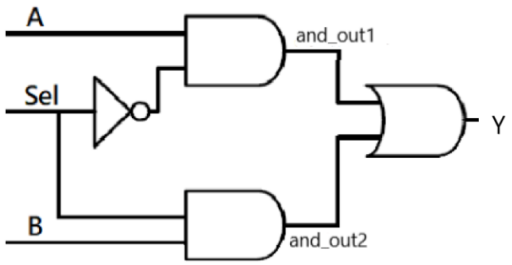
(a) Please write down the result of A in the code below and briefly explain the difference between ">>" and ">>>". (5)

```
wire signed [3:0] A,B;

assign B= 4'b1000;

assign A = B >>>2;
```

(b) When we will use "==" and "==="? Please briefly explain it and discuss the difference between them. (5)

2. [10%] Look at the code below. Is this code correct? If not, please explain "why" and "correct it".

```
always@(A or Sel or B) begin
   Y=and_out1 | and_out2 ;
   and_out1=A &(~Sel);
   and_out2=Sel & B;
end
```



3. [5%]

(a) Please briefly introduce and list one advantage and one disadvantage of synchronous reset and asynchronous reset. (3%)

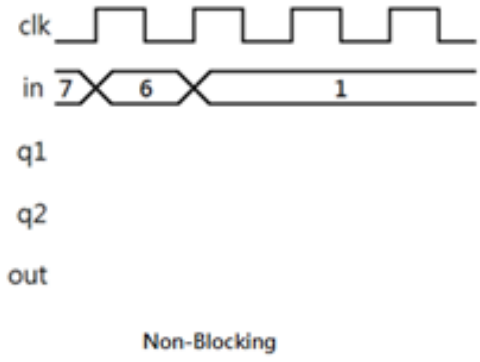
(b) Please draw the diagram of mealy and moore machine and simply compare the difference between them. (2%)

4. [10%]

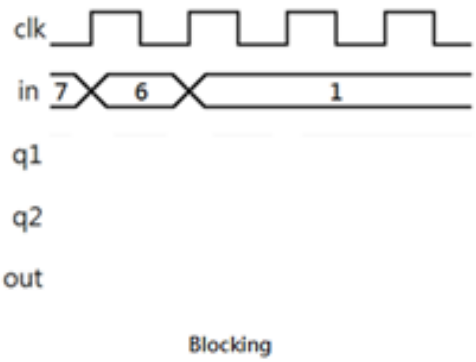
Please calculate the value of each node in different clock cycle for the following two cases

```
always @(posedge clk)
begin
   q1 <= in;
   q2 <= q1;
   out <= q2;
end
```

```
always @(posedge clk)
begin
   q1 = in;
   q2 = q1;
   out = q2;
end
```

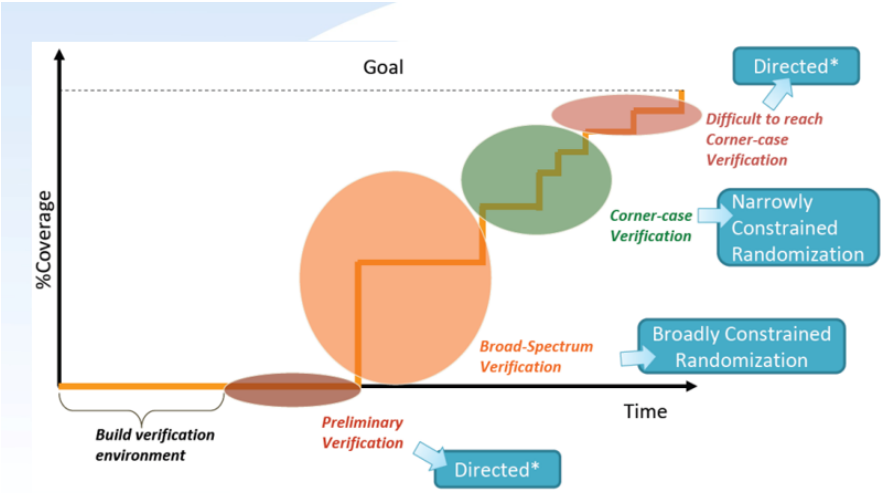


Non-Blocking



Blocking

5. [10%]
Please write down two kinds of testing pattern strategies and explain why do we need both strategies to achieve almost 100% coverage testing without consuming too much time.



6. [10%] Look at the figure below.

```
initial begin
        `ifdef RTL
                $fsdbDumpfile("Design.fsdb");
                $fsdbDumpvars(0,"+mda");
        `endif
        `ifdef GATE
                $fsdbDumpfile("Design_SYN.fsdb");
                $fsdbDumpvars(0,"+mda");
                $sdf_annotate("CORE_SYN.sdf",dut);
        `endif
end
```

i. What is the purpose of syntax "**"+mda"**" ?

ii. What is the purpose of syntax "**sdf_annotate("CORE_SYN.sdf",dut);**" ? Please also describe what is **Standard Delay Format file (.sdf).**

7. [10%]

Give the formulas of the setup time criterion:

i. data required time

ii. data arrival time

iii. setup time criterion

in terms of (T_{cycle}: clock cycle, t_{pcq}: clk-to-Q propagation delay, t_{ccq}: clk-to-Q contamination delay, t_{pd}: logic propagation delay, t_{cd}: logic contamination delay, t_s: setup time)

8. [5%]

How to fix **setup time violation** and **hold time violation(**Please list at least two methods separately**)**?

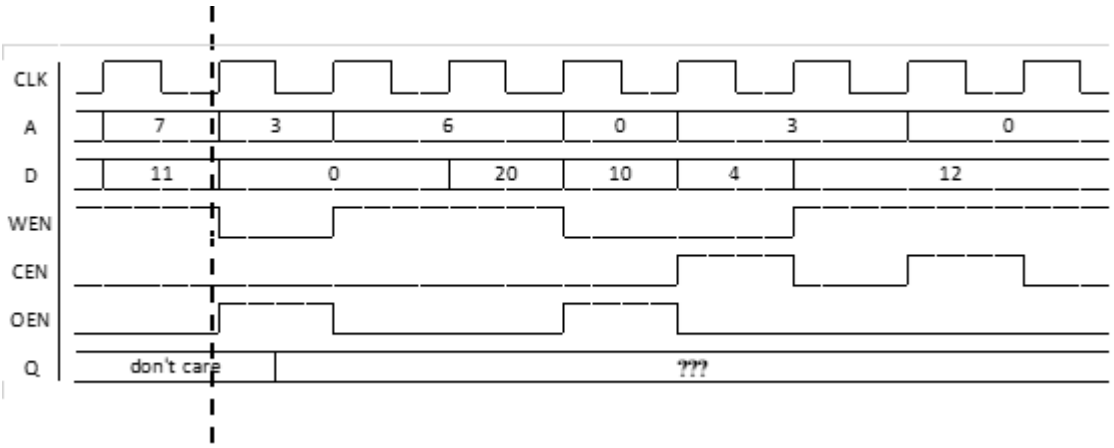
9. [10%]

Following is a port waveform of an 8-word-32-bit memory in RTL simulation. Initial value table gives the word values right before the 2nd CLK positive edge. (dotted line)

(a) Please **complete the waveform of Q signal** after the 2nd CLK negative edge (the "**???**" part). You should **redraw the CLK signal and highlight the start of '???' part** in your waveform. (6)

(b) And **give the final value table** after the last CLK negative edge based on the given initial value table. (Assume all values are decimal and the clock period is 10ns.) (4)

Waveform:



Initial value table:

Address	0	1	2	3	4	5	6	7
Value	X	25	4	52	18	38	X	11

10. [10%]

For the following three stage, what kind of **memory related files** do we need if we want to use SRAM in our design?

How do we get those files?

Why do we need these files?

Please clearly indicate them one by one.

(1) 01 RTL simulation

(2) 02 Synthesis and STA

(3) 03 Gate level simulation

11. [5%]

Please briefly describe the difference between **compile** and **compile_ultra.** And what situation will designer to use **compile** or to use **compile_ultra**?

12. [5%]

Please explain the difference between **Top-down compile** and **Bottom-up compile**, and list their **respective advantage**.