

1. [10%] Please explain STA (static timing analysis) and DTA (dynamic timing analysis) briefly and compare them.

1. [5%] Please explain the difference between STA (static timing analysis) and DTA (dynamic timing analysis) #2017 Spring

✓ STA(Static Timing Analysis) 針對電路中的每條path(D flip-flop間)

- Verify the timing of a digital design based on a **statistic** method (without requiring a simulation) of the full circuit
- STA is a **complete** and **exhaustive** verification of all timing checks of a design because it **analyzes every timing paths in design according to constraints**. 02的timing report就是使用STA分析
- check that if there is any violation on setup/hold time in the timing path, glitches, critical path and clock skew.
- STA aims at different corner to analysis, so the analysis time is faster than DTA.

不是所有情況都會發生,透過DTA跑出較貼近現實情況的模擬結果

✓ DTA (Dynamic Timing Analysis) 針對Design by function寫入test pattern

- 同様可
以驗證
function
是否正確
- Quality(Coverage) of the Dynamic Timing Analysis (DTA) increases with the increase of **input test vectors**. 03的simulation就是使用DTA
 - The growing size of test vectors increase simulation time, especially in post-sim. test pattern電路進入電路模擬,根據不同input,分析signals經過每個path

Review setup/hold time



ICLAB NCTU Institute of Electronics 的 timing

需要很多pattern來確保每條path都符合規範

5

3. [6%] When using clock gating, in terms of power consumption, which gating is better? AND-Gating or OR-Gating? Please justify your answer.

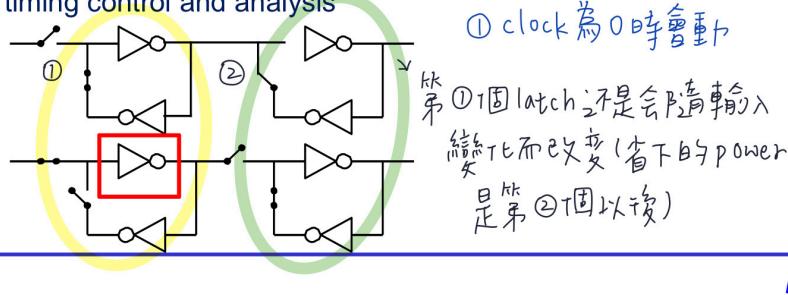
Dynamic Clock Gating (cont.)

➤ OR-gating is better 典型的posedge FF是由2個Latch所組成

- **OR-gating consumes less power than AND-gating**
 - For OR-gating, the gated clock is tied at high when the register is turned off.
 - No matter data is toggling, the first latch circuits will not be toggled.
 - For AND-gating, the gated clock is tied at low when the register is turned off.
 - The **first latch circuits** will consume power as data input is switching.
- The gating control signals should be generated from clock rising edge
- flip-flops → stable gating the clock as clock high period
 - Consistent with original clock rising edge trigger registers design
 - It is easier for timing control and analysis

OR Gating

clock維持在高會把
第1固Latch disable,
會比AND
gating省下第一
固Latch的電



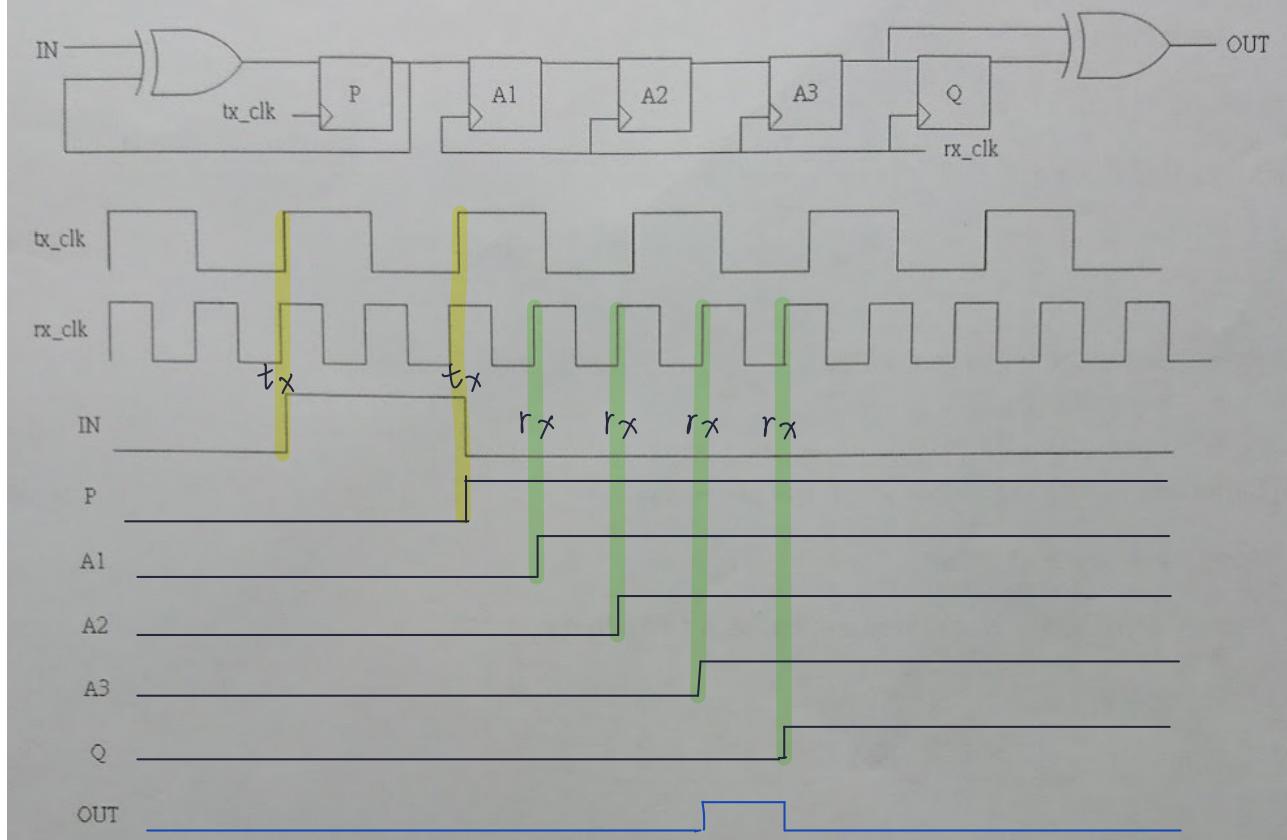
OR gating: 因為
Master slave FF
在off時, OR
gating處於
tie-high, 此時
第一固Latch不會
有power
consumption; 相
對的, 如果使用
AND gating, 由
於tie-low的
特性, 第一固
Latch TNS會有
power consumption



2. [4%] (a) Please explain why we need a **synchronizer** in our design and its functionality.

[4%] (b) What may happen if we don't use XOR gates in a synchronizer?

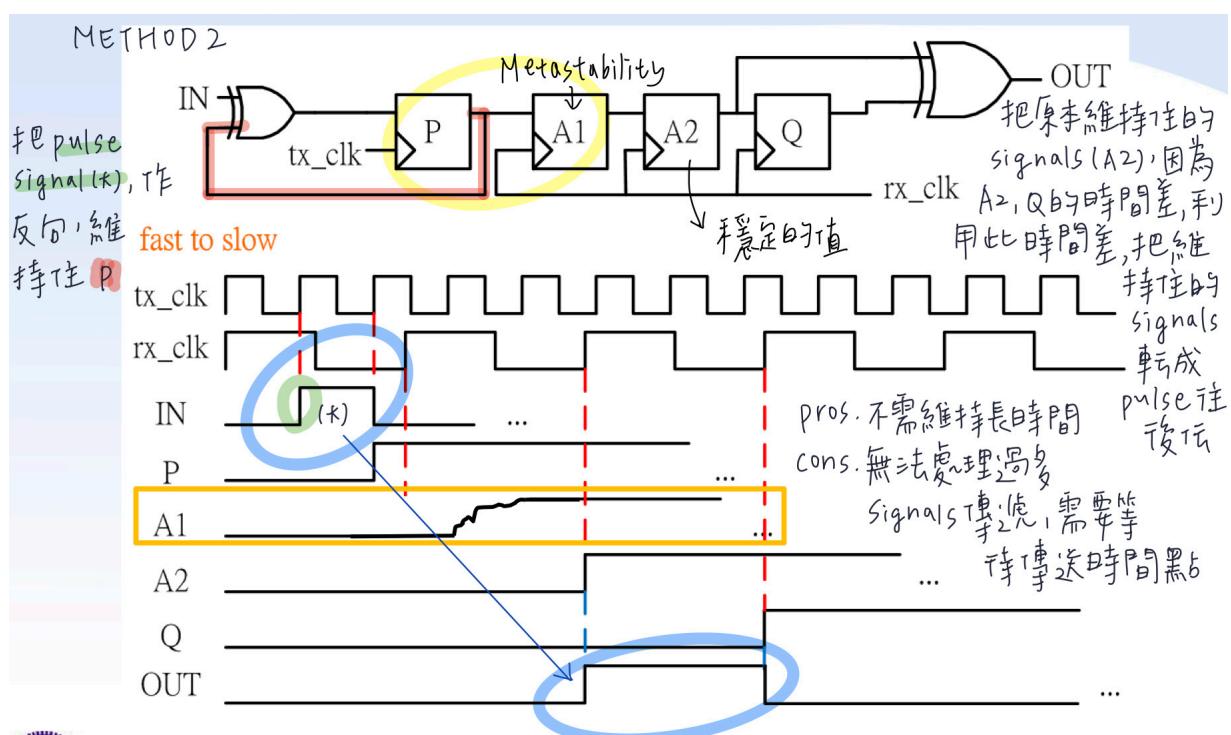
[6%] (c) Complete the waveform below



✓ Because different blocks require different clock period, some blocks need long clock period to operate, but others only do simple work. If we all use long clock period, it will cause the performance to be poor. So that's why we need to use **clock domain crossing**.

(2) 因為兩邊 clock period 不同，
如果 $t_{x\text{-}clk} \ll t_{r\text{-}clk}$, 則會
有 signal loss 的 problem

(快 \rightarrow 慢)



4. [8%] Down below is the figure of power gating.

A is "Power gating controller"

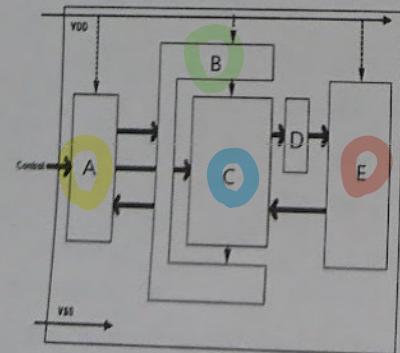
B is "Power switching fabric"

C is "Power gated block"

E is "Always on block"

What is block "D"?

Please also briefly describe how to implement the block D using one gate as an example.



D: Isol

AND/OR Gate: Isolation cell

5.

A) [6%] Why is Typedef used in systemVerilog?

B) [6%] Write a representation of hBytes if "reg" is used as a datatype instead of hexOctet

typedef reg [7:0] octet;

typedef octet [15:0] hexOctet;

hexOctet hBytes [3:7];

✓ Make code clear

Typedef

- SystemVerilog's data type system allows you to define quite complex types. To make this kind of code clear, the **typedef** facility was introduced
- **typedef** allows users to create their own names for type definitions that they will use frequently in their code

B) reg [(5:0)[7:0] hBytes[3:7]

6. [6%] What values are constrained by "Limit"? (List them out)

```
constraint Limit{
```

```
    sa inside { [4:8], 11, 21};
```

```
    payload.size() <= 4;
```

```
}
```

sa = [4, 5, 6, 7, 8, 11, 21]

payload = [0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15]

7. [6%] How many state bins are created:

a. bins s0 = {[0:4]}

b. bins s1 [] = {[3:9]}

a: 1個 bin

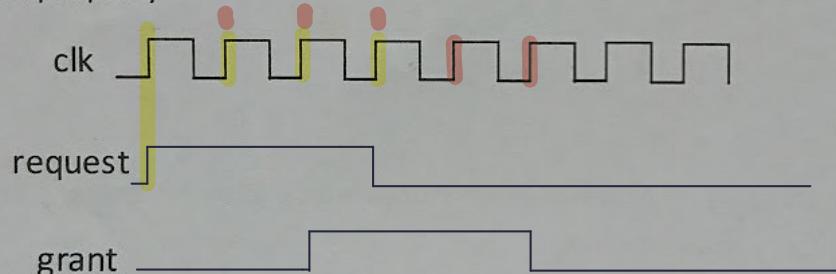
b: 7個 bin

8. [6%] Fill in the waveform below given the property:

```
property p_request_grant;
```

```
@(posedge clock) request ##2 grant ##1 !request ##2 !grant
```

```
endproperty
```



9. [4%] What is purpose of the “uniquify” command in the design flow?

10. [6%] What is the cause, and proper solution of IR drop?

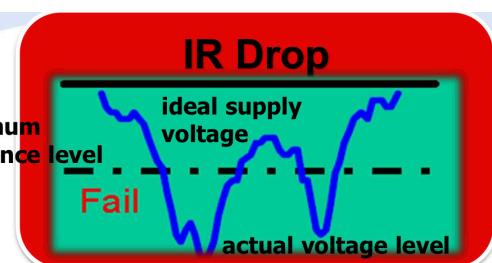
9) 諸如 EDA tool 對于使用同一個 module 的電路重新命名，使各個電路獨立以進行最佳化

(10)

✓ IR Drop

- Average or Instantaneous Power Issue

主因：電路的路徑會有電阻，電阻會造成電壓降，導致給 cell 的 voltage 低於 minimum tolerance level



✓ Power issue

- IR drop (IRD)

① 增加 stripes, 在周圍拉更多 power 線入 circuit
② 改變 pad 摆放置 (powerplan) ⇒ power pad 均勻

④ 若同時很多

cell 一起 toggle

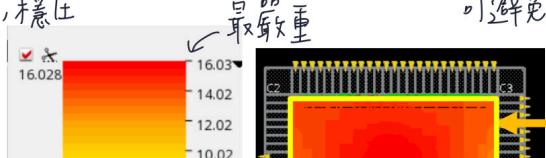
→ 造成很大 power 用量

耗

- Prevention: 1. Adding stripes to avoid IR drop on cell's power line
- 2. Change the position of power pad to avoid long power line
- 3. Use square-shaped Chip to avoid long power line
- 4. Add decoupling cell. 不會讓很多 cell 一起 toggle

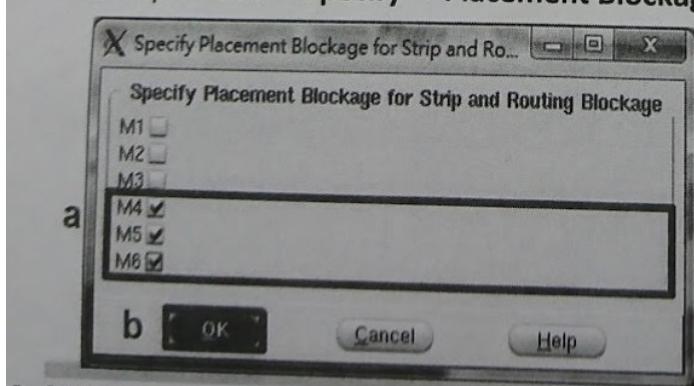
③ chip 見到正方形，可避免過長 power line

Range	Total Count	Displayed / Scissored
> 16.03 mV	1	1 / 0
16.03 ~ 14.02 mV	12584	12584 / 0
14.02 ~ 12.02 mV	7782	7782 / 0
12.02 ~ 10.02 mV	3503	3503 / 0
10.02 ~ 8.01 mV	2611	2611 / 0
8.01 ~ 6.01 mV	1693	1693 / 0
6.01 ~ 4.01 mV	864	864 / 0



Power line too long

11. [4%] In APR flow there is a step before we place the standard cell. Describe its intention.
The step: Place -> Specify -> Placement Blockage



- ◇ M2
- ◇ M3
- ◆ M4
- ◆ M5
- ◆ M6

11) 如果 stripe 無法放的 metal 層，就不能放置 standard cell

M₄, M₅, M₆: power stripe

12. [8%] What is **Antenna Effect**? List 2 repair method for Antenna Effect.

13. [4%] Please simply describe why **RC extraction** is needed.

14. [6%] Describe the powered simulation methods **vector-based** and **vector-independent**.

(2)

Process Antenna Effect

action不會發生

在晶片製造過程中，每層 metal 長完後要打磨，metal 上會累積靜電

powerp
placem
CTS
routin

Antenna Effect 靜電，超過一定程度無法放電，可能會透過元件，打穿氧化層

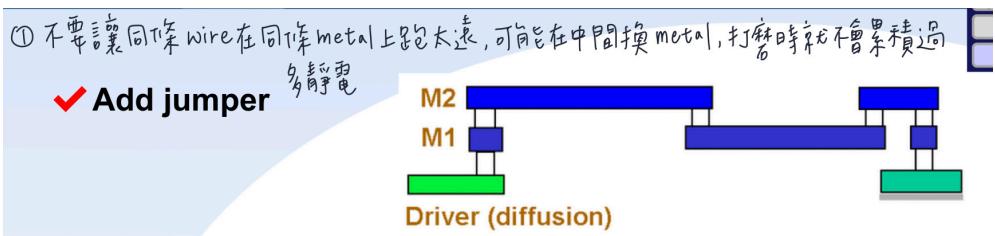
- In a chip manufacturing process, metal is initially deposited so it covers the entire chip
- Then, the unneeded portions of the metal are removed by etching, typically in plasma (charged particles).
- The exposed metal collect charge from plasma and form voltage potential.
- If the voltage potential across the gate oxide becomes large enough, the current can damage the gate oxide.

② 電壓產生高於 threshold
電荷會流到 GND

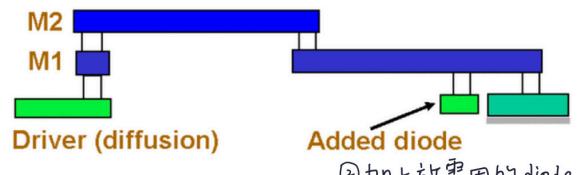
$$\text{Antenna Ratio} = \frac{\text{Area of process antennas on a node}}{\text{Area of gates to the node}}$$

Problem Repair

- Add jumper (change metal layer)
- Add antenna cell (diode)
- Add buffer



✓ Add diode



✓ If after fixing antenna violation, there still exist violations

- Larger chip area
- Place module precisely

(3)

layout 結束後，可以藉
metal 寬度、Wire 間 space 以
及 layout 等資訊檢查表抽
出 RC 值 \Rightarrow 帶入 power
analysis, simulation 以或
得到更準確的結果

14) ✓ Vector: simulation waveform result for all gates

Dynamic power analysis

✓ Vector-based 透過 simulation 產生的波形檔 \rightarrow 會消

- Uses VCD (waveform file)
 - VCD is waveform file, like fsdb
- Requires:
 - Simulation is possible at the full-chip level
 - Simulation provides sufficient functional coverage of design
 - Vectors include those cause highest power consumption

耗多少 power

\rightarrow 可分析 power picket

(打到消耗很多 power 的 pattern)

\rightarrow postsim

\rightarrow 才能考慮到所有使用情形

✓ Vector-independent 三沒有跑 simulation 的情況下分析

- Uses TWF (timing window file, generated by Static Timing Analysis)
 - Clock domain, skews, slack, arrival times of each pin.
- Requires:
 - A good estimation of input switching frequency

\rightarrow 不知道電路每個 signal toggle 的情況，會設 toggle probability

\rightarrow e.g. 70%

\rightarrow 透過 STA 分析 circuit 所有 path，再透過 library 查表，計算 power 消耗