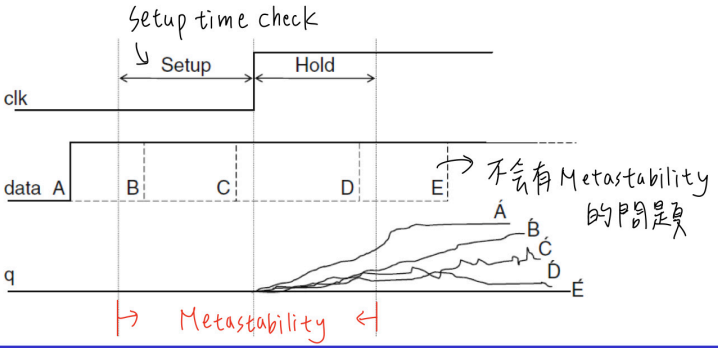
2017 spring

2. [15%] Please answer the following questions:
   a. [5%] Please explain metastability briefly
   b. [5%] What is the functionality of adding XOR gates in traditional synchronizer?
   c. [5%] Complete the waveform below #2017 fall (2)(c)

2) (a)

- ✓ The unstable status due to non-ideal data transition is called metastability. signals 準備時，如果有 violation 情況發生，signals 就會有不穩定的狀況 ⇒ Metastability
- ✓ To avoid this phenomenon, we have to ensure no data transition during setup/hold timing check.
- ✓ However, CDC designs will inevitably face this problem.



(b) 確保給的 pulse 可在下個 clock domain 被 catch 到

3. [5%] Please list 3 methods to reduce the dynamic power and briefly explain them.
4. [10%] Please answer the following questions:
   a. [5%] How to avoid glitch when we apply clock gating method
   b. [5%] Which one can consume less power when we apply clock-gating, AND-gate or OR-gate? why? #2017 FALL (3)

3) ① 降低 VDD：可以減少充放電電容時的 Power

② 降低 switching probability：充放電↓ ⇒ power↓

③ 減少 NMOS，PMOS 同時 on 的時間：可以減少 short circuit power

補（講義上寫的）

■ Dynamic Power Reduction

- Multi Voltage 降 Vdd；SVS, MVS, DVFS
- Power Gating 2 power mode: A low power mode / active mode
- RTL and Architecture Design Techniques pipeline（增加 register）
  → 增加電容，減少 power supply
  ↳ parallel
  1 cycle → 2 cycle
  frequency 減半，
  delay 變寬鬆，Vdd 可↓
- Clock gating
  ⇓
  △ turn off the unused register
  △ reduce the clock switching power

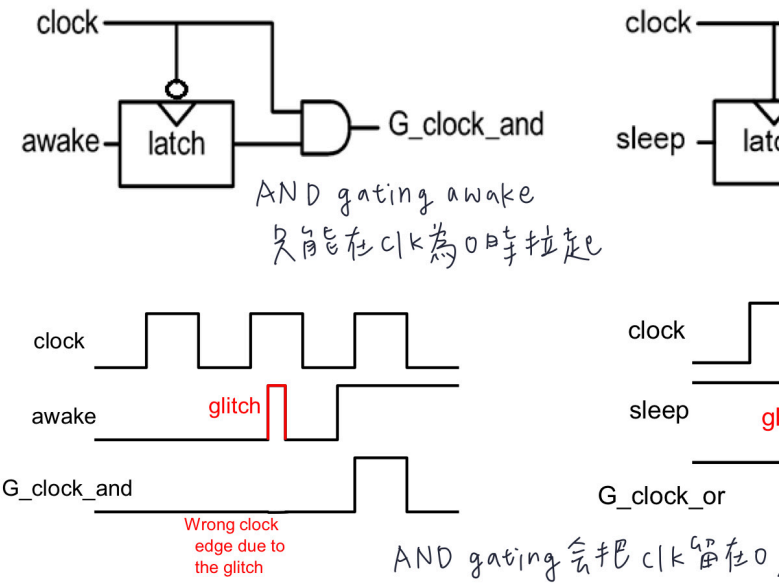
sleep mode
（shut down power to block of logic）

4)(a)

在可能發生glitch的signal加上latch，讓原本會發生glitch的情況，會被latch擋住ㄋ不會有glitch

latch：enable → 讓Data通過；

disable → 其值不改變

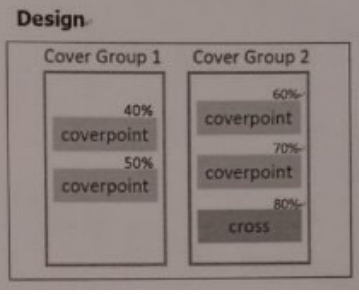


5. [10%] List one enhancement in **design** and **verification** using SystemVerilog, respectively. Moreover, briefly explain what the corresponding **advantage** is. (Assertion is excluded)
6. [10%] Please explain the difference between **structure** and **packed structure.**

PPT沒有相關內容

5) Design：logic　　Verification：randc

7. [5%] Please explain the difference between **functional coverage** and **code coverage**.
8. [5%] Calculate the coverage of the whole design, the coverage of coverpoints or cross is specified as the following figure.



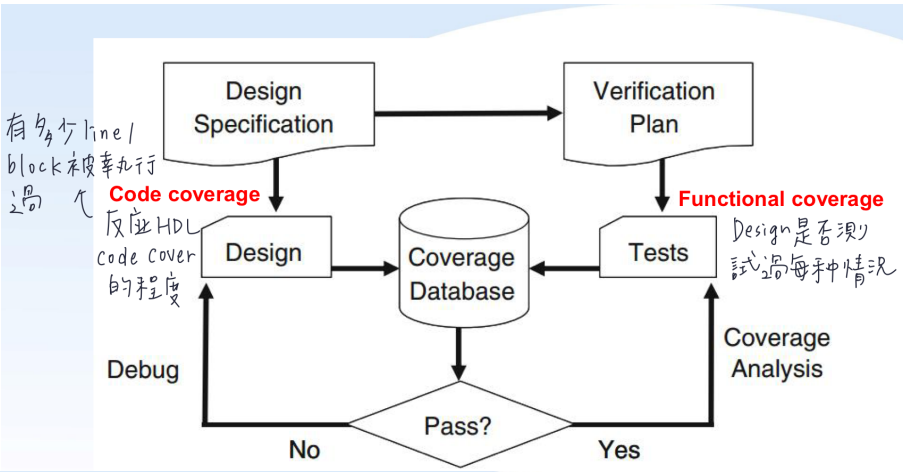
cg1：$\frac{1}{2}\times 0.4+\frac{1}{2}\times 0.5=0.45$

cg2：$\frac{1}{3}\times 0.6+\frac{1}{3}\times 0.7+\frac{1}{3}\times 0.8=0.7$

$\frac{1}{2}\times 0.45+\frac{1}{2}\times 0.7$

$=0.575$ #

7)



有多少line/block被執行過了

反應HDL code cover的程度

Design是否測試過每種情況

code coverage：有被執行到code比例，ex. 程式碼中每個block是否皆有被執行到，FSM的每個state是否都有走過…等

Functional coverage

- Possible to represent all meaningful design functionality
- Implements the verification plan – what needs to be verified
- Noise-free – nothing is don't-care
- Requires planning, coding, and debug
- May be incomplete due to human error

Code coverage

- Easy to generate automatically
- Guaranteed to be structurally complete – not prone to human error
- Standard models capture much of the meaningful behavior of the design
- May not capture all meaningful design functionality
- Can be noisy – "don't-care" or duplicate covers

ex. default但永遠打不到

9. [5%] Please explain the difference between **immediate assertions** and **concurrent assertions**.
10. [5%] How can **assertions** help us in building verification environment?

9)

✓ **Immediate assertions** test for a condition at the current time 某個時間點的 condition 是否 hit

A test of an expression when the moment the statement is executing

滿足某條件下, check current time 的行為

✓ **Concurrent assertions** test for a sequence of events over multiple clock cycles 用來測接下來 cycles 的一系列情況

Test for a sequence of events spread over multiple clock cycles 檢查一連串的行為

10)

SystemVerilog assertions have several advantages

- Concise syntax 語法簡潔
- Ignore by synthesis
- Can be disabled
- Can have severity level 嚴重性可分等級

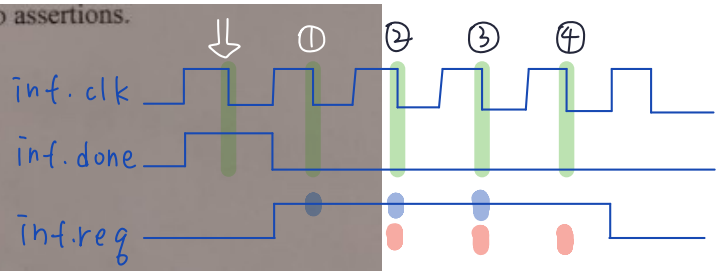
11. [5%] Please **draw the waveform** to explain the following two assertions.

```
property next_req1;
@(negedge inf.clk) inf.done === 1 |-> ##[1:3] inf.req == 1;
endproperty

property next_req2;
@(negedge inf.clk) inf.done === 1 |=> ##[1:3] inf.req == 1;
endproperty
```

在 ● 其中一個為 1

在 ● 其中一個為 1



12. [5%] How to prevent crosstalk by using placement solution and routing solution separately?
13. [5%] Please simply describe what's antenna effect? #2017 FALL(12)
14. [5%] Please simply describe what LEF and LIB library contain?
15. [5%] Describe the difference of Technology LEF file and Cell library LEF file.

12)

Crosstalk prevention – Placement solution

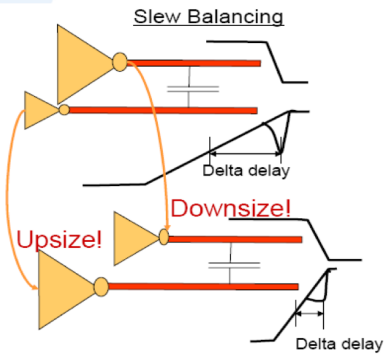
- Insert buffer in lines
- Upsize driver
- Congestion optimization

如果 2 signals, 其一 driving 能力較弱就容易被其它 signals 影響, 造成其 transition time 很長

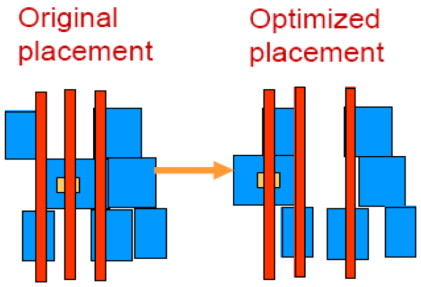
⇒ 調整 buffer, inverter 大小讓每條 signals transition time 差不多

Crosstalk prevention – Routing solution

- Limit length of parallel nets
- Wider routing grid
- Shield special nets



• Reduce coupling capacitance



有空間拉遠一點避免互相影響程度

14) LEF ┌ Technology : placement, rounting design rule, process information for layers　和製程相關
└ Physical Macros : macro / standard cell information

✓ **What is lef ?**
- Library Exchange Format (LEF)
- LEF defines the elements of an IC process technology and associated library of cell models.
- LEF file can be divide into two part: technology and physical macros

✓ Technology

簡略版layout，讓APR完成繞線
→紀錄每個cell的圖形info. ex. IO pin, block size　abstract model
→省儲存data大小，較快跑完APR

LIB: standard cell / IO Pad cell
timing / power / cell area information

15) Technology LEF ┌ Process technology : Layers, Design rule, Parasitic
製程相關 └ APR technology : Site, Rounting pitch, default direction, Via rule

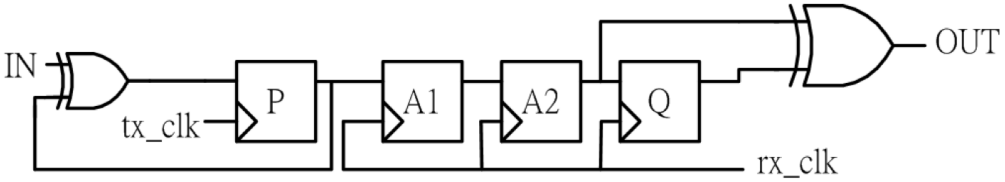
Cell Library LEF
┌ Define physical data for: standard cell, I/O pads, MEM, 其它 hard macros
└ Define abstract shape

2018 Spring

1. [15%] Please answer the following questions:
   a. [3%] Please explain CDC.
   b. [8%] In order to solve CDC problem, you need to use Synchronizer with XOR. Please draw the "2-stage Synchronizer with XOR" with Flip-Flop and XOR.
   c. [4%] And if we use 1-stage Synchronizer with XOR, what problem may occur?

1) (a) ✓ Because different blocks require different clock period, some blocks need long clock period to operate, but others only do simple work. If we all use long clock period, it will cause the performance to be poor. So that's why we need to use clock domain crossing .

(b)



(c) 若只使用1 stage，易產生亞穩態使電路工作異常