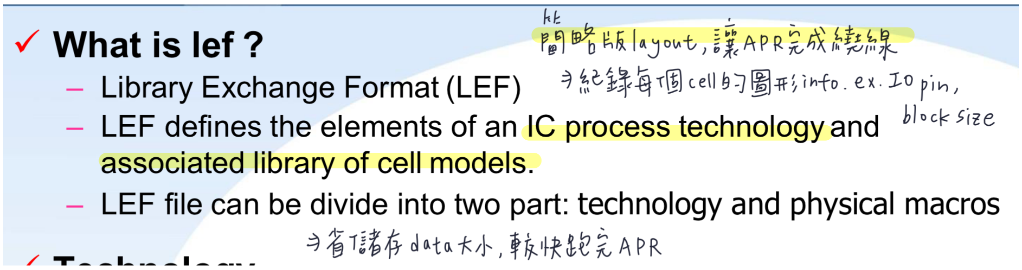
14) LEF
- Technology : placement, rounting design rule, process information for layers
- Physical Macros : macro / standard cell information

和製程相關



✓ **What is lef ?**
- Library Exchange Format (LEF)
- LEF defines the elements of an IC process technology and associated library of cell models.
- LEF file can be divide into two part: technology and physical macros

✓ Technology

簡略版layout，讓APR完成繞線

→紀錄每個cell的圖形info. ex. IO pin, block size

→省儲存data大小，較快跑完APR

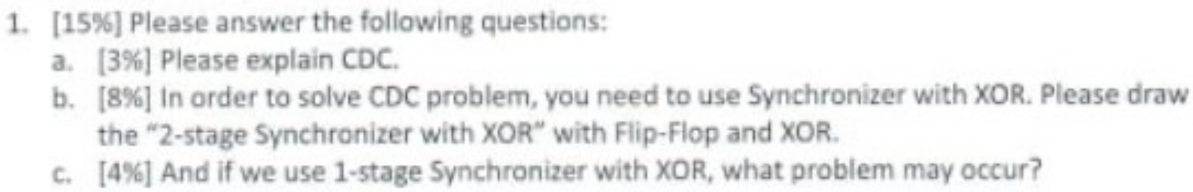
abstract model

LIB : standard cell / IO Pad cell
timing / power / cell area information

15) Technology LEF
製程相關
- Process technology : Layers, Design rule, Parasitic
- APR technology : Site, Rounting pitch, default direction, Via rule

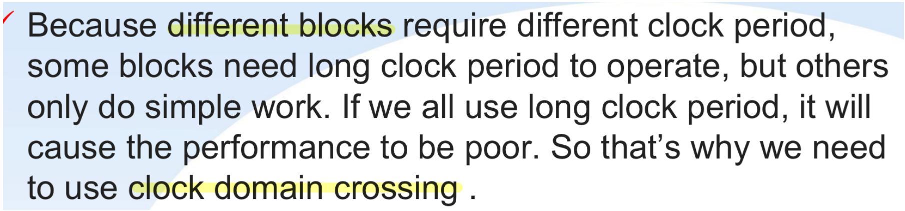
Cell Library LEF
- Define physical data for : standard cell, I/O pads, MEM, 其它hard macros
- Define abstract shape

#2018 Spring



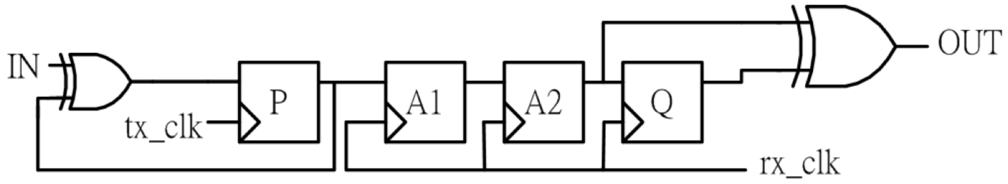
1. [15%] Please answer the following questions:
   a. [3%] Please explain CDC.
   b. [8%] In order to solve CDC problem, you need to use Synchronizer with XOR. Please draw the "2-stage Synchronizer with XOR" with Flip-Flop and XOR.
   c. [4%] And if we use 1-stage Synchronizer with XOR, what problem may occur?

1) (a)



Because different blocks require different clock period, some blocks need long clock period to operate, but others only do simple work. If we all use long clock period, it will cause the performance to be poor. So that's why we need to use clock domain crossing .

(b)



(c) 若只使用1stage，易產生亞穩態使電路工作異常

2. [3%] Describe 3 different Voltage Scaling Strategies (SVS, MVS, DVFS).

- **Static Voltage Scaling (SVS):**
  - Different blocks or subsystems are given different, fixed supply voltages.
- **Multi-level Voltage Scaling (MVS):**
  - A block or subsystem is switched between two or more voltage levels.
  - Only a few, fixed, discrete levels are supported for different operating modes. 動態調整Vdd (自由度較低)
- **Dynamic Voltage and Frequency Scaling (DVFS):**
  - An extension of MVS where a larger number of voltage levels are dynamically switched to follow changing workloads.

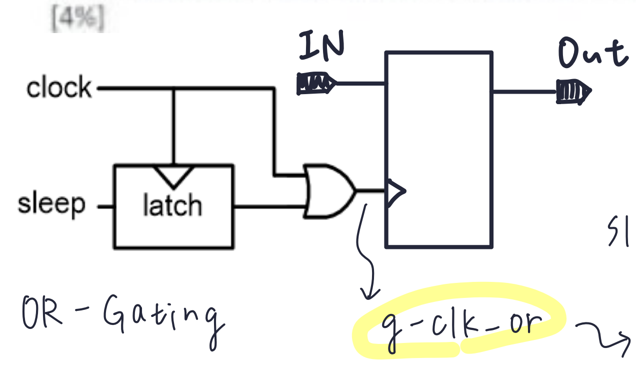
主要調整Voltage和frequency (Vdd level相對較多)

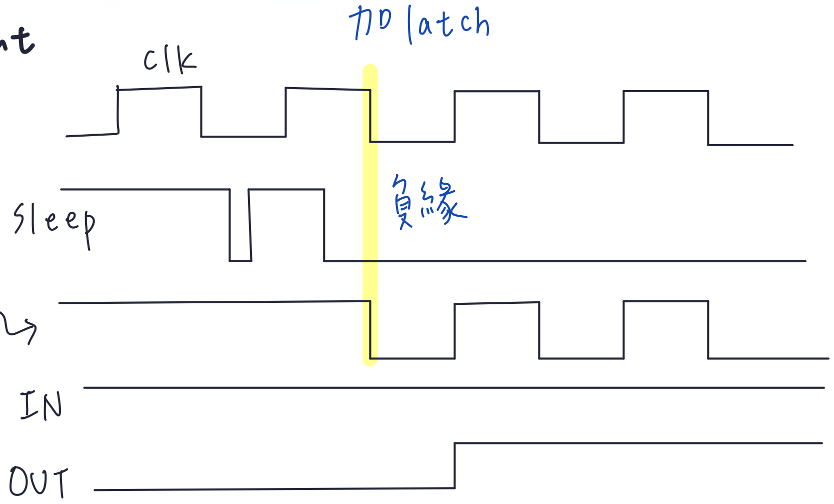
3. [2%] What problems might occur when 2 power domains at different voltage levels are connected together (list one)? And how to solve it?

- **Connecting 2 power domains at different voltage levels can cause design issues** 前一級過高，下一級Gate可能損壞
  - Timing inaccuracy
  - Signals are not propagated

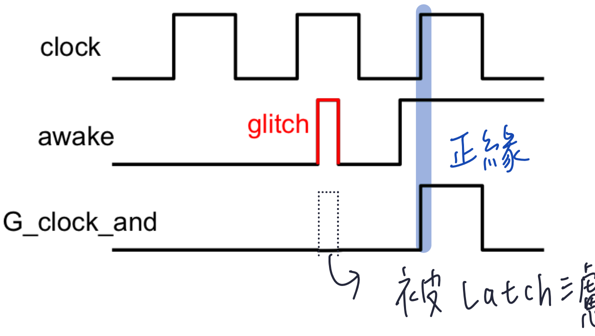
加上過渡元件 ⇒ Level shifter

4. [10%] In Dynamic Clock Gating Technique, And-gating and Or-gating both suffer from glitch problem. Please draw the glitch-free Dynamic Clock Gating block diagram with input signals: clock, awake(sleep) and output signal: G_clk_and(G_clk_or) [6%] and their waveform (please also draw glitch in awake(sleep) signal and explain how the problem can be avoided? [4%]





AND- Gating (Latch加INV)



透過Latch, awake/sleep更新只會在正緣(AND)/負緣(OR)

→ 可避免glitch

#2017 Fall (10)

5. [10%] Please answer the following questions:
  a. [5%] Please briefly describe IR drop.
  b. [5%] Please briefly describe the way to prevent IR drop.

6. [6%] Why we need library characterization? (one reason)

6) 我們需要知道製程上的一些特性，如 timing，寄生電阻，電容等，才能在 simulation 時知道接近真實的情況

7. [10%] Please explain the following:

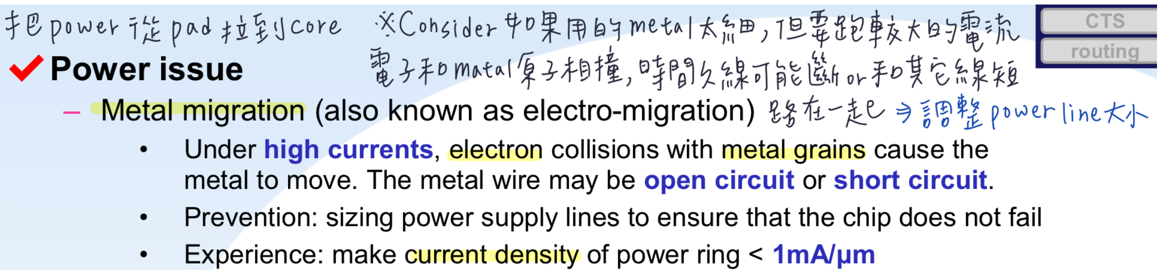
a. [4%] What is the usage of Halo in floorplan

b. [3%] What is Metal migration

c. [3%] What is Antenna effect

7) (a) 設置 Halo 可以避免 rounting 或放置 standard cell 時，與 IP 太過接近導致問題發生

(b)



把 power 從 pad 拉到 core

※Consider 如果用的 metal 太細，但要跑較大的電流 電子和 matal 原子相撞，時間久線可能斷 or 和其它線短路在一起 ⇒ 調整 power line 大小

CTS
routing

✓ **Power issue**

– Metal migration (also known as electro-migration)

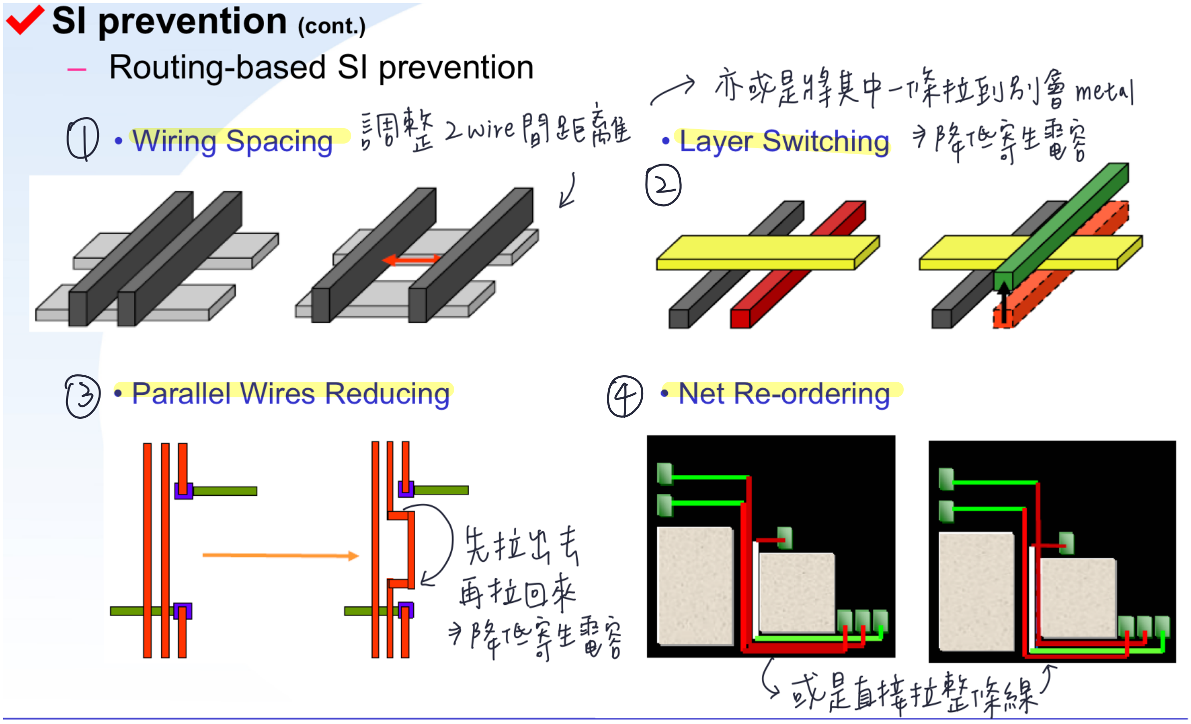
- Under **high currents**, electron collisions with metal grains cause the metal to move. The metal wire may be **open circuit** or **short circuit**.
- Prevention: sizing power supply lines to ensure that the chip does not fail
- Experience: make current density of power ring < **1mA/μm**

8. [6%] List three of Signal Integrity (SI) Issue

① Crosstalk ③ Leakage

② Supply / Propagated noise ④ overshoot, undershoot

9. [4%] List two routing method to prevent Signal Integrity (SI) Issue



✓ **SI prevention** (cont.)

– Routing-based SI prevention

① • Wiring Spacing 調整 2 wire 間距離

→ 亦或是將其中一條拉到別層 metal

② • Layer Switching ⇒ 降低寄生電容

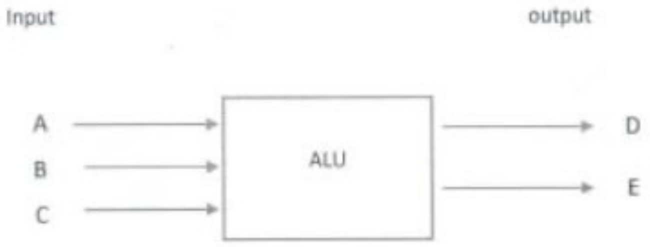
③ • Parallel Wires Reducing

先拉出去 再拉回來 ⇒ 降低寄生電容

④ • Net Re-ordering

或是直接拉整條線

10. [7%] Please answer this question:



(input and output are all one bit signal)

```
module TESTBED;
        reg clock ;
        INF inf(systemclock);
        PATTERN test(.clk(clock) , .inf(inf.PATTERN));
        ALU dut(.clk(clock) , .inf(inf.DESIGN));
endmodule
```

Above figure is the I/O port for the ALU design and the module TESTBED .

You need to declare and finish the interface content used in the TESTBED module .

```
Interface ......;
.
.
.
endinterface
```

```
interface INF (input bit clk);
logic clk, A, B, C, D, E;
modport PATTERN (
        input D, E,
        output A, B, C;
);
modport DESIGN (
        input A, B, C,
        output D, E;
);
endinterface;
```

11. [8%] Please answer the following questions:

```
covergroup test @(posedge clk);
        option.per_instance = 1;
        option.at_least = 100;
        coverpoint inf.signal_0{
                bins signal_0 [] = ([0:4] => [0:4]);
        }
        signal1:coverpoint inf.signal_1{
                bins signal_1 = 1 ;
        }
        coverpoint inf.signal_2{
                option.auto_bin_max = 16;
        }
        signal3:coverpoint inf.signal_3{
                bins s3_0 = 0;
                bins s3_1 = 1;
                bins s3_2 = 2;
        }

        cross signal1 , signal3 ;
endgroup
```

Above is a covergroup declaration.

a. [4%] If signal_2 is a 10 bits signal, how many numbers will contain in one bin?

b. [4%] In what condition that this covergroup will achieve 100% coverage?

(you need to write down each condition clearly)

a)

$2^{10} = 1024$ value

$1024 / 16 = 64$ #

b) ① inf.signal_0

0~4 ⇒ 0~4　每組100次

② inf.signal_1　100次

③ inf.signal_2

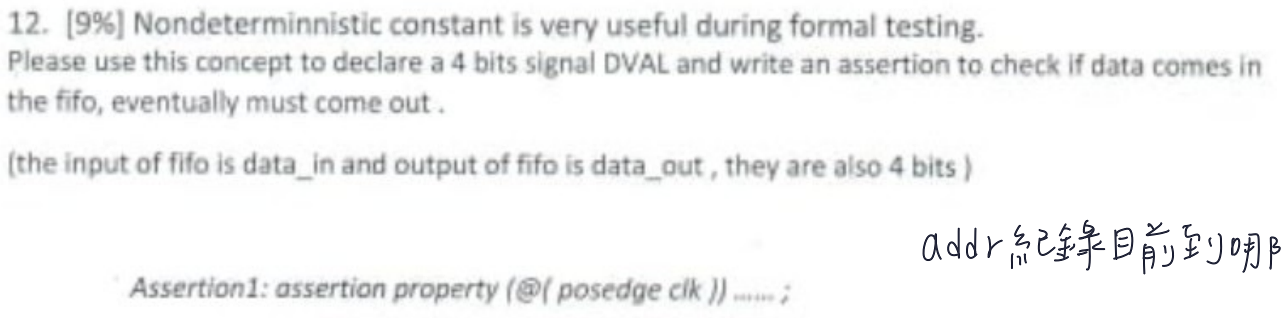
在每個bin中都要達成100次

Ex. 落在 0~63 100次↑

④ inf.signal_3 = 0,1,2

每組各100次

⑤ ②且④ 各達100次



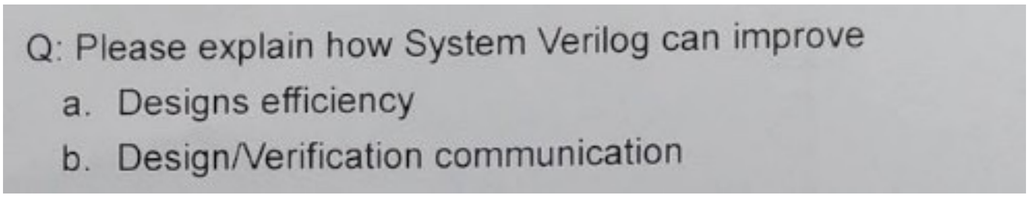
12. [9%] Nondeterminnistic constant is very useful during formal testing.
Please use this concept to declare a 4 bits signal DVAL and write an assertion to check if data comes in the fifo, eventually must come out .

(the input of fifo is data_in and output of fifo is data_out , they are also 4 bits)

addr紀錄目前到哪?

Assertion1: assertion property (@(posedge clk)) ...... ;

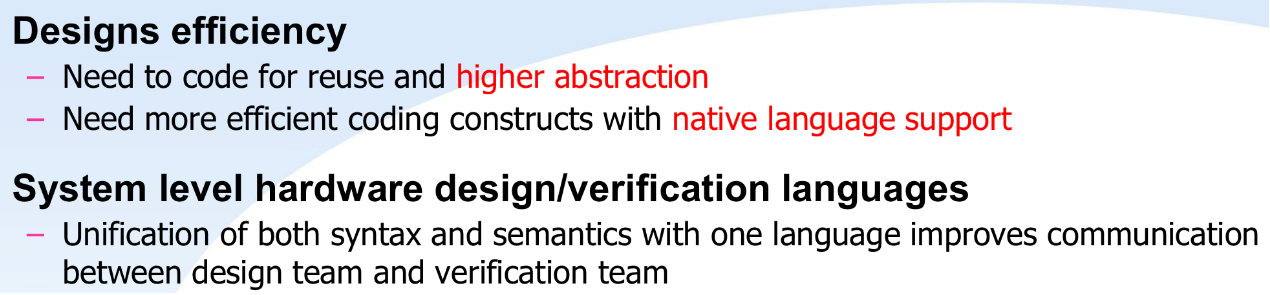
#2019 FALL



Q: Please explain how System Verilog can improve

a. Designs efficiency

b. Design/Verification communication

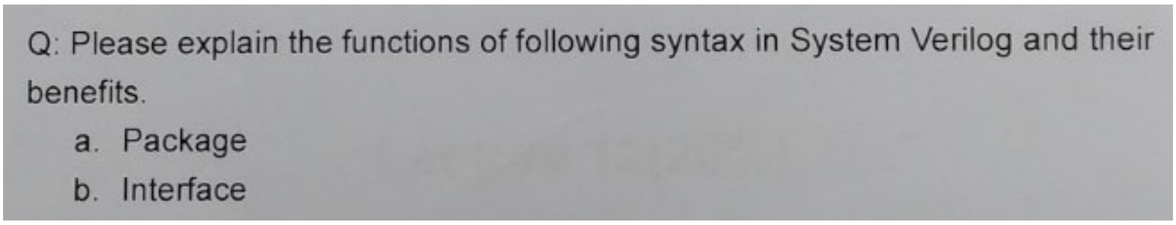


Designs efficiency

- Need to code for reuse and higher abstraction
- Need more efficient coding constructs with native language support

System level hardware design/verification languages

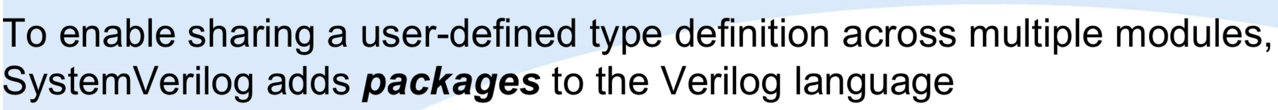
- Unification of both syntax and semantics with one language improves communication between design team and verification team



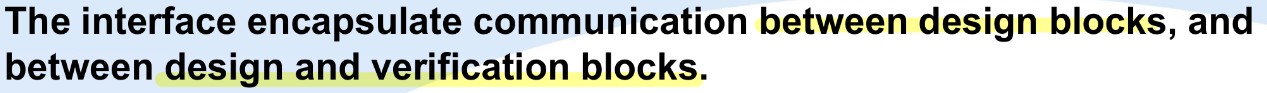
Q: Please explain the functions of following syntax in System Verilog and their benefits.

a. Package

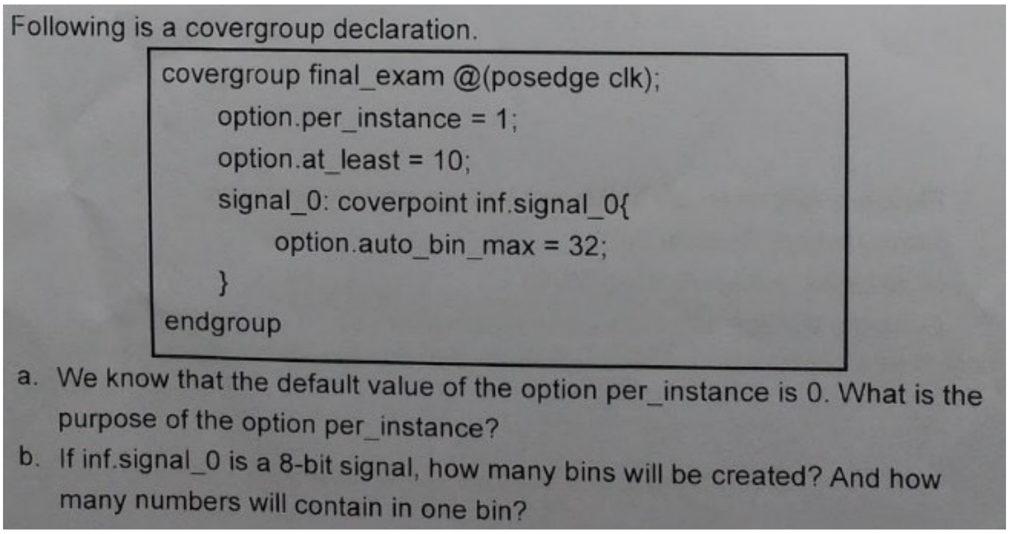
b. Interface

a) 

To enable sharing a user-defined type definition across multiple modules, SystemVerilog adds ***packages*** to the Verilog language

b) 

The interface encapsulate communication between design blocks, and between design and verification blocks.



Following is a covergroup declaration.

```
covergroup final_exam @(posedge clk);
    option.per_instance = 1;
    option.at_least = 10;
    signal_0: coverpoint inf.signal_0{
        option.auto_bin_max = 32;
    }
endgroup
```

a. We know that the default value of the option per_instance is 0. What is the purpose of the option per_instance?

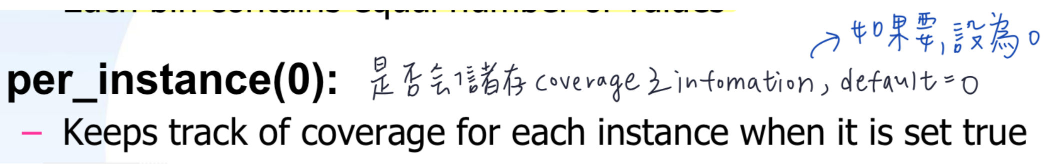
b. If inf.signal_0 is a 8-bit signal, how many bins will be created? And how many numbers will contain in one bin?

b) 8-bit Var

→ $2^8 = 256$ values

min(32, 256) = 32 bins

256/32 = 8/bin

a) 

Each bin contains equal number of values

↗如果要,設為0

per_instance(0): 是否会儲存coverage之infomation, default=0

- Keeps track of coverage for each instance when it is set true