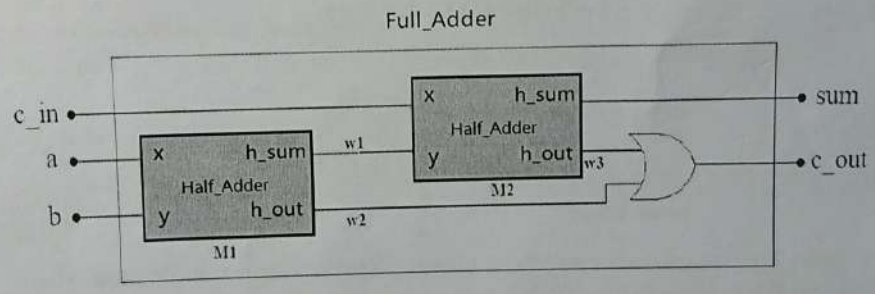
劉力瑋 | 9 | 4

ICLAB 2017Fall Midterm Exam

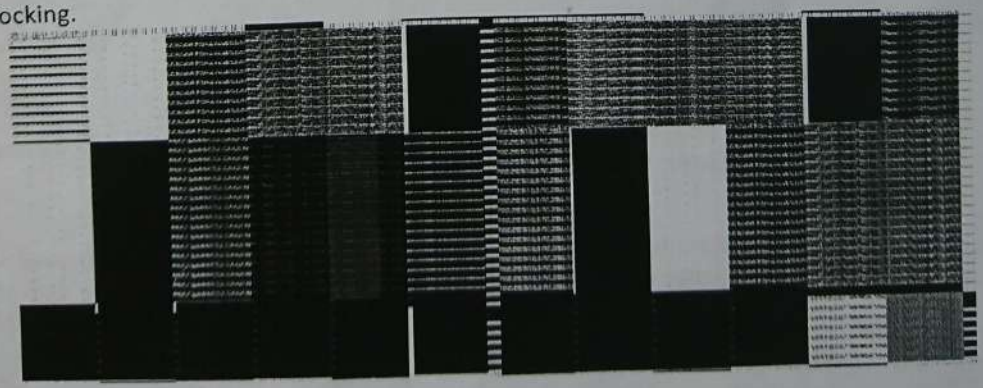
Name: **Student ID:**

1. [15%] Please answer the following questions:
   a. [5%] Why we need different delay time Mid/Typ/Max for our synthesis?
   b. [5%] What is the different between "==' and '==='in Verilog?
   c. [5%] Why don't we use array as memory? (Please describe two major reasons)
2. [10%] Write down the following circuit scheme by calling the module "Half_Adder". Please follow the name list.

Module1 name: Full_Adder
Input : a , b , c_in
Output: sum , c_out
Module2 name: Half_Adder
Input : x , y
Output: h_sum , h_out



3. [10%] Please calculate the value of each node in different clock cycle for non-blocking and blocking.



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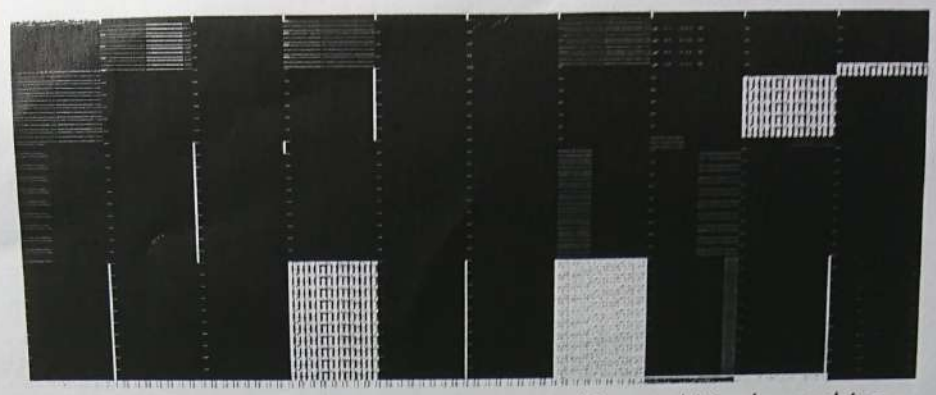

4. [5%] Please describe the differences between Moore machine and Mealy machine.

5. [5%] Please simply describe their roles in design environment (PATTERN.v, TESTBENCH.v, RTL.v)
6. [5%] Please list at least two differences between task and function
7. [10%] Timescale is very important in hardware design, so it is necessary to set the right timescale while designing your architecture.

```
`timescale 1ns/XXXps
module TEST
        parameter CYCLE = 2.45;
        reg     CLK;
        initial   CLK = 0;
        always #(CYCLE/2.0) CLK = ~CLK;
endmodule
```

   a. [5%] Try to explain the two parts (1ns/XXXps) of command `timescale
   b. [5%] What is the value of XXX for precision requirement?

8. [10%] Timing
   a. [5%] Please briefly explain the term **skew time**.
   b. [5%] How to fix **setup time violation** and **hold time violation**?
9. [5%] Please list three kinds of **IP (Intellectual Property)** and briefly explain their **difference (two** features for each one).
10. [5%] Please state the main reason why hardware designers prefer to use SRAMs instead of registers to implement large storage. Also, if we would like to storage 1500*16-bit data in a SRAM which has the same architecture in Lab5, how many input pins and address pins do we need? List one possible solution.

urse Name

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10	36
11	2
12	8

11. [10%] The following module is an image processor. **CONV_IM** is a large combinational circuit and it will convolute the image **im** with the filter **f** then store the results in the SRAM RA1SH. The **wen_sram** and the address **addr** will control the module in write mode or read mode. **POST_IM** is a large combinational circuit and function as a post image processor. Assuming the functionality of the submodules **CONV_IM** and **POST_IM** are correct. What are the potential problems in the Verilog code below? Please propose some solutions to fix those problems.

```
module image_processor (clk, im, f, addr, wen_sram, post_out) begin
input [1023:0] im;
input [5:0] f;
input [1023:0] addr;
input wen_sram;
output [1023:0] post_out;
wire [1023:0] im_out;

CONV_IM conv_im1( .output(im_out), .image(im), .filter(f) ) ;
RA1SH U1(.Q(sram_out),
         .CLK(clk),
         .CEN(1'b0),
         .WEN(wen_sram),
         .A(addr),
         .D(im_out),
         .OEN(1'b0));
POST_IM post_im1(.output(post_out), .input(sram_out));
end
```

12. [10%] Optimize the design

    a. [5%] Please list three methods to resolve **multiple instances** before running the compile command.

    b. [5%] Among synthesis algorithm, using **compile_ultra** command can maximize performance and minimize area. However, when will designer choose to use **compile** command instead of **compile_ultra**?

1.

a. 因為有製程變異，所以我們會用不同 delay time 來做 timing closure，使設計更 reliable。 +5

b. "==" 會將 x, z 視為 don't care (0或1)，而 "===" 必須在兩邊都為 x 或兩邊都為 z 才會成立，適用於 Testbench +0

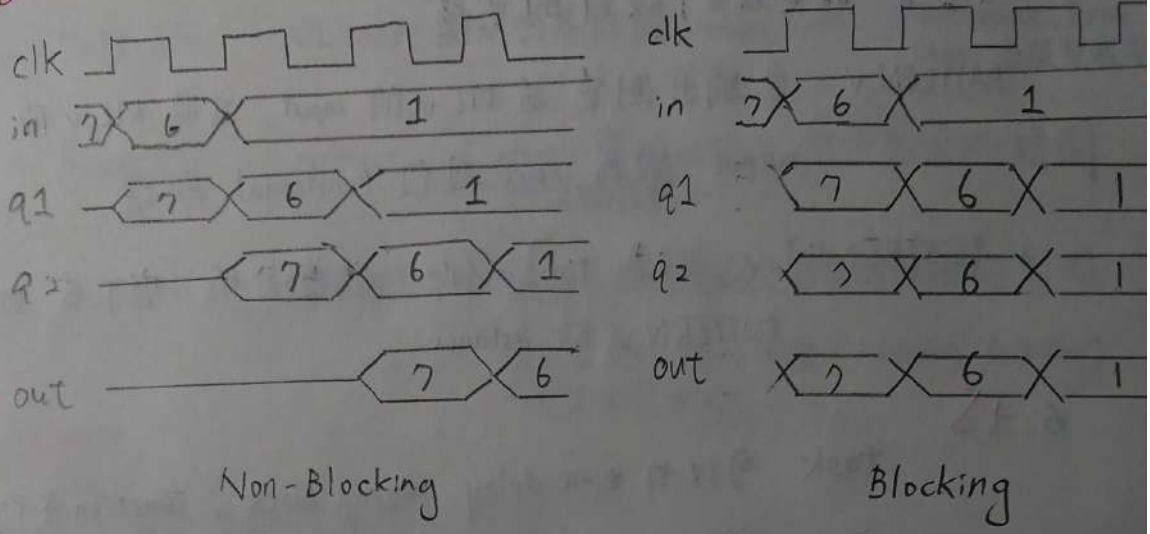
c. 用 array 來做 memory 的缺點是 "面積大"，"功耗較多" +1.5

2. include?

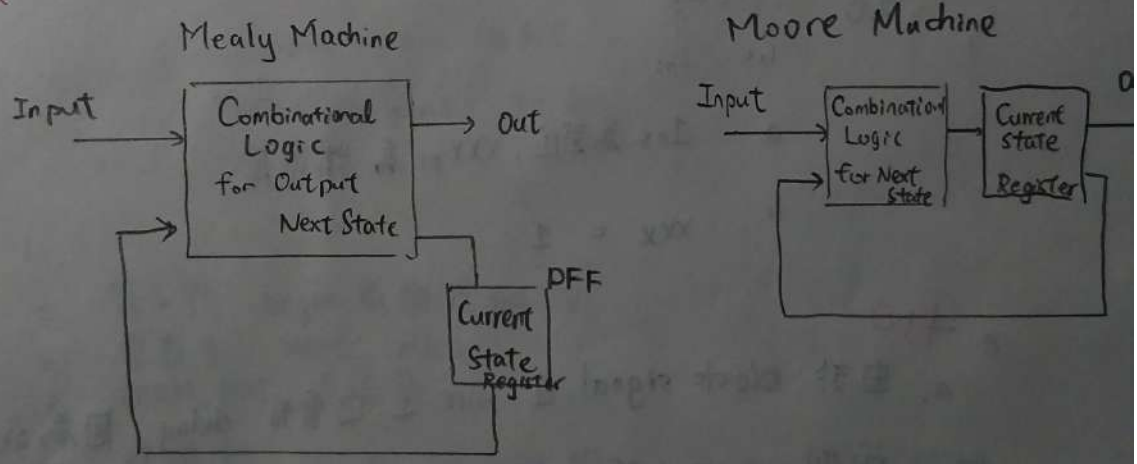
```
module Full_Adder ( a, b, c_in , sum , c_out );
input  a, b, c_in ;
output  sum, c_out ;

wire  w1, w2, w3;

Half_Adder M1(.x(a), .y(b), .h_sum(w1), .h_out(w2))
Half_Adder M2(.x(c_in), .y(w1), .h_sum(sum), .h_out(w3

   or    or1( c_out , w3 , w2 );

endmodule
```

+8

3. +10

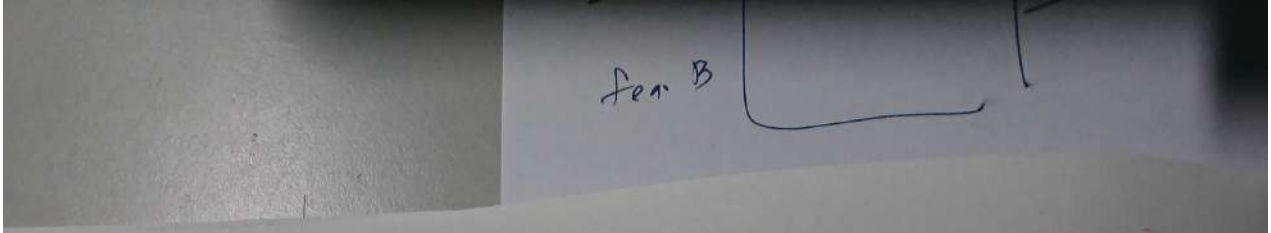


4. +5



Mealy Machine 的 output 由 input 跟 current state 決定

Moore Machine 的 output 由 current state 決定



5. +5

RTL.v 就是我們設計的電路

PATTERN.v 會輸出測資給 RTL.v 的 input，並將 RTL.v 的 output 做為 input 進行 functional 驗證

TESTBENCH.v 做為 top module，像鏡頭般，底下有 RTL.v 與 PATTERN.v 的 instance.

6. +5

task 可以有 time delay, always block., function 不行

task 可以呼叫 task 或 function, function 只可呼叫 f

7. +10

$$\frac{2.45}{2.0} = 1.225$$

1 ns　1 ps

a. 1ns 為單位，XXX ps 為精準度

b. xxx = 1

8. +10

a. 由於 clock signal 在 wire 上也會有 delay，因為我們兩個 register 間的 clock delay 稱為 skew time

b.

setup time violation : Pipeline, Retiming

Hold time violation : 加 Buffer.

9. +5

Soft IP　RTL code　① 適用於不同 technology node　② Performance、Timing、Area 會隨製程變動

Firm IP　Netlist　① Synthesis 後的 netlist　② 可節省合成時間，修改幅度較小

Hard IP　LEF、GDSII　① Layout 後的電路，受限於使用的製程

② 只可在 APR 階段修改（Flipping、Rotating），修改幅度最小

10. +5

a. 因為 SRAM 的面積較小。

b. 16 bit, 1500 word

⇒ $\log_2 1500 \geq 10.xxx$ ⇒ 11 bit Address

input pins : 16 bit

address pins : 11 bit

11. +10

1. 第一行 begin 前面要加 ;
2. 要宣告 input clk;
3. sram_out 未宣告。
4. 建議將 RA1SH 的 input 與 output 用 register 隔開，避免在 Post Synthesis Simulation 因為 delay 產生非預期的結果

3. 加 endmodule 於最後。

6. 把 begin end 拿掉

fea B

12 +10

a. uniquify

set_dont_touch

ungroup

b. 當希望電路保留原本的 Hierarchy 時，會使用 compile