12. [9%] Nondeterminnistic constant is very useful during formal testing.
Please use this concept to declare a 4 bits signal DVAL and write an assertion to check if data comes in the fifo, eventually must come out .

(the input of fifo is data_in and output of fifo is data_out , they are also 4 bits)

addr紀錄目前到哪?

Assertion1: assertion property (@(posedge clk)) ..... ;

#2019 FALL

Q: Please explain how System Verilog can improve
a. Designs efficiency
b. Design/Verification communication

Designs efficiency
- Need to code for reuse and higher abstraction
- Need more efficient coding constructs with native language support

System level hardware design/verification languages
- Unification of both syntax and semantics with one language improves communication between design team and verification team

Q: Please explain the functions of following syntax in System Verilog and their benefits.
a. Package
b. Interface

a) To enable sharing a user-defined type definition across multiple modules, SystemVerilog adds ***packages*** to the Verilog language

b) **The interface encapsulate communication between design blocks, and between design and verification blocks.**

Following is a covergroup declaration.

```
covergroup final_exam @(posedge clk);
    option.per_instance = 1;
    option.at_least = 10;
    signal_0: coverpoint inf.signal_0{
        option.auto_bin_max = 32;
    }
endgroup
```

a. We know that the default value of the option per_instance is 0. What is the purpose of the option per_instance?
b. If inf.signal_0 is a 8-bit signal, how many bins will be created? And how many numbers will contain in one bin?

b) 8-bit Var
→ $2^8 = 256$ values
min(32, 256) = 32 bins
256/32 = 8/bin

a)

per_instance(0): 是否紀錄存 coverage之infomation, default=0 ↗如果要設為0
- Keeps track of coverage for each instance when it is set true

Please explain what is cross talk, and list at least three solutions.

CTS routing

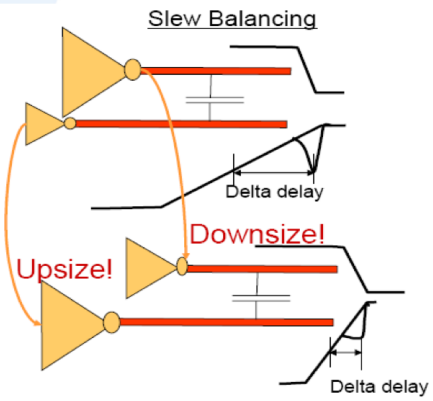
Crosstalk prevention – Placement solution

- Insert buffer in lines
- Upsize driver
- Congestion optimization

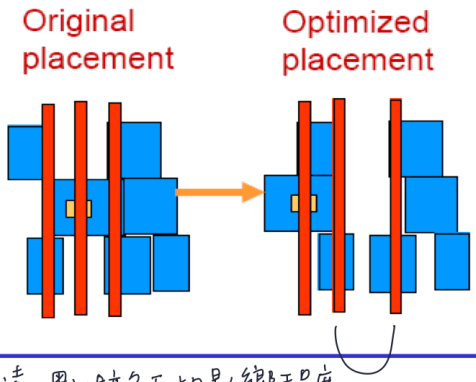
如果2 signals，其一 driving能力較弱
就容易被其它signals影響，造成其
transition time很長
⇒ 調整buffer, inverter大小
讓每條signals transition time差不多

Crosstalk prevention – Routing solution

- Limit length of parallel nets
- Wider routing grid
- Shield special nets



• Reduce coupling capacitance

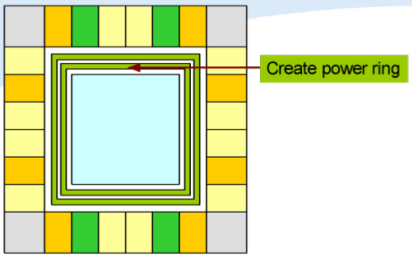


有空間拉遠一點避免互相影響程度

Please describe the benefits of using **wire group** and **interleaving** on power ring.

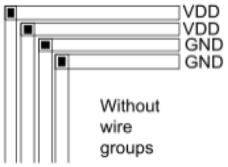
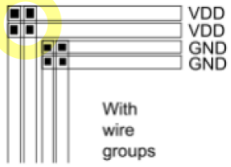
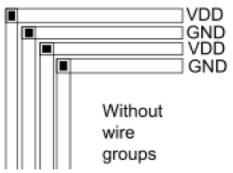
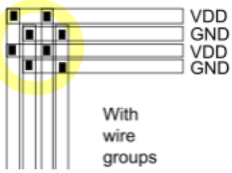
CTS routing

4.2. Core Power Ring



可以降低power ring上的電阻

- Interleaving and Wire group 更加improve power ring的效果

	Without Wire group	With Wire group
Without Interleaving		
Interleaving		

交錯，VDD,GND間就能有很大的decoverling電容讓電源更穩定