ICLAB 2019 Spring

Paper Based Exam

Total Score : 115

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1. Please clearly explain what is cell-based and full-custom. [3%] What is the advantage and disadvantage of them? [3%]
2. There are three code below. If there is any syntax error, please find error and correct it. Otherwise, if the code is correct, you need to write down correct. [6%]

(a)

```
module MUX2_1(out,a,b,sel,clk,rst);
input       sel,clk,rst;
input       a,b;
output      out;
wire        c;
reg         a,b;
reg         out;

assign  c = (sel==1'b0)?a:b;

always@(posedge rst or posedge clk)
begin
            if(reset==1'b1) out <= 0;
            else out <= c;
end
endmodule
```

(b)

```
always @(posedge clk or negedge rst_n) begin
        if(!rst_n) out <= 0;
        else if(sel==0) out <= out + 1;
        else out <= 0;
end
always @(posedge clk or negedge rst_n) begin
        if(!rst_n) out <= 0;
        else if(sel==1) out <= out + 2;
        else out <= 0;
end
```

(b) [8%] Give the following formulas in terms of (t_{cycle}: clock cycle、t_{setup}: setup time、t_{hold}: hold time、t_{pcq}: clk-to-Q propagation delay、t_{ccq}: clk-to-Q contamination delay、t_{pd}: logic propagation delay、t_{cd}: logic contamination delay).

	Setup time	Hold time
Data required time =		
Data arrival time =		

11. [12%] Please complete the SRAM logic table below, and clearly explain each mode

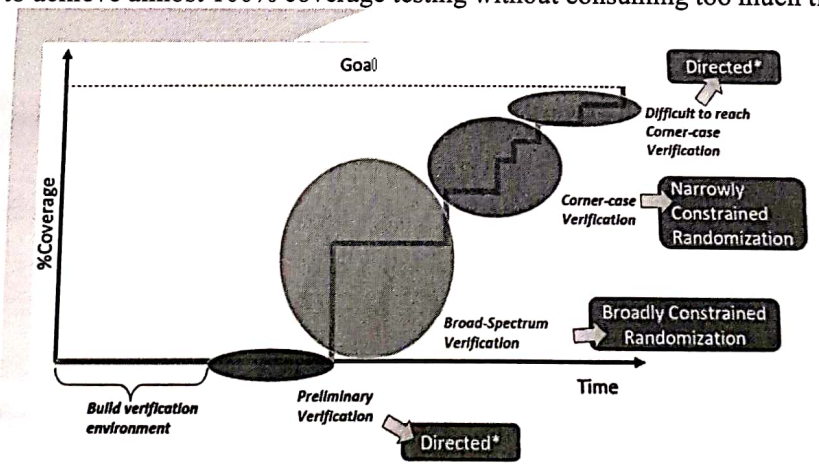
CEN	WEN	OEN	Data Out	Mode	Detailed explanation

12. [12%] For the following three stage, what kind of file do we need if we want to use SRAM in our design?(1%) How do we get those files?(1%) Why do we need these files? Please clearly indicate them one by one.(2%)
    (1) [4%] RTL simulation
    (2) [4%] Synthesis and STA
    (3) [4%] Gate level simulation
13. [10%] After synthesis, what kind of output files should be generate? Please list these files and explain the content and the purpose of these files.
14. [5%] Please explain in what kind of situation do we need to use the command"set hdlin_auto_save_templates TRUE" ?

(c)

```
module DESIGN( clk, rst, in_a, in_b, in_sel, out);

input in_a, in_b, in_sel;
input rst, clk;
output reg out;

reg 2_to_1;

assign out=(rst==1'b1)? 1'b0:2_to_1;
always @(posedge clk or posedge rst) begin
    mux_task;
end

task mux_task;
begin
    if(in_sel==0)    2_to_1 = in_a;
    else             2_to_1 = in_b;
end
endtask

endmodule
```

3. [10%] Please answer the following questions:
   a. [3%]Does the **reg** type always be synthesised as register after synthesis stage? Why?
   b. [3%]Why do we need application specific integral circuit (ASIC) ? What can we benefit from using ASIC?
   c. [4%]What is the difference between '= =' and '= = =' in Verilog? In what circumstance will we use '= = =' instead of '= ='?
4. [6%] Please briefly introduce and list one advantage and two disadvantage of synchronous reset.
5. [5%] Please draw the diagram of mealy and moore machine and simply compare the difference between them.
6. *[6%] Please explain what situation will cause latch in your design and how to fix this problem.*
7. *[8%]Please write down at least four elements of a functioning pattern file (there are six elements in total in the pdf), and specify the purpose of each element.*
8. *[10%]Please write down two kinds of testing pattern strategies and explain why do we need both strategies to achieve almost 100% coverage testing without consuming too much time.*



9. [5%]What is the meaning of the following commands, in what situation will we need to add them ?
   //synopsys translate_off
   //synopsys translate_on

10. (a) [6%] Briefly describe what clk-to-Q contamination delay and logic contamination delay are?