Digital Signal Processing in VLSI Design

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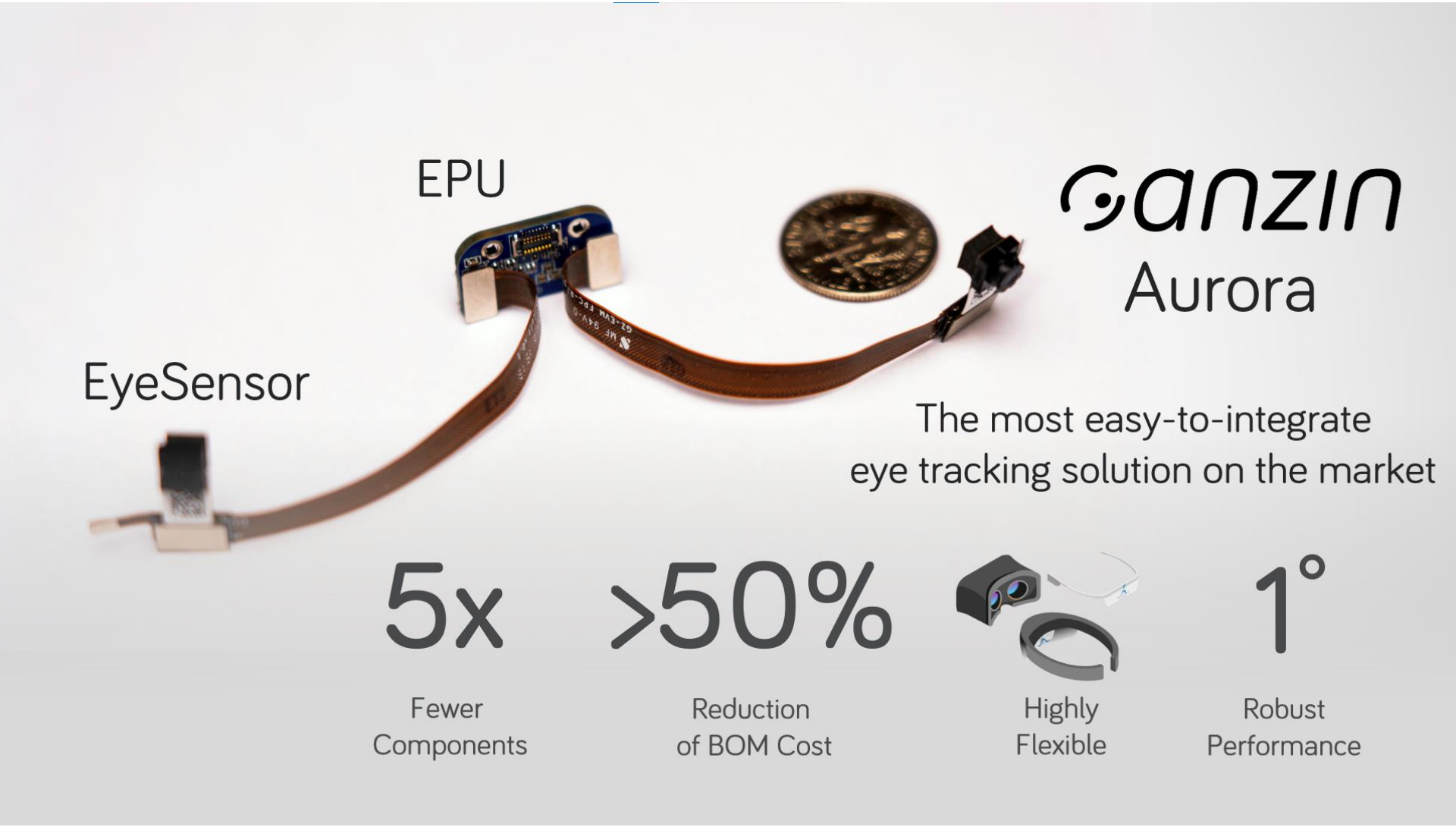
Fall 2023

打造鋼鐵人、柯南眼鏡不是夢！台大師生看好「眼球追蹤」技術齊心創業

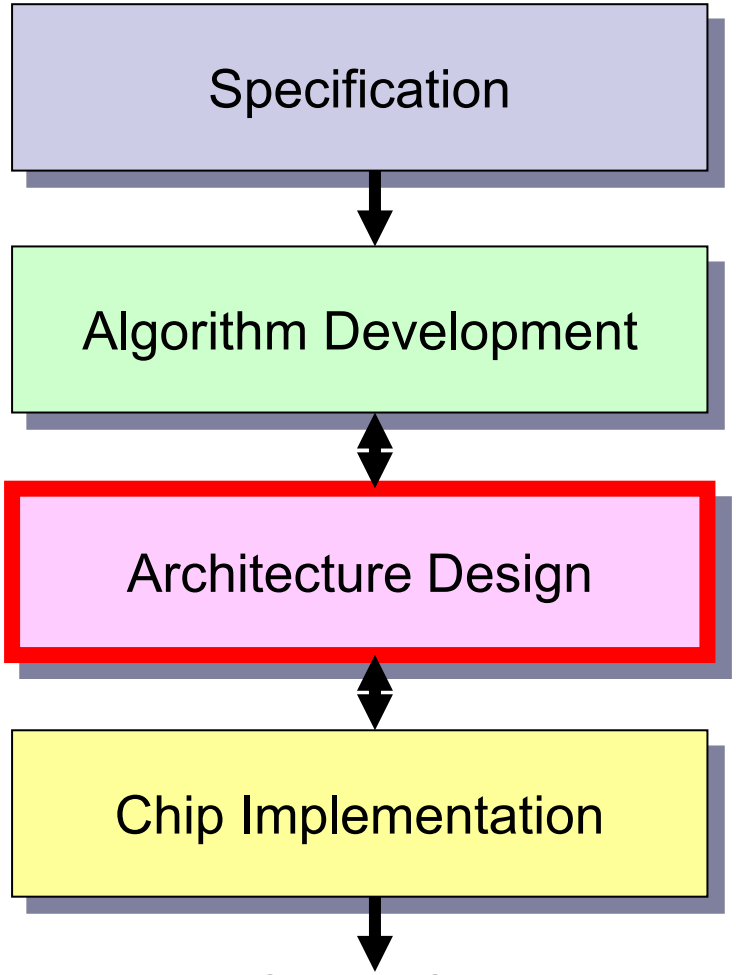
---數位時代創業小聚2020/07/20


EPU
EyeSensor
ganzin
Aurora
The most easy-to-integrate
eye tracking solution on the market
5x
Fewer
Components
>50%
Reduction
of BOM Cost
Highly
Flexible
1°
Robust
Performance

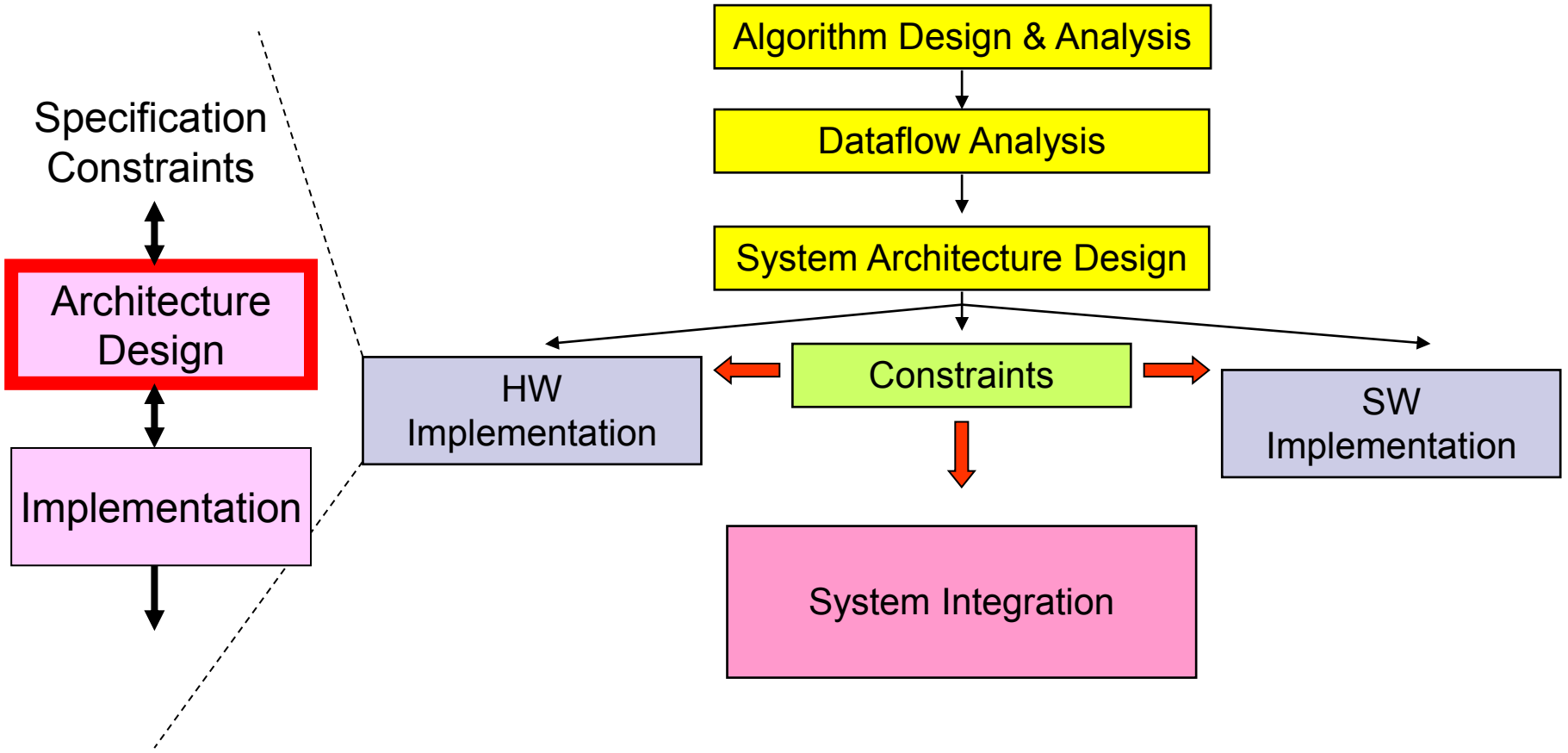
Targets of This Course

- Introduction to the design skills of digital signal processing VLSI systems
- The main focuses of this course are **VLSI hardware architectures for DSP**, not DSP algorithms, and not general-purpose digital signal processor (DSP) design

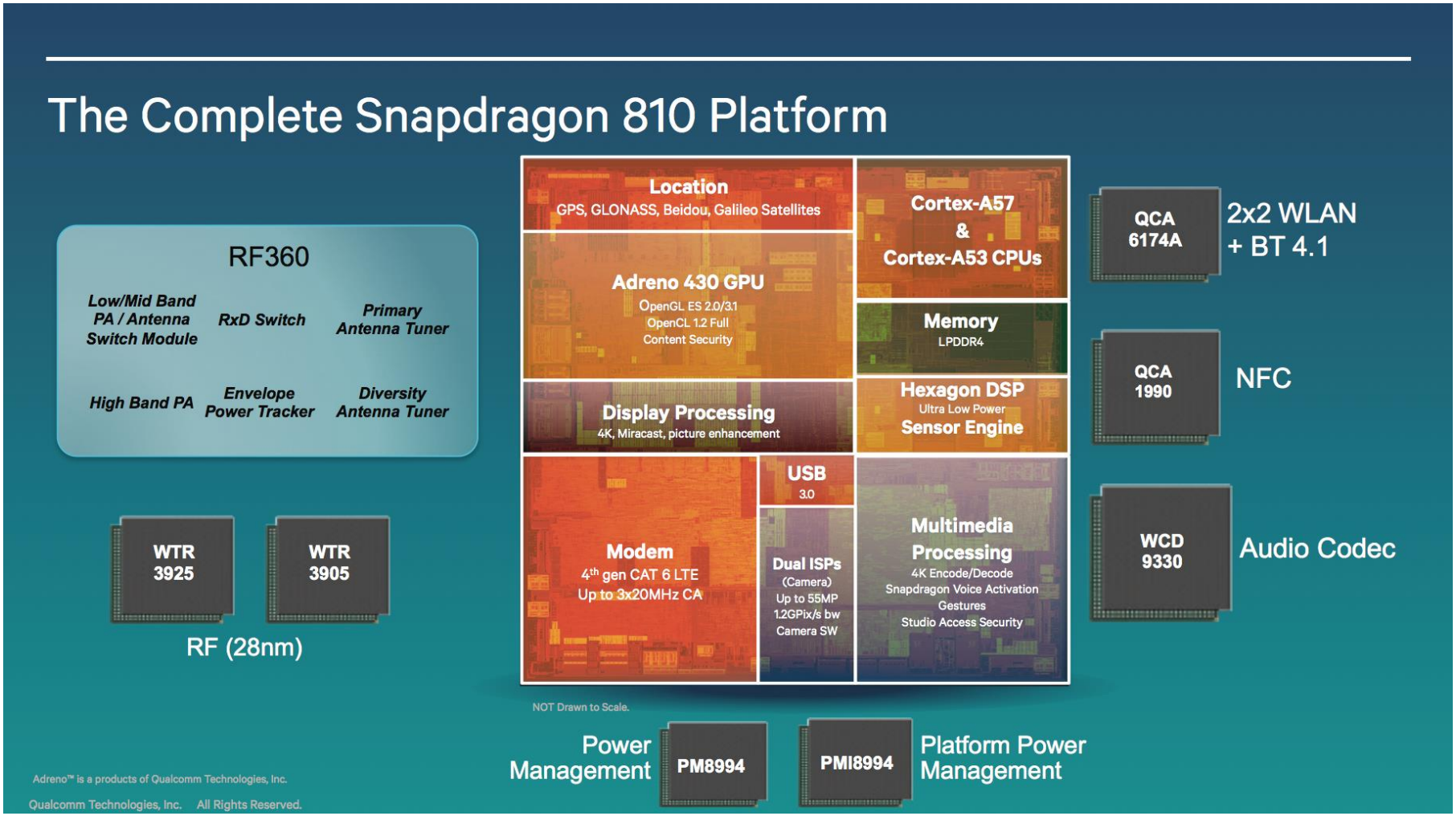
Role of Architecture Design -- From ASIC Point of View



Role of Architecture Design -- From SoC Point of View



In an SoC, the Role of DSP Architecture?

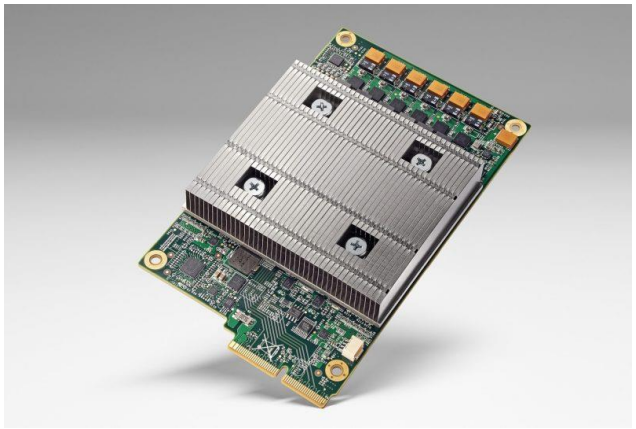


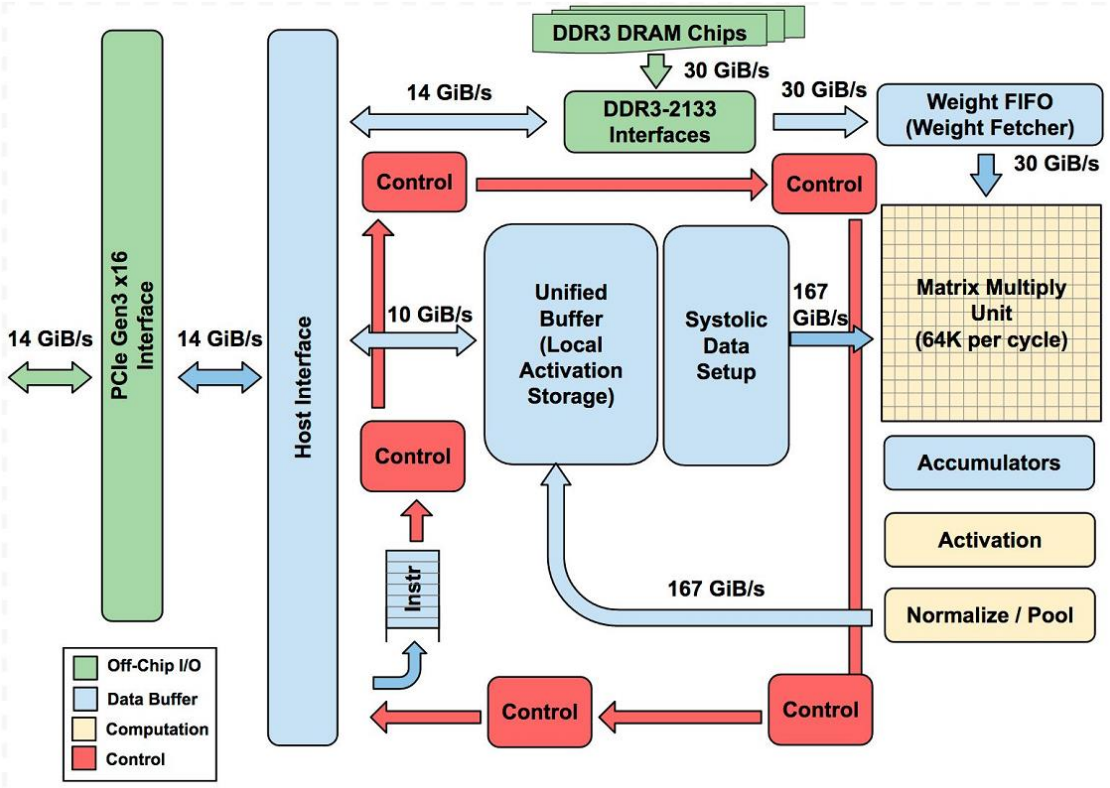
Architecture Design?

- Computer architecture "programmable"
- DSP architecture
- The boundary is getting blur

Example: Google TPU

Systolic Array





Course Outline (1/2)

- ***Part I: Basic Design Skills***
- Introduction to digital signal processing systems
- Iteration bound
- Pipeline and parallel processing
- Retiming
- Unfolding
- Folding
- Systolic array architecture
- Scheduling and resource allocation
- Processing element design
- SoC and DSP architecture

Course Outline (2/2)

- ***Part II: Case Study***
- Case study
  - FFT
  - Motion estimator
  - Neural network

Schedule

Week	Date	Topic
1	9/8	Introduction to digital signal processing systems
2	9/15	Iteration bound
3	9/22	Pipeline and parallel processing/Retiming
4	9/29	中秋節
5	10/6	Unfolding
6	10/13	Folding
7	10/20	Systolic array architecture
8	10/27	Scheduling and resource allocation
9	11/3	Processing element design
10	11/10	SoC and DSP Architecture (I)
11	11/17	Midterm Exam
12	11/24	SoC and DSP Architecture (II)
13	12/1	FFT
14	12/8	Motion Estimator
15	12/15	Neural Network Architecture
16	12/22	Final presentation

行程有可能修改，請隨時注意NTU Cool訊息

Grading

- Homework 40%
  - About 10 homeworks
- Midterm 35%
- Final project 25%

Course Website and Lectures

- Course website: https://cool.ntu.edu.tw/courses/32765
- Pre-recorded courseware on the website and on-site/on-line lectures
- Will record the lecture

References

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- P. Lapsley, J. Bier, A. Shoham, E. A. Lee, ***DSP Processor Fundamentals***, IEEE Press, 1996.
- L.-G. Chen, C.-T. Huang, C.-Y. Chen, and C.-C. Cheng, ***VLSI Design of Wavelet Transform***, Imperial College Press, 2006.
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- Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, and Joel S. Emer, **Efficient Processing of Deep Neural Networks**, Morgan & Claypool Publishers, 2020.
- Related papers