# DSP in VLSI Design
## Homework (III)

## Pipelining and Parallel Processing

Deadline: Oct. 6

1. Consider a direct-form implementation of the FIR filter

$$y(n) = ax(n) + bx(n-2) + cx(n-3)$$

Assume that the time required for 1 multiply-add operation is T.

(a) Pipeline this filter such that the clock period is approximately T.

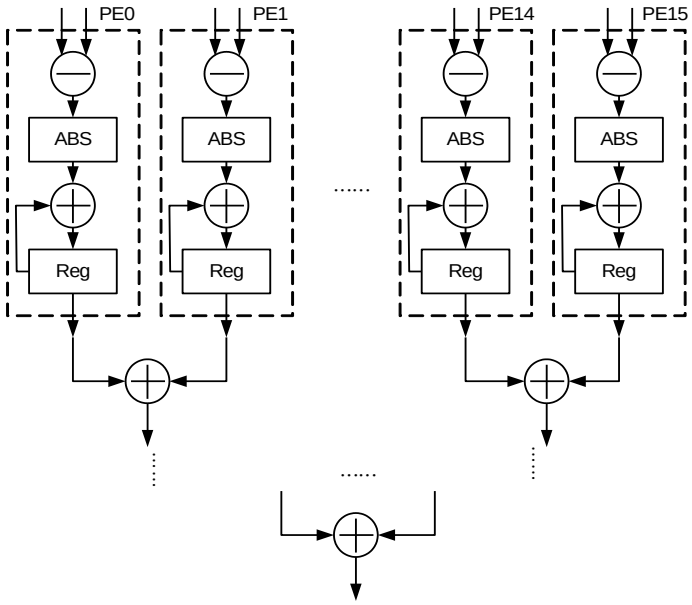
(b) Draw a block filter architecture for a block size of three. Pipeline this block filter such that the clock period is about T. What is the system sampling rate?

(c) Pipeline the block filter in part (b) such that the block period is about T/2. Show the appropriate cutsets and label the outputs clearly. What is the system sampling rate now? (Hint: you can use fine-grain pipelining.)

2. Consider the core of a systolic array motion estimation architecture shown in the following figure. Assume the computation time of subtractor, absolutor, and adder are 5ns, 7ns, and 6ns, respectively.

(a) Where is the critical path? What is the maximum working frequency of this circuit?

(b) If we want to double the working frequency with pipelining, please design the associated architecture.



3. Consider the 6-th-order FIR filter

$$y(n) = ax(n) + bx(n-4) + cx(n-6).$$

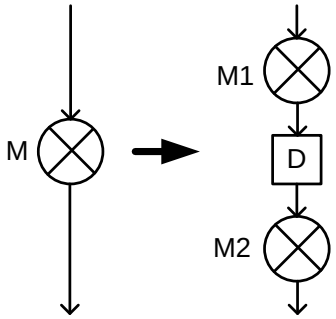
Draw the block diagram of this filter for block size of 3.

4. For the example shown in Page 30 in the handout, with the same sampling period (9 u.t.),

(a) How is the new supply voltage?

(b) How is the power saving percentage?

We then employ fine-grained pipelining technique to further reduce the power consumption, that is, each multiplier is replaced with a pipelined multiplier as follows:




where $T_M$=8 u.t., $T_{M1}$=$T_{M2}$=4 u.t.; $C_M$=8$C_A$, $C_{M1}$=$C_{M2}$=4$C_A$

(c) How is the new supply voltage?

(d) How is the power saving percentage?

5. This example can give you more insights of the advantages of multi-core processors. Assume we have two processors fabricated in the same process with the threshold voltage in 1V. Processor A is a single-core processor with the supply voltage of 5V. For executing one specific task, the dynamic power consumption is 1W, where the static power consumption is 200mW, and the execution time is 10S. Processor B is a new design with four cores. We assume that the task can be perfectly executed in parallel, and there is no extra data accessing overhead for executing the same specific task on the quad-core processor. It is also assumed that the leakage current over unit circuit area is a constant.

a) If Processor B employs the same supplied voltage. What are the advantages of the new design in terms of processing speed and energy consumption?

b) If it is allowed to lower the supply voltage to 4V for Processor B. What are the advantages of the new design in terms of processing speed and energy consumption?