```
1
2   module rateDivider (enable, clock);
3      input clock;
4      output reg enable;
5      reg [26:0] counter;
6
7      always @(posedge clock)
8         begin
9            if(counter == 0) begin
10              counter <= 27'd1000000;
11              enable <= 1;
12           end
13           else begin
14              counter <= counter - 1;
15              enable <= 0;
16        end
17        end
18  endmodule
19
20  module MarioJumpRateDivider (enable, clock);
21     input clock;
22     output reg enable;
23     reg [26:0] counter;
24
25     always @(posedge clock)
26        begin
27           if(counter == 0) begin
28              counter <= 27'd10000;
29              enable <= 1;
30           end
31           else begin
32              counter <= counter - 1;
33              enable <= 0;
34        end
35        end
36  endmodule
```