73

```
//Creators: Hannah Brooks, Wasif Butt
     //if you steal this ill be very upset
 3
 4
     module project
 5
 6
            CLOCK_50,
                                           // On Board 50 MHz
 7
            SW,
 8
            KEY
                                           // On Board Keys
 9
            LEDR,
10
            VGA_CLK,
                                           // VGA clock
11
            VGA_HS,
                                           // VGA H_SYNC
12
            VGA_VS,
                                           // VGA V_SYNC
13
            VGA_BLANK_N,
                                           // VGA BLANK
            VGA_SYNC_N,
14
                                           // VGA SYNC
                                           // VGA Red[9:0]
// VGA Green[9:0]
15
            VGA_R,
16
            VGA_G,
                                           // VGA Blue[9:0]
17
            VGA_B,
            PS2_CLK,
PS2_DAT,
18
19
20
            AUD_ADCDAT,
21
22
            // Bidirectionals
23
            AUD_BCLK,
24
            AUD_ADCLRCK,
25
            AUD_DACLRCK,
26
27
28
            FPGA_I2C_SDAT,
29
            // Outputs
30
            AUD_XCK,
31
            AUD_DACDAT,
32
33
            FPGA_I2C_SCLK,
            HEXO,
34
35
            HEX1,
36
            HEX2,
37
            HEX3
38
         );
39
         /**********************************
40
         // keyboard wires
41
         wire [7:0] the_command;
wire send_command;
42
43
44
45
         inout
                      PS2_CLK;
46
         inout
                      PS2_DAT;
47
48
         wire
                      command_was_sent;
49
                      error_communication_timed_out;
         wire
50
51
52
53
         wire [7:0] received_data;
         wire
         //VGA stuff
55
                      CLOCK_50;
                                           // 50 MHz
         input
         input [3:0] KEY;
input [9:0] SW;
56
57
         output [9:0] LEDR;
58
59
60
         output
                          VGA_CLK;
                                                  // VGA clock
61
                                                  // VGA H_SYNC
                          VGA_HS;
         output
                          VGA_VS;
                                                  // VGA V_SYNC
62
         output
                                                  // VGA BLANK
// VGA SYNC
// VGA Red[7:0] Changed from 10 to 8-bit DAC
// VGA Green[7:0]
63
         output
                          VGA_BLANK_N;
64
                          VGA_SYNC_N;
         output
                   [7:0] VGA_R;
[7:0] VGA_G;
[7:0] VGA_B;
[6:0] HEXO;
65
         output
66
         output
                                                  // VGA Blue[\bar{7}:0]
67
         output
68
         output
                   \begin{bmatrix} 6:0 \end{bmatrix} HEX1;
69
         output
70
                   [6:0] HEX2;
         output
71
         output
                   [6:0] HEX3;
72
```

```
vga_adapter VGA(
 75
                .resetn(resetn)
 76
               .clock(CLOCK_50),
               .colour(colour),
 78
               .x(x),
               .y(y),
 79
 80
                .plot(writeEn),
                /* Signals for the DAC to drive the monitor. */
 82
                .VGA_R(VGA_R),
 83
                .VGA_G(VGA_G),
 84
                .VGA_B(VGA_B)
 85
                .VGA_HS(VGA_HS),
 86
                .VGA_VS(VGA_VS),
 87
                .VGA_BLANK(VGA_BLANK_N),
 88
                .VGA_SYNC(VGA_SYNC_N),
 89
                .VGA_CLK(VGA_CLK));
            defparam VGA.RESOLUTION = "160x120";
 90
            defparam VGA.MONOCHROME = "FALSE";
 91
 92
            defparam VGA.BITS_PER_COLOUR_CHANNEL = 4;
            defparam VGA.BACKGROUND_IMAGE = "black.mif";
 93
 94
 95
 96
      //*****************************
      , ,
*******
 97
 98
         wire outofBounds, ground;
 99
100
         //keys using keyboard
         reg keyR, keyL, keyUp, keyDown, keySpace;
wire right, left, up, down, spaecbar;
101
102
103
104
         assign right = keyR;
105
         assign left = keyL;
         assign up = keyUp;
106
107
         assign down = keyDown;
108
         assign spacebar = keySpace;
109
110
         PS2_Controller ps2(
111
            // Inputs
            CLOCK_50,
112
113
114
            the_command,
115
            send_command,
116
117
            // Bidirectionals
                                  // PS2 Clock
118
            PS2_CLK,
119
            PS2_DAT,
                                  // PS2 Data
120
121
            // Outputs
122
            command_was_sent,
            error_communication_timed_out,
125
            received_data,
                                     // If 1 - new data has been received
126
            received_data_en
127
128
         reg moving;
130
         always @(posedge received_data_en) begin
131
            if ((received_data == <mark>8'b1111_0000</mark>) && moving == 1)                          begin
132
               keySpace \leq 0;
133
               keyL <= 0;
134
               keyR <= 0;
               keyUp \ll 0;
135
136
               keyDown <= 0;
137
               moving \leftarrow 0;
138
            end
139
            if (moving == 0)
140
               moving <= 1;</pre>
141
            else if ((received_data == 7'b0101001) && start)
142
               keySpace <= 1;
            143
144
               keyDown <= 1;
```

```
else if ((received_data == 7'b1101011) && moving == 1 && (lvl1 || lvl2 || lvl3))
145
146
                   keyL <= 1;
else if ((received_data == 7'b1110100) && moving == 1 && (lvl1 || lvl2 || lvl3))</pre>
147
148
                        keyR <= 1;
                    else if ((received_data == 7'b1110101) && moving == 1 && (1v11 | 1v12 | 1v13)
149
150
                        keyUp <= 1;
151
               end
152
153
154
               //VGA input controlling wires
155
               reg [11:0] colour;
               reg [7:0] x, y;
156
157
               reg writeEn;
158
              wire resetn;
159
               assign resetn = KEY[3];
160
161
               //draw controls
162
              wire resetAddress, resetAddress2, resetAddress3, fall;
              wire drM, drML, jump, jumpL, drStage1; //draw controls level 1 wire drM2, drML2, jump2, jumpL2, drStage2; //draw controls level 2 wire drM3, drML3, jump3, jumpL3, drStage3; //draw controls level 3 wire erM, jumping, a falling pipe, dead; //erase controls level 1
163
164
165
166
              wire erM2, jumping2, falling2, next; //erase controls level 2 wire erM3, jumping3, falling3, flag; //erase controls level wire [11:0] marioColourRight, marioColourLeft, jumpColourRight, jumpColourLeft,
167
168
169
         stage1Colour, stage2Colour, stage3Colour, startColour; //colours
wire [7:0] Mariox, Marioy, Jumpx, Jumpy, lvl1bkgx, lvl1bkgy; //x y controls for drawing
wire moveRight, moveLeft, moveUp; //draw in direction ********TO BE DELETED*******
wire [7:0] px, py; //position tracker for mario
wire [4:0] jumpCounter; //jumping position tracker
wire startEnable, lvl1Enable, lvl2Enable, lvl3Enable; //write enables
170
171
172
173
174
175
176
               //overall FSM controls
177
              wire start, draw, lvl1, lvl2;
178
179
               //counters
180
              wire done;
181
               reg [14:0] address;
182
              wire [14:0] outAddress;
183
184
               //rate divider enable
185
               wire go, goJump:
              wire timer_enable;
186
187
188
               //accessing memories to draw images
189
               mario drawMarioRight(address, CLOCK_50, marioColourRight);
190
               marioLeft drawMarioLeft(address, CLOCK_50, marioColourLeft);
              jump jumpMarioRight(address, CLOCK_50, jumpColourRight); jumpLeft jumpMarioLeft(address, CLOCK_50, jumpColourLeft); start_screen startscreen(address, CLOCK_50, startColour); stage1_bkg stage1(address, CLOCK_50, stage1Colour); stage2_bkg stage2(address, CLOCK_50, stage2Colour); stage3_bkg stage3(address, CLOCK_50, stage3Colour);
191
192
193
194
195
196
197
198
              always @(*) begin
199
                    if (start) begin
200
                        writeEn <= startEnable;</pre>
                        if(draw) begin
201
202
                             colour <= startColour;</pre>
                             x \ll 1v11bkgx;
203
                             y <= lvl1bkgy;
204
205
                             address <= outAddress;</pre>
206
                        end
207
                        else begin
208
                             address <= 0;
209
                             x <= 0;
210
                             y <= 0;
                        end
211
212
                   end
213
                   else if (lvl1) begin
                        writeEn <= lvl1Enable;
214
215
                        if (resetAddress)
216
                             address <= 0;
```

```
else
218
                    address <= outAddress;</pre>
219
                if (drStage1 || erM || jumping || falling) begin
                    colour <= stage1Colour;
                    x <= lvl1bkgx;
                     <= lvl1bkgy;
                end
                else if(drM || drML || jump || jumpL) begin
                    if (jump) begin
                       colour <= jumpColourRight;</pre>
229
                       address <= outAddress;</pre>
230
                    end
                    else if (jumpĻ) begin
231
                       colour <= jumpColourLeft;</pre>
                       address <= outAddress;
234
                    end
235
                    else if (drM) begin
236
                       colour <= marioColourRight;
237
                       address <= outAddress;</pre>
238
                    end
239
                    else begin
240
                       colour <= marioColourLeft;
241
                       address <= outAddress;
                    end
243
244
                   x <= Mariox:
245
                    y <= Marioy;
246
                end
247
             end
248
             else if (1v12) begin
                writeEn <= lvl2Enable;
                if (resetAddress2)
                    address <= 0;
                else
253
                    address <= outAddress;
254
255
                if (drStage2 || erM2 || jumping2 || falling2) begin
                    colour <= stage2Colour;</pre>
                    x \ll 1v \cdot 1bkqx;
258
                     <= lvl1bkgy;
259
                end
260
                else if(drM2 || drML2 || jump2 || jumpL2) begin
261
262
                    if (marioColourRight == 12'b000010101110 && drM2) begin
263
                       address <= outAddress;</pre>
                       colour <= 12'b000000000000;
264
265
                    end
                    else if (marioColourLeft == 12'b000010101110 && drML2) begin
266
267
                       address <= outAddress;</pre>
                       colour <= 12'b000000000000;
268
                    end
                    else if (jumpColourRight == 12'b000010101110 \&\& jump2) begin
                       address <= outAddress;</pre>
                       272
                    end
                    else if (jumpColourLeft == 12'b000010101110 && jumpL2) begin
                       address <= outAddress;</pre>
276
                       colour <= 12'b000000000000;
                   end
277
                    else if (jump2) begin
278
279
                       colour <= jumpColourRight;</pre>
280
                       address <= outAddress;</pre>
281
                    end
282
                    else if (jumpL2) begin
                       colour <= jumpColourLeft;
address <= outAddress;</pre>
283
284
285
                    end
286
                    else if (drM2) begin
287
                       colour <= marioColourRight;
288
                       address <= outAddress;</pre>
289
                    end
```

217

```
290
                                      else begin
291
                                            colour <= marioColourLeft;</pre>
292
                                            address <= outAddress;
293
294
                                      x <= Mariox;
                                         <= Marioy;
                                end
                         end
299
                         else if (lvl3) begin
300
                               writeEn <= lvl3Enable;
                                if (resetAddress3)
301
302
                                      address <= 0;
303
                                else
304
                                      address <= outAddress;
305
                                if (drStage3 || erM3 || jumping3 || falling3) begin
306
307
                                      colour <= stage3Colour;
308
                                      x \ll 1v11bkgx;
                                      y \ll 1v11bkgy;
309
310
311
                                else if(drM3 || drML3 || jump3 || jumpL3) begin
312
                                      if (flag && ((Mariox == 8'd105 && Marioy == 8'd70) || (Mariox == 8'd106 &&
313
            Marioy == 8'd70) \mid Mariox == 8'd105 & Marioy == 8'd71) \mid Mariox == 8'd106 & Marioy == 8'd71) \mid Mariox == 8'd106 & Marioy == 8'd71) \mid Mariox == 8'd70 & Marioy == 8'd71) \mid Mariox == 8'd70 & Marioy == 8'd71) | Mariox == 8'd106 & Marioy == 8'd71) | Mariox == 8'd710 & Mariox == 8'd710
            8'd71))) begin
314
                                             address <= outAddress;
315
                                            colour <= 12'b1011111100001;
316
317
                                      else if (jump3) begin
318
                                            colour <= jumpColourRight;</pre>
319
                                            address <= outAddress;</pre>
320
                                      end
                                      else if (jumpL3) begin
                                            colour <= jumpColourLeft;
                                            address <= outAddress;
324
                                      end
                                      else if (drM3) begin
325
326
                                            colour <= marioColourRight;</pre>
                                            address <= outAddress;</pre>
                                      end
                                      else begin
330
                                            colour <= marioColourLeft;
331
                                            address <= outAddress;</pre>
                                      end
334
                                      x <= Mariox;
335
                                      y <= Marioy;
336
                               end
                         end
337
338
                  end
339
340
                   //FSMs
                   overallFSM overall(CLOCK_50, resetn, spacebar, pipe, next, flag, done, start, draw, lvl1,
341
              lvl2, lvl3, startEnable, dead, timer_énable);
342
343
                   lvl1FSM level1(CLOCK_50, resetn, go, goJump, right, left, up, down,
344
                                                   resetAddress, drM, drML, erM, jump, jumpL, jumping, falling, drStage1,
            moveRight,
345
                                                   done, jumpCounter, fall,
346
                                                   lvl1Enable, rightColour, leftColour, ground, outofBounds, pipe, lvl1,
            start, dead);
347
348
                   lvl2FSM level2(CLOCK_50, resetn, go, goJump, right, left, up, down,
349
                                                   resetAddress2, drM2, drML2, erM2, jump2, jumpL2, jumping2, falling2,
            drStage2, moveRight,
350
                                                   done, jumpCounter, fall,
351
                                                   lvl2Enable, rightColour, leftColour, ground, outofBounds, next, lvl2,
            start);
353
                   lvl3FSM level3(CLOCK_50, resetn, go, goJump, right, left, up, down,
354
                                                   resetAddress3, drM3, drML3, erM3, jump3, jumpL3, jumping3, falling3,
            drStage3, moveRight,
```

```
355
                              done, jumpCounter, fall,
356
                              lvl3Enable, rightColour, leftColour, ground, outofBounds, flag, lvl3,
       start);
357
358
           //datapath
          drawStuff drawObjects(CLOCK_50, drM, drML, erM, jump, jumpL, jumping, falling, drStage1, drM2, drML2, erM2, jump2, jumpL2, jumping2, falling2, drStage2, drM3, drML3, erM3, jump3, jumpL3, jumping3, falling3, drStage3, done, jumpCounter, outAddress, fall, Mariox, Marioy, Jumpx, Jumpy, lvl1bkgx, lvl1bkgy, px, py, draw);
359
360
361
362
363
364
365
           //movement registers
           marioReg marioMovement(CLOCK_50, go, ground, px, py,
366
367
                                 erM, jump, jumpL, jumpCounter, jumping, falling, drStage1, drStage2,
       drStage3,
368
                                 right, left, up, down, outofBounds, pipe, next, flag, start, lvl1, lvl2
       , 1v13, dead);
369
370
371
           //refresh rate divider
372
           rateDivider moverate(go, CLOCK_50);
373
           MarioJumpRateDivider jumprate(goJump, CLOCK_50);
374
375
           //clock
           timer timer(HEXO, HEX1, HEX2, HEX3, CLOCK_50, timer_enable);
376
377
378
           input
                             AUD_ADCDAT;
379
380
           inout
                             AUD_BCLK;
381
           inout
                             AUD_ADCLRCK;
382
           inout
                             AUD_DACLRCK;
383
384
           inout
                             FPGA_I2C_SDAT;
385
386
           output
                                 AUD_XCK;
387
           output
                                 AUD_DACDAT;
388
                                 FPGA_I2C_SCLK;
           output
389
390
           wire
                             audio_in_available;
391
                       31:0
                                 left_channel_audio_in;
           wire
                              right_channel_audio_in;
read_audio_in;
392
           wire
                      [31:0]
393
           wire
394
395
           wire
                              audio_out_allowed;
396
                      [31:0]
                                 left_channel_audio_out;
           wire
                                 right_channel_audio_out;
397
           wire
                      [31:0]
398
           wire
                             write_audio_out;
399
                      [7:0] data_received;
           wire
400
401
           reg [18:0] delay_cnt;
           wire [18:0] delay;
402
403
404
           reg snd;
405
406
           reg [22:0] beatCountMario;
407
           reg [9:0] addressMario;
408
409
           sound r1(.address(addressMario), .clock(CLOCK_50), .q(delay));
410
411
           always @(posedge CLOCK_50)
412
               if(delay_cnt == delay) begin
413
                  delay_cnt <= 0;</pre>
414
                  snd <= !snd;</pre>
415
               end else delay_cnt <= delay_cnt + 1;</pre>
416
           always @(posedge CLOCK_50) begin
  if(beatCountMario == 23'b10011000100101101000000)begin
417
418
                  beatCountMario <= 23'b0:
419
                  if(addressMario < 10'd999)</pre>
420
                      addressMario <= addressMario + 1;</pre>
421
422
                  else begin
423
                      addressMario <= 0;
424
                      beatCountMario <= 0;</pre>
```

```
425
                end
426
            end
427
            else
                beatCountMario <= beatCountMario + 1;</pre>
         end
430
         wire [31:0] sound = snd ? 32'd100000000 : -32'd100000000;
431
432
433
         assign read_audio_in
                                      = audio_in_available & audio_out_allowed;
         assign left_channel_audio_out = left_channel_audio_in+sound;
434
435
         assign right_channel_audio_out = left_channel_audio_in+sound;
436
                                         = audio_in_available & audio_out_allowed;
         assign write_audio_out
437
438
         Audio_Controller Audio_Controller (
439
            // Inputs
440
             .CLOCK_50
                                          (CLOCK_50),
441
                                      (\sim KEY[0]),
             .reset
442
443
             .clear_audio_in_memory
                                         (),
                                      (read_audio_in),
444
             .read_audio_in
445
446
             .clear_audio_out_memory
                                          (left_channel_audio_out)
447
             .left_channel_audio_out
                                         (right_channel_audio_out),
448
             .right_channel_audio_out
449
             .write_audio_out
                                      (write_audio_out),
450
             .AUD_ADCDAT
                                      (AUD_ADCDAT),
451
             // Bidirectionals
             .AUD_BCLK
                                       (AUD_BCLK)
455
             .AUD_ADCLRCK
                                       (AUD_ADCLRCK),
456
             .AUD_DACLRCK
                                      (AUD_DACLRCK),
457
459
            // Outputs
460
             .audio_in_available
                                          (audio_in_available),
             .left_channel_audio_in
                                          (left_channel_audio_in)
461
             .right_channel_audio_in
                                          (right_channel_audio_in),
462
463
464
             .audio_out_allowed
                                          (audio_out_allowed),
465
466
             .AUD_XCK
                                   (AUD_XCK),
                                      (AUD_DACDAT)
467
             .AUD_DACDAT
468
469
         );
470
471
         avconf \#(.USE\_MIC\_INPUT(1)) avc (
472
                                          (FPGA_I2C_SCLK),
             .FPGA_I2C_SCLK
                                          (FPGA_I2C_SDAT),
473
             .FPGA_I2C_SDAT
                                       (CLOCK_50),
474
             .CLOCK_50
475
             .reset
                                      (\sim KEY[0])
         );
477
478
479
      endmodule
480
481
482
483
```