

Hardware in the loop and embedded computing

GIZMO

2021 DE2-Gizmo (Physical Computing)
Lecture 1

Dyson School of
Design Engineering

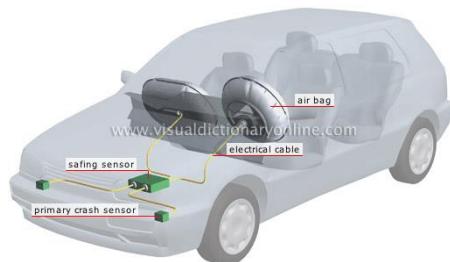
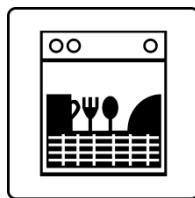
Computers and Software

The most visible use of computers and software is processing information for human consumption



Computers and Software

The vast majority of computers in use, however, are much less visible



Computers and Software

These less visible computers are called **embedded systems**, the software they run is called **embedded software**

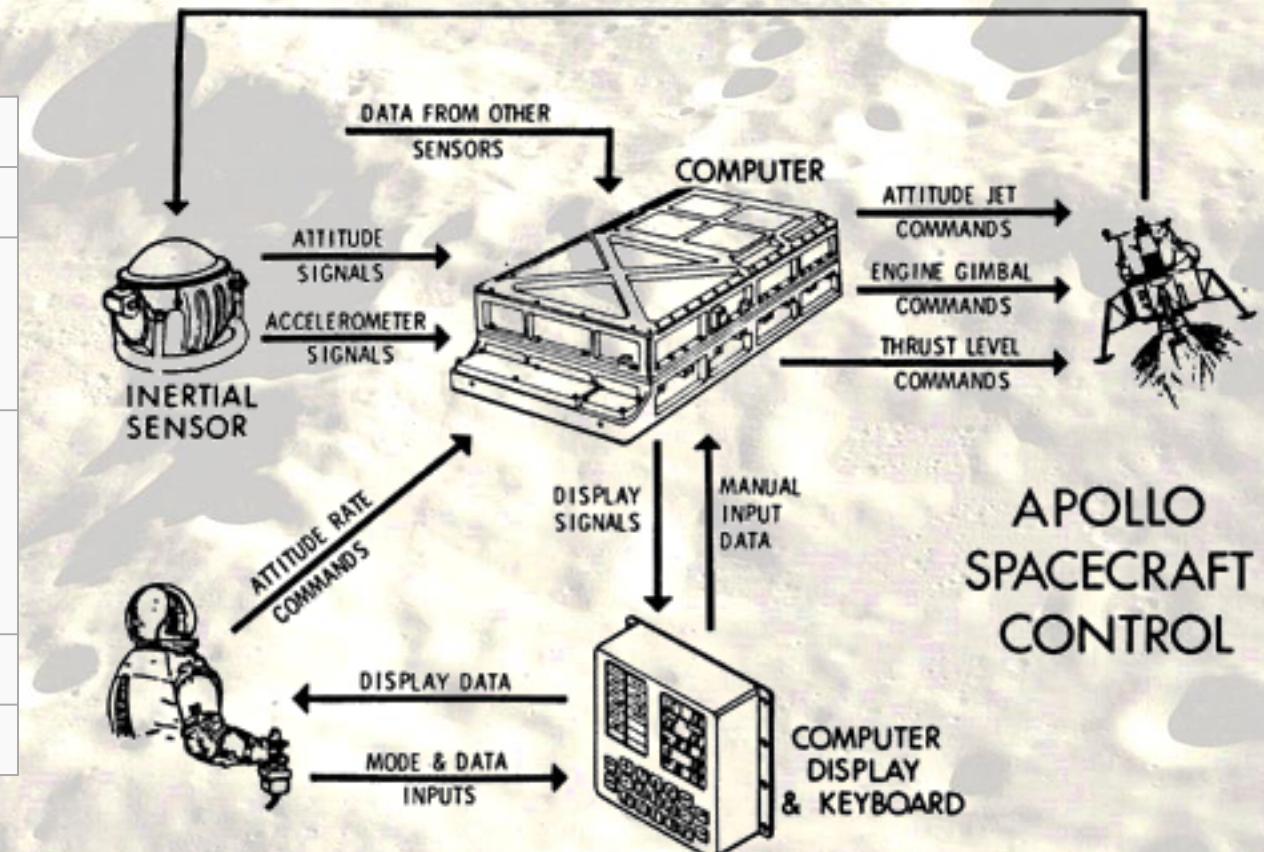
- In use since the 1970s
- First embedded system?
Probably the Apollo Guidance Computer (1966)



Apollo Guidance Computer (1966)

Function: Provide *computation and electronic interfaces* for guidance, navigation, and control of the spacecraft

Processor	Discrete integrated circuit
Frequency	2.048 MHz
Memory	16-bit words, 2048 words RAM, 36,864 words ROM
Ports	DSKY, IMU, Hand Controller, Landing Radar, Telemetry Receiver, Engine Command, etc.
Weight	32 kg
Dimensions	61×32×17 cm



Apollo Guidance
Computer (1966)



Ernst Arm - MH-1 (1961)

The first academic activity in robotics:

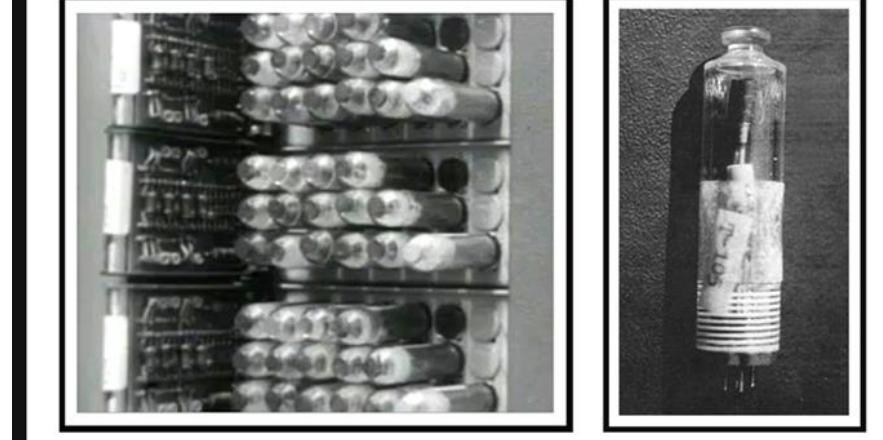
H. A. Ernst, MH-1, A Computer-Operated Mechanical Hand, Ph.D. Thesis, Department of Mechanical Engineering, MIT, 1961

Ernst used a slave arm equipped with touch sensors, and ran it under computer control using a TX-o. The objective was to use the information from the touch sensors to guide the arm

Ernst Arm - MH-1 (1961)



MIT TX-0 Transistorized Computer Built in 1955, Operational in 1956



What is the technological difference between the Apollo Guidance Computer (1966) and MH-1 (1961)?

Integrated Circuit

■ Jack Kilby

- Texas Instruments
- Filed on 6 February 1959
- Awarded on 23 June 1964

■ Robert Noyce

- Fairchild
- Filed on 30 July 1959
- Awarded on 25 April 1961

April 25, 1961
R. N. NOYCE
SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE
Filed July 30, 1959
2,981,877
3 Sheets-Sheet 1

FIG. 1

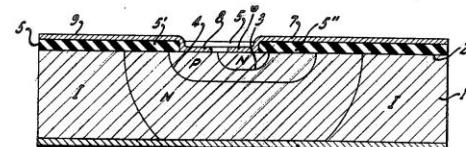
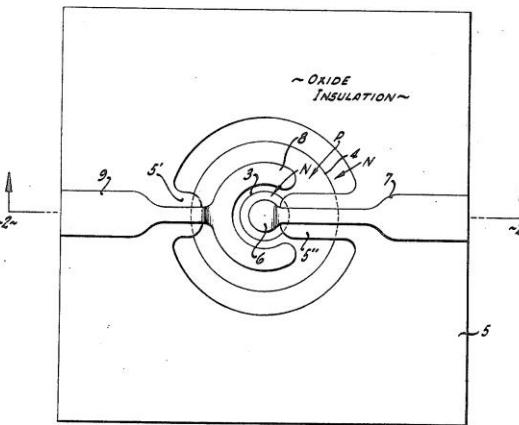


FIG. 2

INVENTOR.
ROBERT N. NOYCE
BY *Leppencott & Ralls*
ATTORNEYS

United States Patent Office

2,981,877

Patented Apr. 25, 1961

1

2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD
STRUCTURE

Robert N. Noyce, Los Altos, Calif., assignor to Fairchild Semiconductor Corporation, Mountain View, Calif., a corporation of Delaware

Filed July 30, 1959, Ser. No. 830,507

10 Claims. (Cl. 317—235)

This invention relates to electrical circuit structures incorporating semiconductor devices. Its principal objects are these: to provide improved device-and-lead structures for making electrical connections to the various semiconductor regions; to make unitary circuit structures more compact and more easily fabricated in small sizes than has heretofore been feasible; and to facilitate the inclusion of numerous semiconductor devices within a single body of material.

In brief, the present invention utilizes dished junctions extending to the surface of a body of extrinsic semiconductor, an insulating surface layer consisting essentially of oxide of the same semiconductor extending across the junctions, and leads in the form of vacuum-deposited or otherwise formed metal strips extending over and adherent to the insulating oxide layer for making electrical connections to and between various regions of the semiconductor body without shorting the junctions.

The invention may be better understood from the following illustrative description and the accompanying drawings.

Fig. 1 of the drawings is a greatly enlarged plan view of a transistor-and-lead structure embodying principles of this invention.

Fig. 2 is a section taken along the line 2—2 of Fig. 1;

Fig. 3 is a greatly enlarged plan view of a multi-device semiconductor-and-lead structure embodying principles of this invention;

Fig. 4 is a section taken along the line 4—4 of Fig. 3;

Fig. 5 is a simplified equivalent circuit of the structure shown in Figs. 3 and 4, with additional circuit elements external to said structure represented by broken lines;

Fig. 6 is a greatly enlarged plan view of another transistor-and-lead structure embodying principles of the invention;

Fig. 7 is a section taken along the line 7—7 of Fig. 6.

Figs. 1 and 2 illustrate one example of a structure according to this invention. A single-crystal body of semiconductor-grade silicon, represented at 1, has a high-quality surface, 2, prepared in accordance with known transistor technology. Within the body 1 there are high-resistivity regions, designated 1 in the drawing, composed either of high-purity silicon having so few donor and acceptor impurities that it is a good insulator at ordinary temperatures, and an intrinsic semiconductor at elevated temperatures, or of somewhat less-pure silicon containing a trace of a material such as gold that diminishes the effect of donor and acceptor impurities by greatly reducing the carrier concentrations.

Elsewhere within body 1, there are extrinsic N-type and extrinsic P-type regions, designated N and P respectively, formed in the well-known manner by diffusing N-type and P-type dopants through surface 2 into the crystal, with appropriate masking to limit the dopant to the desired areas. The smallest and uppermost N-type region constitutes an emitter layer of the transistor. This emitter layer overlies a somewhat larger P-type region which constitutes the base layer of the transistor. The base

layer, in turn, overlies a still larger N-type region which constitutes the collector layer of the transistor. Between the emitter and base layers there is a dished, P-N junction 3, having a circular edge which extends to surface 2 and there completely surrounds the emitter. Between the base and collector layers there is a dished, P-N junction 4, having a circular edge that extends to surface 2 and there completely surrounds the base. The thickness of the emitter and base layers has been exaggerated in the drawings; in actual practice each of these layers is but a few microns thick. The collector layer generally is considerably thicker, and in the example illustrated extends completely through the body 1 so that contact thereto may be made from the back side. Thus, the three extrinsic semiconductor layers described form a transistor equivalent to previously known types of double-diffused junction transistors.

During diffusion of the donor and acceptor impurities into the semiconductor, at elevated temperature in an oxidizing atmosphere, the surface of the silicon dioxide and forms an oxide layer 5, often one micron or more in thickness, congenitally united with and covering surface 2. This layer may consist chiefly of silicon dioxide, or of disproportionated silicon suboxide, depending upon the temperature and conditions of formation. In any event, the oxide surface layer is durable and firmly adherent to the semiconductor body, and furthermore it is a good electrical insulator.

According to common prior practice in manufacturing diffused-junction transistors, the semiconductor body was deoxidized by chemical etching prior to deposition of metal contacts onto the semiconductor surface. According to the present invention, only selected portions of the oxide layer are removed, as illustrated in Figs. 1 and 2, for example, while other portions of the oxide layer are left in place to serve as insulation for electrical leads used in making connections to and between the several semiconductor regions.

In particular, portions of the remaining oxide film extend across the edges of the P-N junctions at the surface of the semiconductor body, to facilitate the making of electrical connections from one side of a junction to another without shorting the junction. Thus, as illustrated in Figs. 1 and 2, the remaining oxide film comprises a tongue 5' that crosses the edge of junction 4, and another tongue 5'' that crosses the edges of both junctions 3 and 4. On the other hand, at least a portion of the surface over each of the emitter and base layers must be cleared to permit the formation of base and emitter contacts.

A convenient and highly accurate way to remove only selected portions of the oxide film is to use photoengraving techniques. The photoengraving resist is placed over the oxide-coated surface, and this is then exposed through a master photographic plate having opaque areas corresponding to the areas from which the oxide is to be removed. In the usual photographic developing, the unexposed resist is removed; and chemical etching can then be employed to remove the oxide layer from the unexposed areas, while the exposed and developed resist serves as a mask to prevent chemical etching of the oxide areas that are to be left on the semiconductor surface.

A discoid, metal, emitter contact 6 is adherent to surface 2, wholly within the edge of junction 3, centered upon and in electrical connection with the emitter region of the transistor. Electrical connections to this emitter contact are made through a metal strip 7 extending over and adherent to oxide layer 5. The strip 7 extends over the tongue 5' of the insulating oxide layer across the junctions 3 and 4, and thus provides an electrical connection extending from one side of the

Evolution of the integrated circuit

Embedded Systems

20th century

21st century

Integrations of small computers or systems on a chip for specialized/specific applications

Engineering problem

Cope with limited resources:
limited processing power, limited energy sources, small memories, etc.

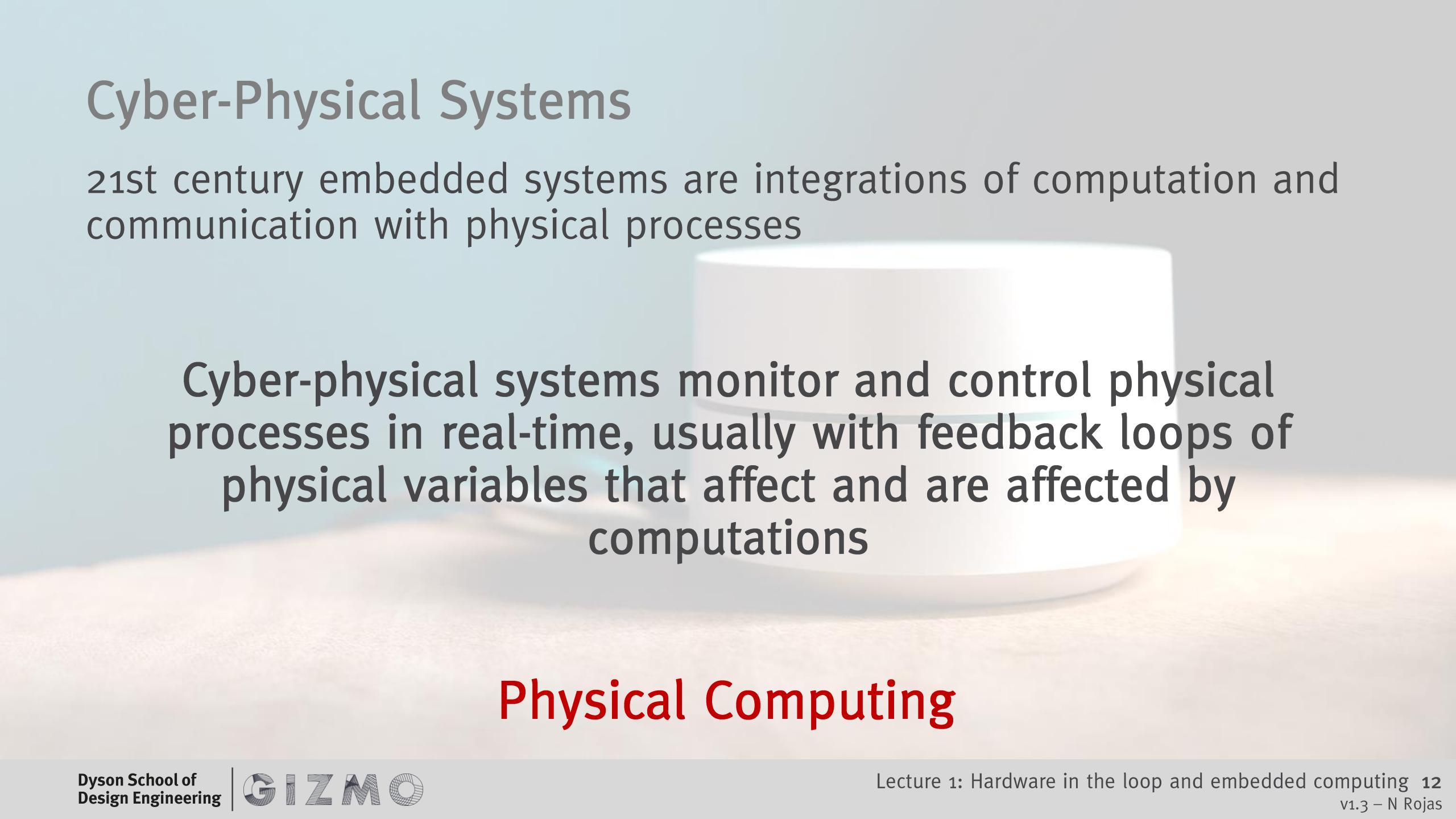
Engineering problem

Principal challenges stem from their *interaction with physical processes*, and not from their limited resources

Cyber-physical systems

Cyber-Physical Systems

21st century embedded systems are integrations of computation and communication with physical processes

A white cylindrical object, possibly a sensor or actuator, rests on a light-colored, textured surface. The background is a soft-focus landscape of hills under a clear sky.

Cyber-physical systems monitor and control physical processes in real-time, usually with feedback loops of physical variables that affect and are affected by computations

Physical Computing

Cyber-Physical Systems

- Internet of Things (IoT)
- Industrial Internet (IIoT)
- Systems of Systems
- Internet of Everything (IoE)
- Industry 4.0
- Smart <Everything>
- Machine-to-Machine (M2M)
- TSensors (trillion sensors)
- The Fog

All of these reflect a vision of a technology that deeply connects our *physical world* with our *information world*

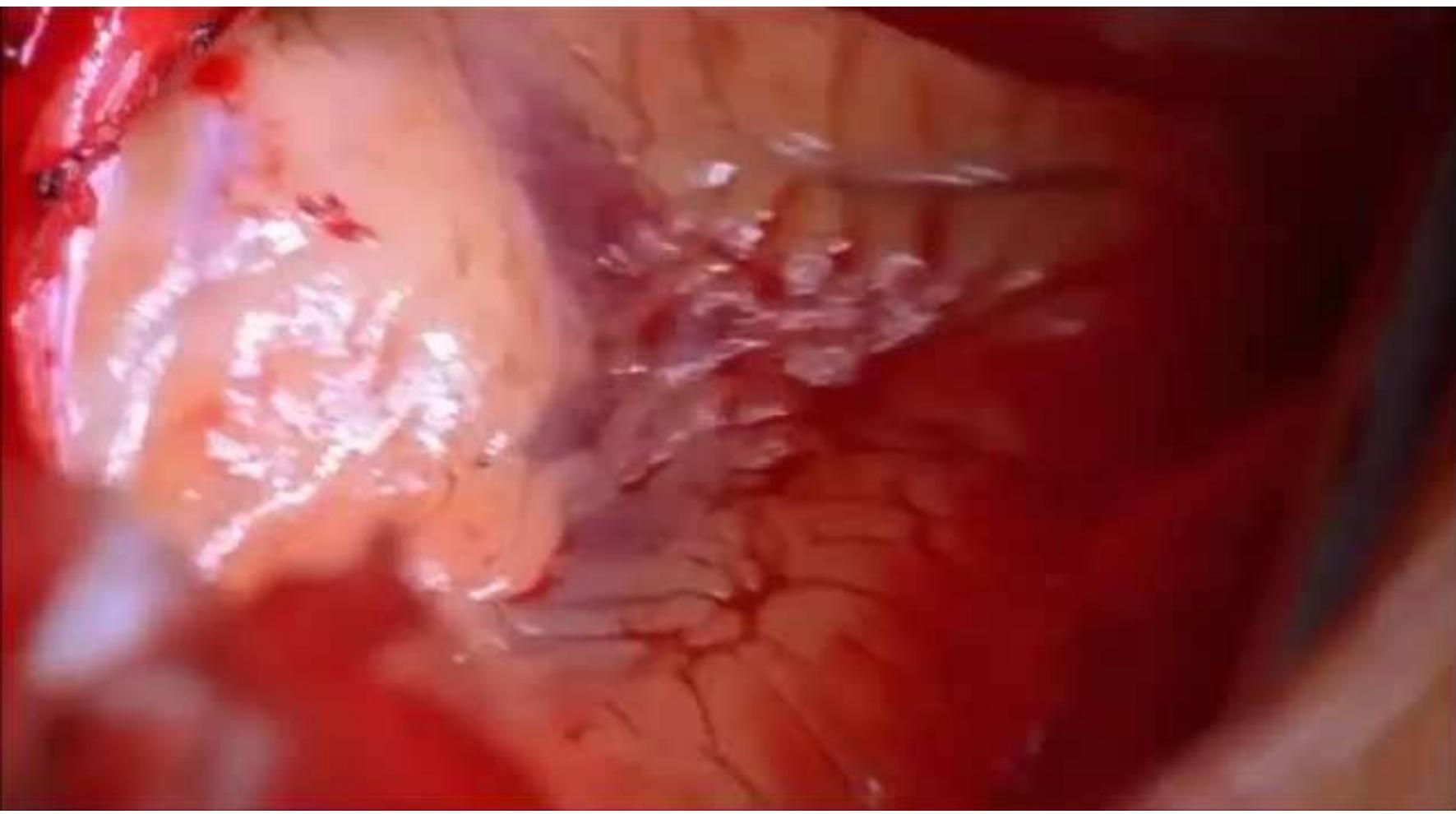
Cyber-Physical Systems

Potential to eclipse the 20th century information technology (IT) revolution. They are transforming the way people interact with engineered systems

Applications

Some key areas:

- Energy
- Health
- Manufacturing
- Telecommunication
- Transport
- Security



[Heart surgery](#)

Cyber-Physical Systems

Example challenge: *Operating Inside a Beating Heart*

Stopping the heart increases the risk of brain damage. A number of research teams have been working on an alternative where a surgeon can operate on a beating heart rather than stopping the heart

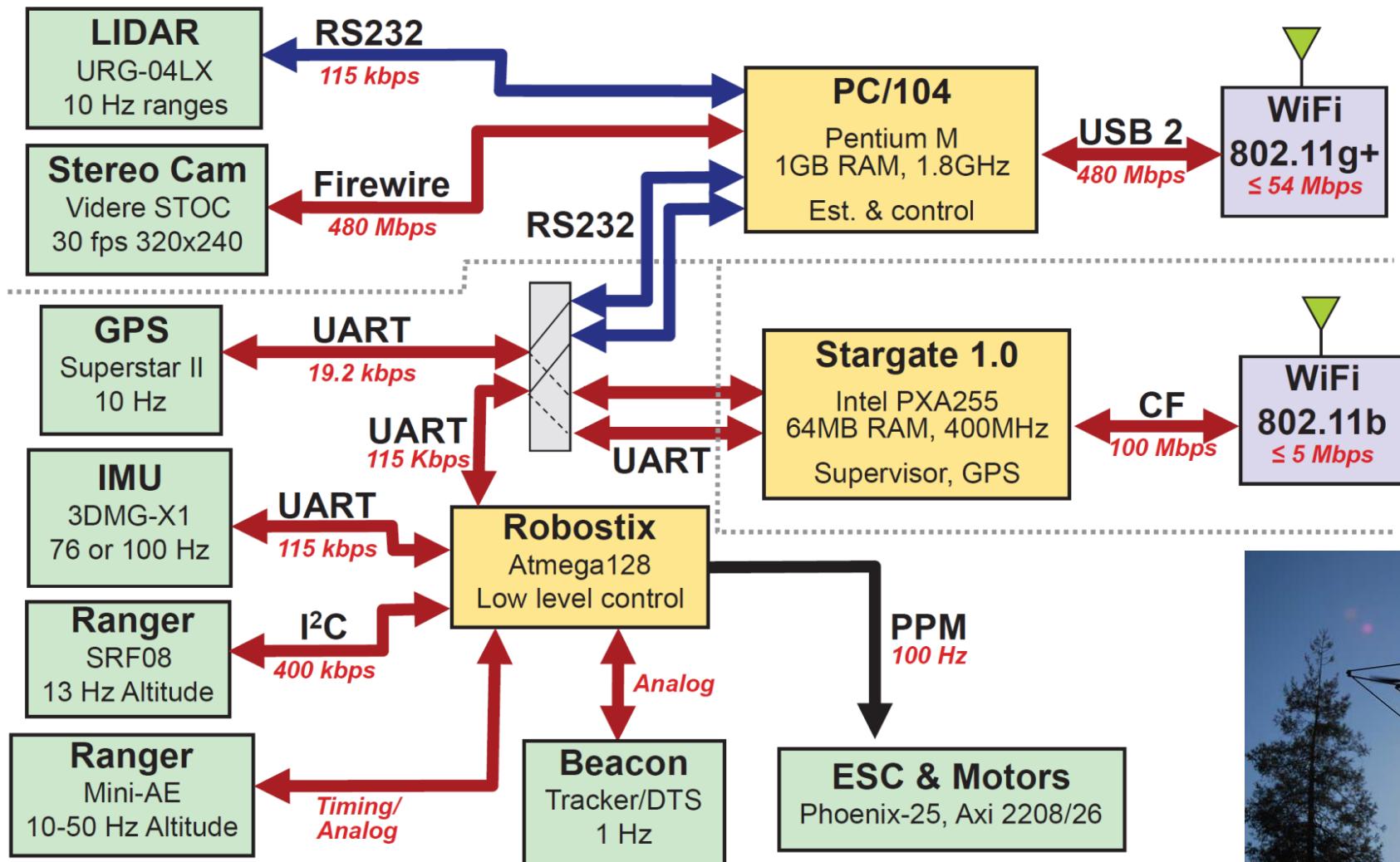
Any ideas to make this possible?

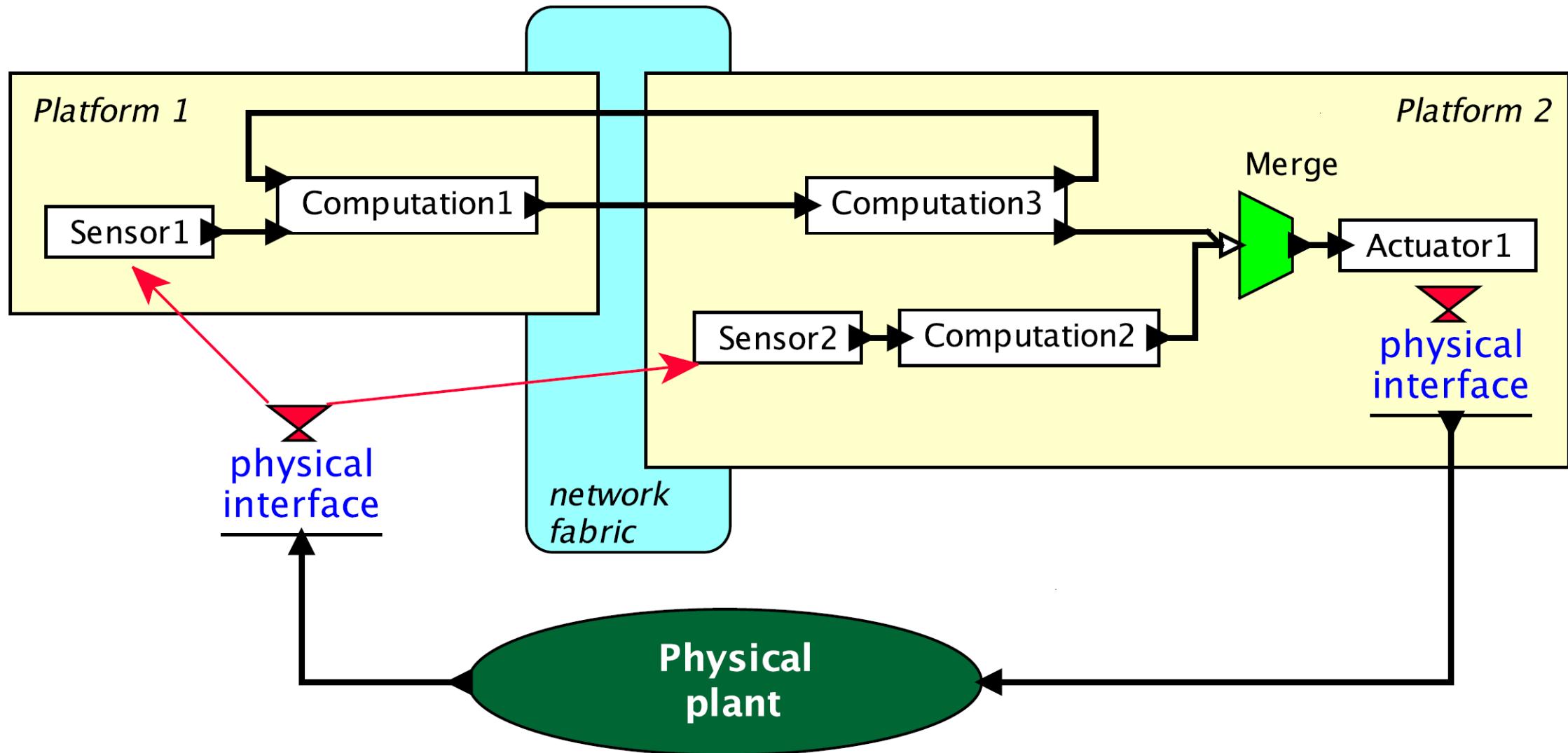
Structure of a Cyber-Physical System



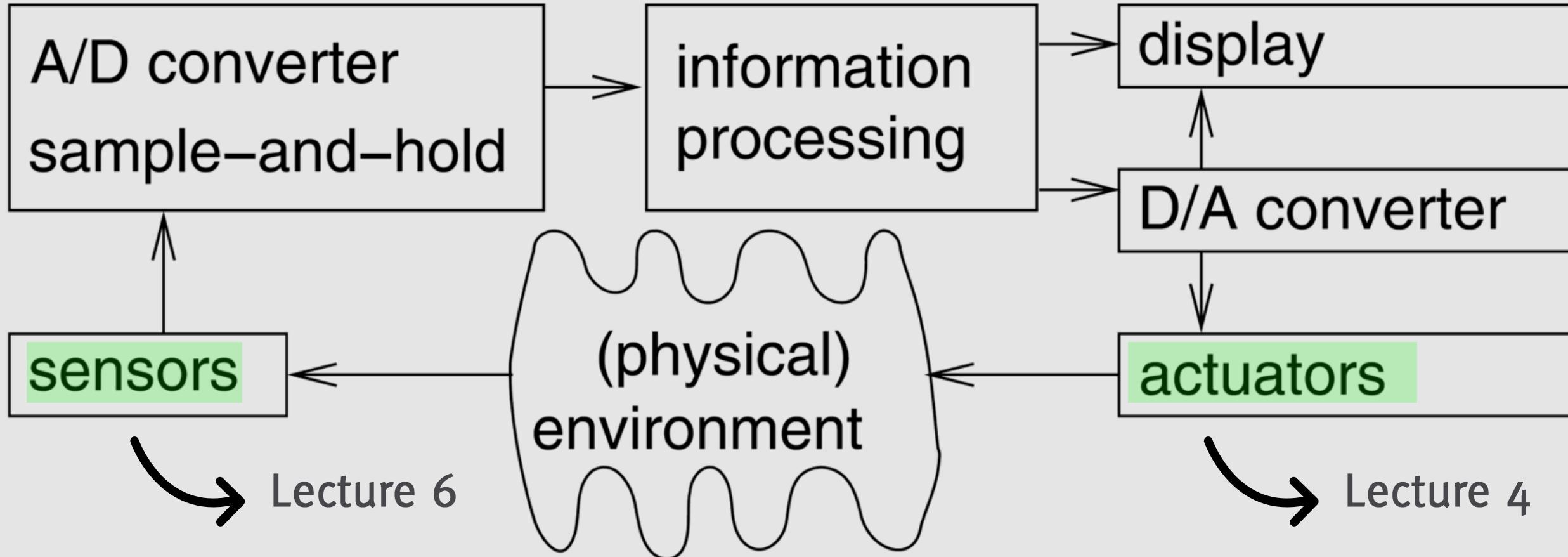
[Autonomous backflips
\(STARMAC, 2008\)](#)

Structure of a Cyber-Physical System





Structure of a Cyber-Physical System (Hardware in the Loop)



Hardware in the Loop (Simplified Structure)

Embedded Processors (Information Processing)

From very small, slow, inexpensive, low-power devices, to high-performance, special-purpose devices

- (Single-board) microcontrollers
- Programmable Logic Controllers (PLCs)
- Digital Signal Processors (DSPs)
- Graphics Processing Units (GPUs)
- Single-board computers

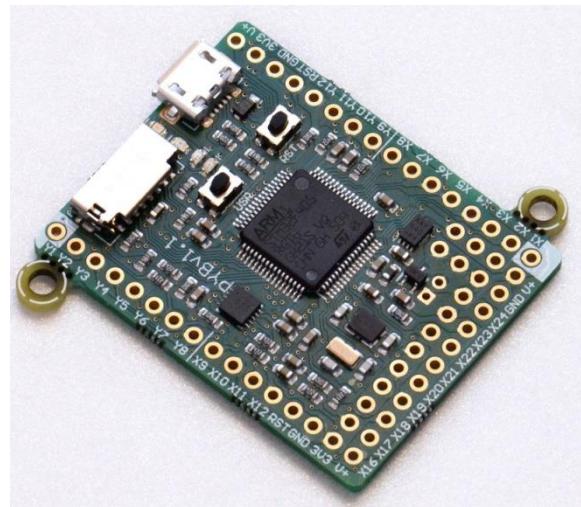


Arduino Mega 2560

Single-board microcontroller

Microcontroller: *Atmel ATmega2560*

Language: *C/C++*



Pyboard v1.1

Single-board microcontroller

Microcontroller: *STM32F405RG (ARM Cortex-M4)*

Language: *MicroPython (Python 3)*



Raspberry Pi 3

Single-board computer (needs OS)

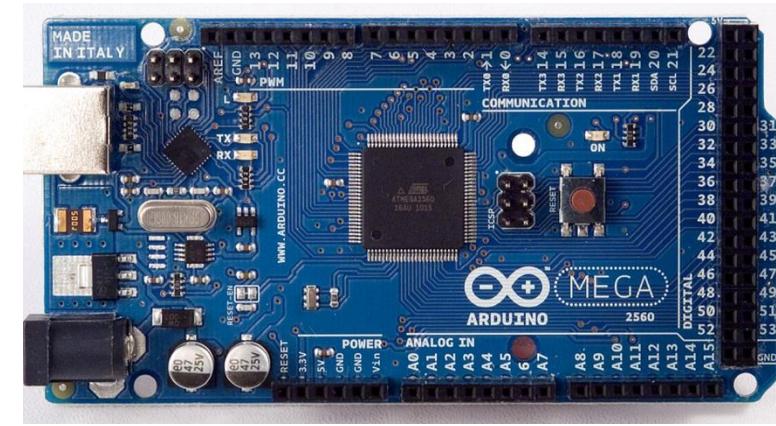
CPU: *4×ARM Cortex-A53*

Language: *Python, C/C++, Java, etc.*

What is the difference?

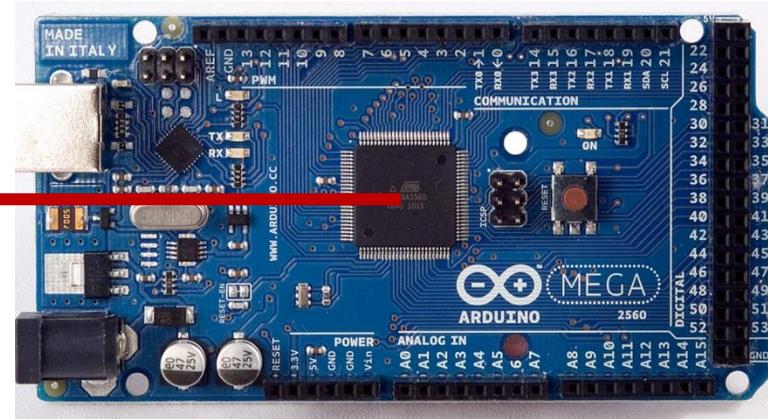
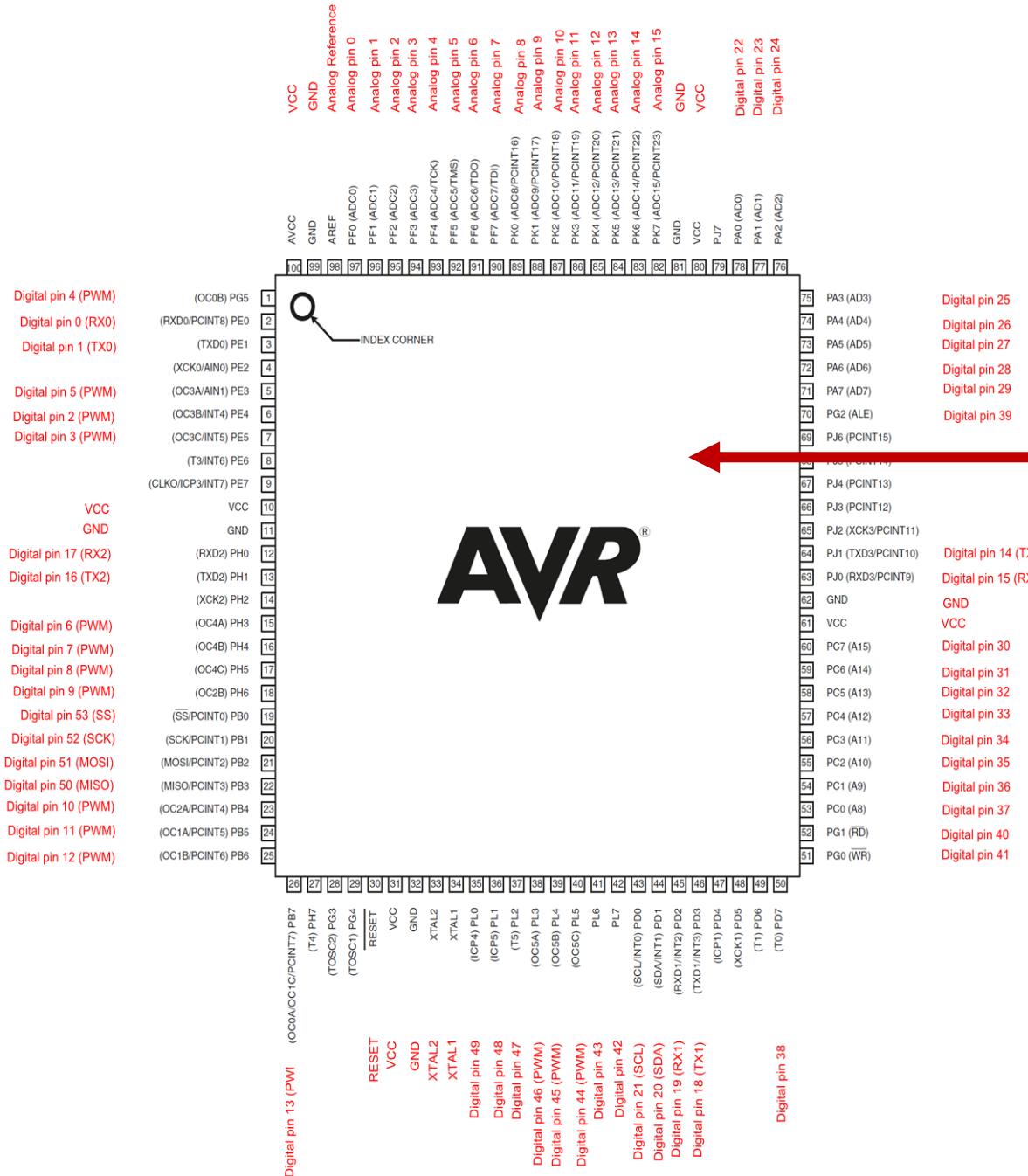
Microcontroller	ATmega2560
Operating Voltage	5V
Input Voltage (recommended)	7-12V
Input Voltage (limit)	6-20V
Digital I/O Pins	54 (of which 15 provide PWM output)
Analog Input Pins	16
DC Current per I/O Pin	20 mA
DC Current for 3.3V Pin	50 mA
Flash Memory	256 KB of which 8 KB used by bootloader
SRAM	8 KB
EEPROM	4 KB
Clock Speed	16 MHz
LED_BUILTIN	13
Length	101.52 mm
Width	53.3 mm
Weight	37 g

Arduino Mega 2560



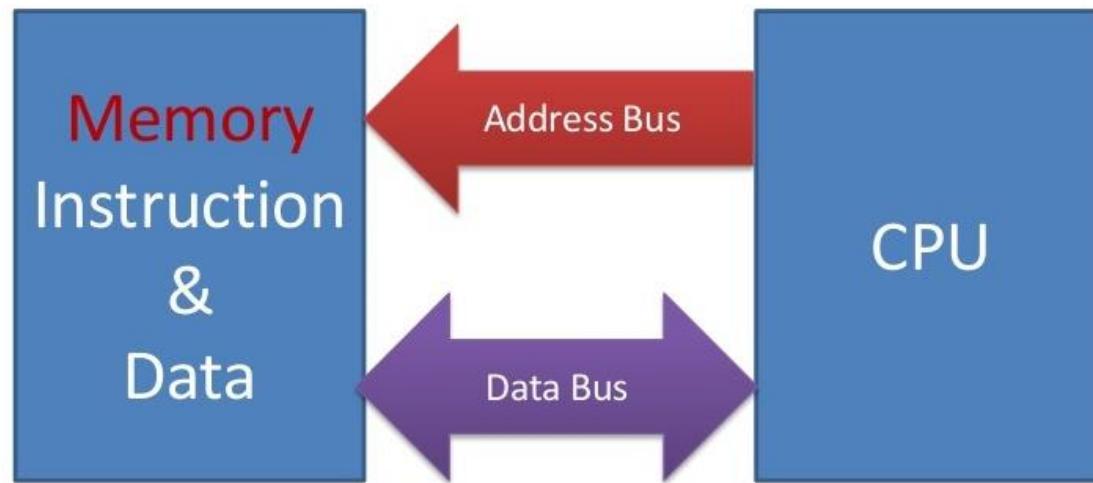
Arduino Mega 2560
Single-board microcontroller
 Microcontroller: *Atmel ATmega2560*
 Language: *C/C++*

ATMega 2560



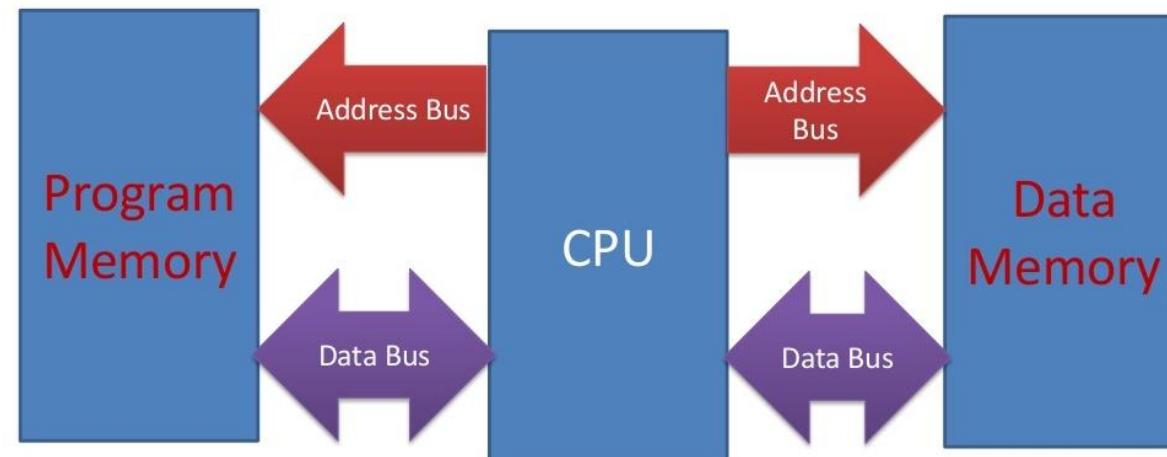
Arduino Mega 2560
Single-board microcontroller
 Microcontroller: *Atmel ATMega2560*
 Language: *C/C++*

Embedded Processor Architectures and Memory



Von Neumann
architecture

Harvard
architecture



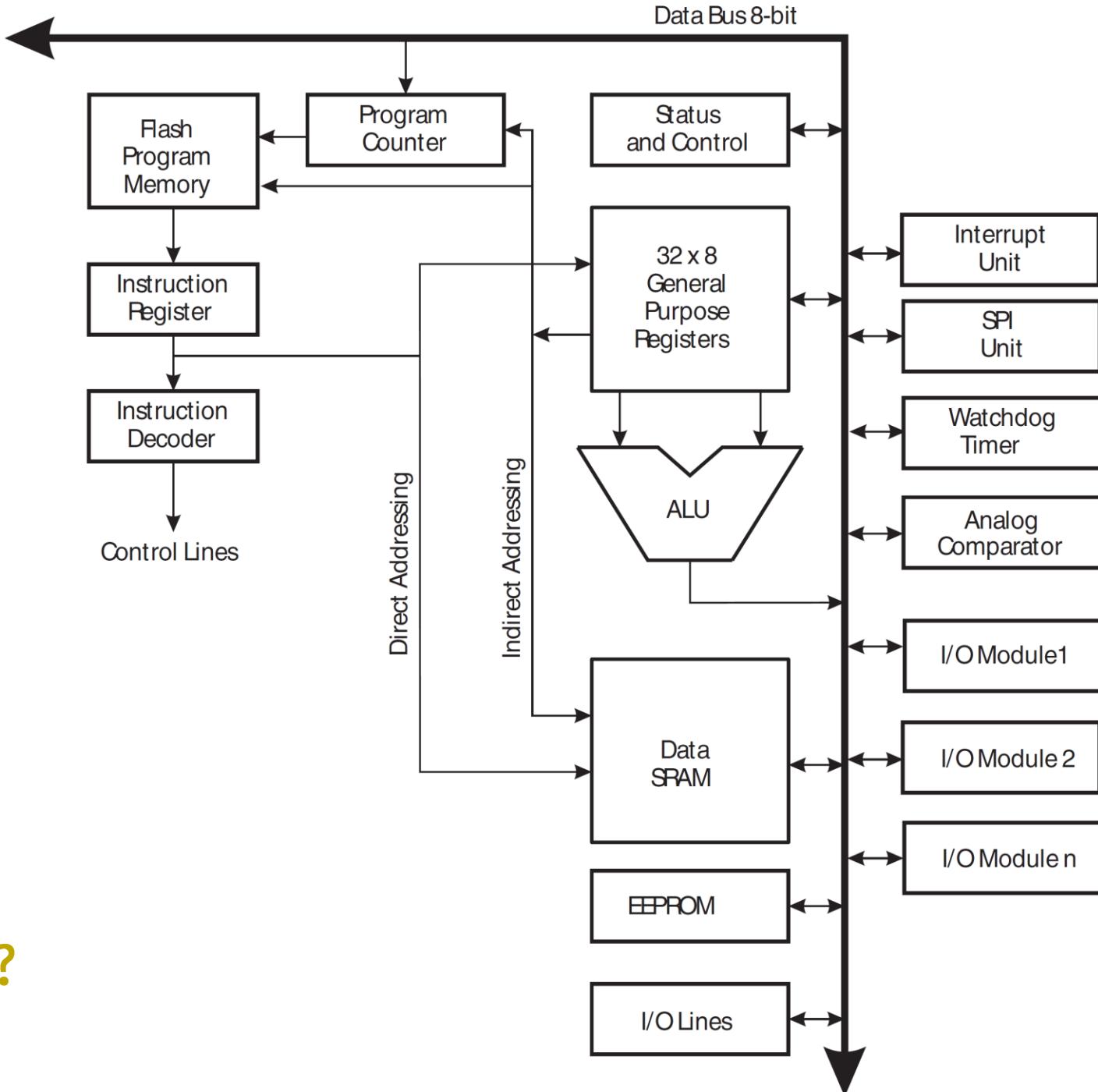
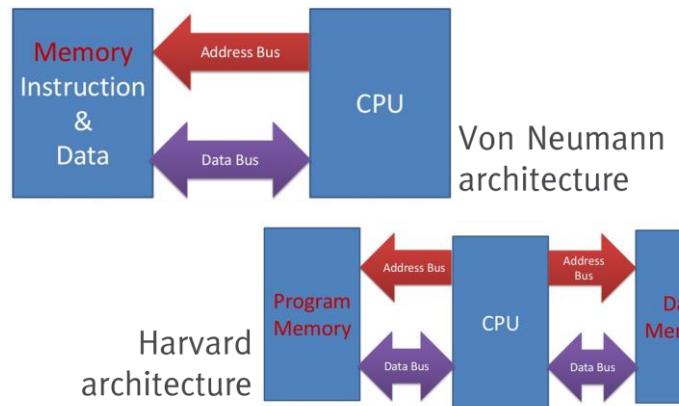
Role of Memory

Traditional roles: *storage and communication for programs*

Additionally, in cyber-physical systems:

Communication with sensors and actuators

ATMega 2560



Von Neumann or Harvard?

Non-Volatile Memory

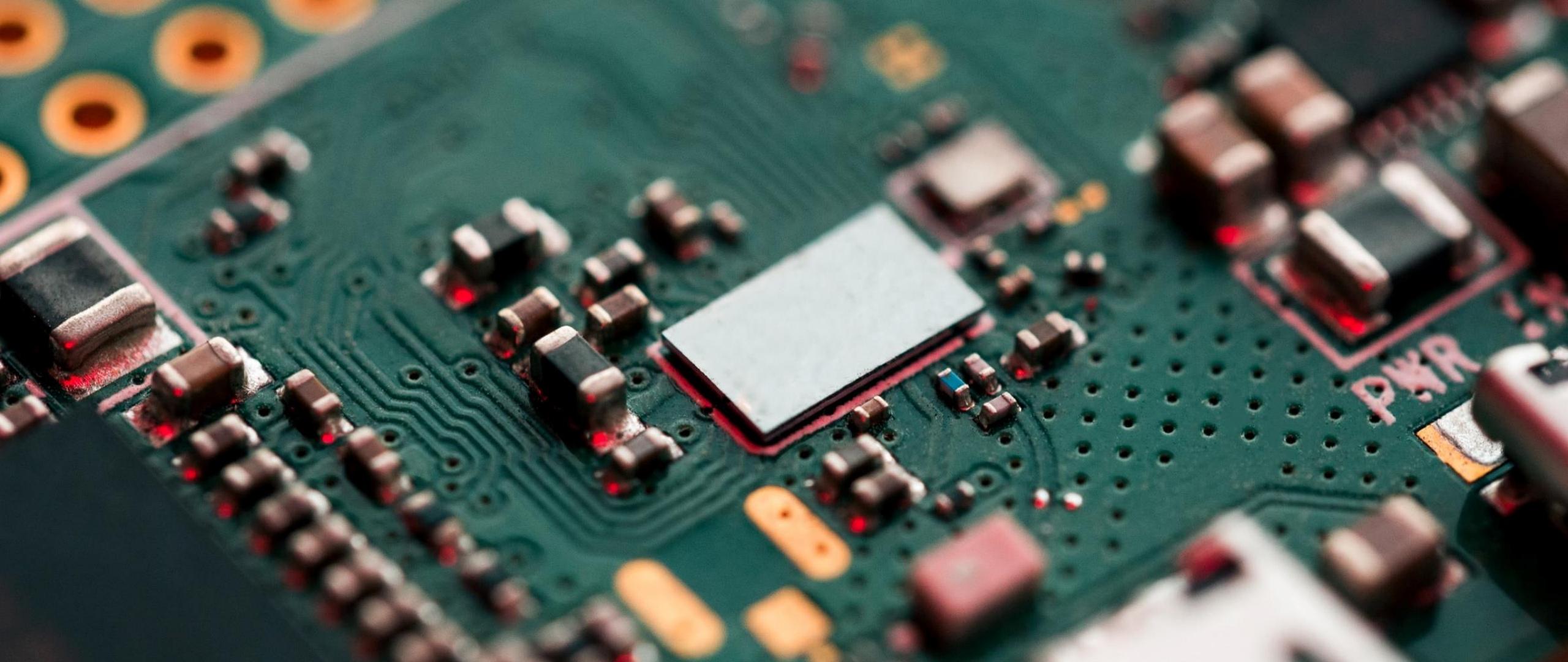
Preserves contents when power is off

- EPROM: Erasable Programmable Read-Only Memory (1971)
 - Erase by exposing the chip to strong UV light
- EEPROM: Electrically Erasable Programmable Read-Only Memory (1978)
- Flash memory (~1980)
 - Erase a “block” at a time. Limited number of program/erase cycles (~ 100,000)
- Disk drives

Volatile Memory

Loses contents when power is off

- **SRAM:** Static Random-Access Memory
 - Fast, deterministic access time. But more expensive and less dense than DRAM (6 times less capacity per number of transistors).
- **DRAM:** Dynamic Random-Access Memory
 - Slower than SRAM. Access time depends on the sequence of addresses.
 - Typically used for main memory.
- Boot loader
 - On power up, transfers data from non-volatile to volatile memory.



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