hroac2HW6

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Chapter 11 - [redacted]

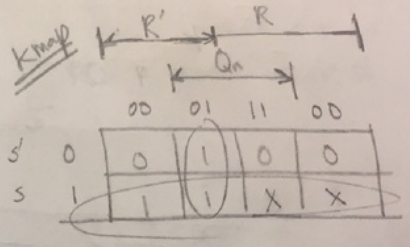
Problem #1 Draw the design Table, k-maps and circuit for

A. SR F.F. From D FF
B. T F.F. From JK F.F.

A Design Table

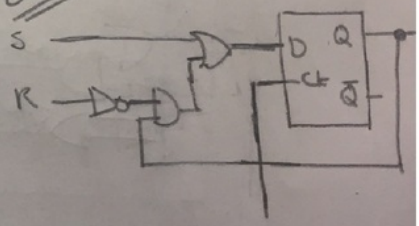
J	k	Qn	Qn+1	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	X	X	X
1	1	X	X	X

Kmap



$D = S + R'Q_n$

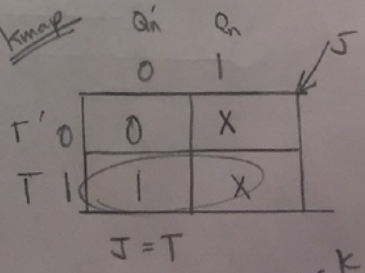
Circuit



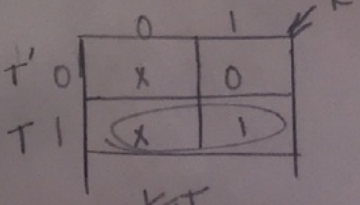
B

J	k	Qn	Qn+1	T
X	0	0	0	0
0	X	1	1	0
X	1	1	0	1
1	X	0	1	1

Kmap

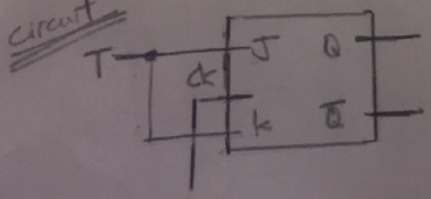


J = T



K = T

Circuit



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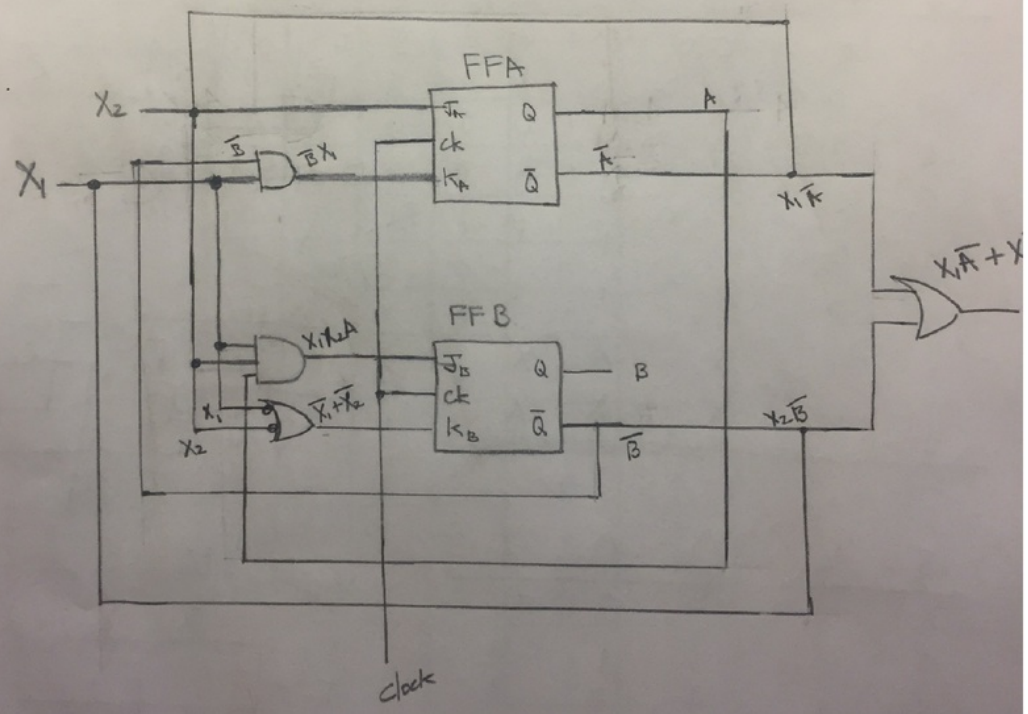
Problem 2. Draw the Logic Diagram, Analysis table, state trans. diag. Sequential circuit. 2 JK Flip Flops. (FFA, FFB). 2 inputs X_1 and X_2

$J_A = X_2$
$K_A = X_1 \overline{B}$
$J_B = X_1 X_2 A$
$K_B = \overline{X_1} + \overline{X_2}$
← input

$Z = X_1 \overline{A} + X_2 \overline{B}$ ← output.



Problem #2 cont

Analysis table.

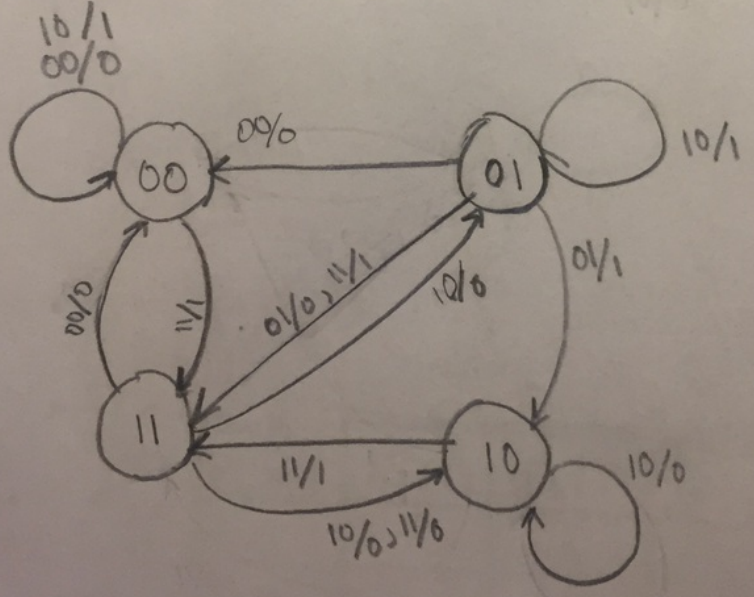
AB = {00, 01, 10, 11}.

A(t)	B(t)	$X_1(t)$	$X_2(t)$	$J_A(t)$	$J_B(t)$	A(t+1)	B(t+1)	z(t)
0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	1	0	1
0	0	1	0	0	0	0	0	1
0	0	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0
0	1	0	1	1	0	1	1	0
0	1	1	0	0	0	0	1	1
0	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	1
1	0	1	0	0	0	1	0	0
1	0	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0
1	1	0	1	1	0	0	1	0
1	1	1	0	0	0	0	1	0
1	1	1	1	1	1	0	1	0

Problem #2

state transition diagram

A(t) B(t)	X1(t) X(t) = 00	01	10	11
00	00/0	10/1	00/1	11/1
01	00/0	11/0	01/1	11/1
10	00/0	00/1	10/0	11/1
11	00/0	01/0	01/0	01/0

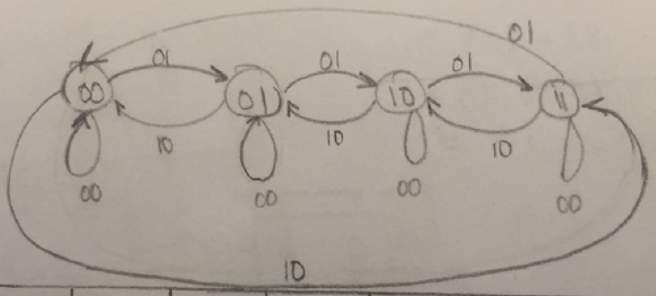


Problem #3 Textbook pg 593 #16 (d) Truth Table, Kmap Circuit

Figure 11.55 is a state transition diagram for seq circuits w/ 2 FFs and 2 inputs.

A(t) B(t)	$X_1(t)$ $X_2(t)$ = 00	01	10	11
00	00	01	11	X
01	01	10	00	X
10	10	11	01	X
11	X	00	10	X

A(t+1) B(t+1), Y(t).



A(t)	B(t)	$X_1(t)$	$X_2(t)$	$T_A(t)$	$T_B(t)$	A(t+1)	B(t+1)	
0	0	0	0	0	0	0	0	
0	0	0	1	0	1	0	1	
0	0	1	0	1	0	1	1	
0	0	1	1	1	1	X	X	
0	1	0	0	0	1	0	1	
0	1	0	1	0	0	1	0	
0	1	1	0	1	1	0	0	
0	1	1	1	1	0	X	X	
1	0	0	0	1	0	1	0	
1	0	0	1	1	1	1	1	
1	0	1	0	0	0	0	1	
1	0	1	1	0	1	X	X	
1	1	0	0	1	1	X	X	
1	1	0	1	1	0	0	0	
1	1	1	0	0	1	1	0	
1	1	1	1	0	0	X	X	

Problem #3 Kmap + Circuit

T_A

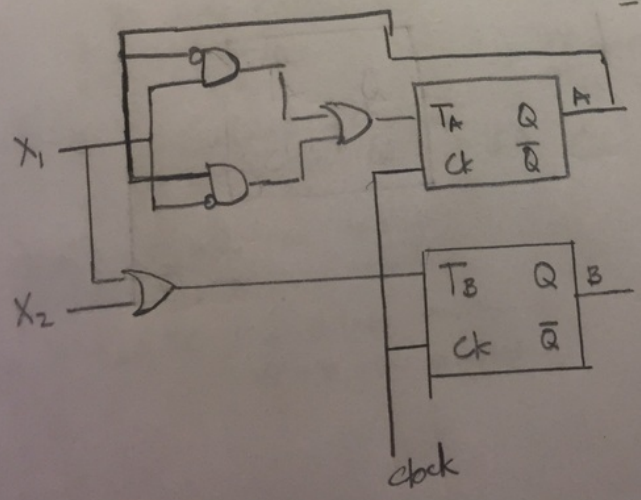
AB \ X_1X_2	00	01	10	11
00	0	0	1	1
01	0	0	1	1
10	1	1	0	0
11	1	1	0	0

$T_A = \bar{A}X_1 + A\bar{X}_1$

T_B

AB \ X_1X_2	00	01	10	11
00	0	1	0	1
01	1	0	1	0
10	0	1	0	1
11	1	0	1	0

$T_B = \bar{A}B\bar{X}_1 + AB\bar{X}_1 + \bar{A}\bar{B}X_1 + A\bar{B}\bar{X}_1 + \bar{A}BX$
$+ ABX_2 + \bar{A}\bar{B}X_2 + A\bar{B}X_2$
$= [B\bar{X}_1(\bar{A}+A) + \bar{B}\bar{X}_1(\bar{A}+A)$
$+ BX_2(\bar{A}+A) + \bar{B}X_2(A+A)]$
$= (B\bar{X}_1 + \bar{B}\bar{X}_1 + BX_2 + \bar{B}X_2)(\bar{A}$
$= (X_1(B+\bar{B}) + X_2(B+\bar{B}))(\bar{A}$
$= (X_1 + X_2)(B+\bar{B})(\bar{A}+A)$



Problem #4 A sequential circuit has 3 state registers and 3 inputs.

a.) How many states does it have

$n = 3$ = state registers

$2^3 = 8$

b.) How many transitions from each state does it have?

8 transitions

m = inputs = 3

$2^3 = 8$

c.) How many total transitions

$2^m 2^n = (8)(8) = 64$

Problem #5 594, #21a.

- 10-bit address
- 64 byte PROM
- 32 byte RAM
- 4-port I/O

connect w/ two add lines.

a.) Draw Full address decoding

b.) Include table similar to 11.47

c.) Memory Map - show how each ch is enabled.

d.) Can you add additional chips

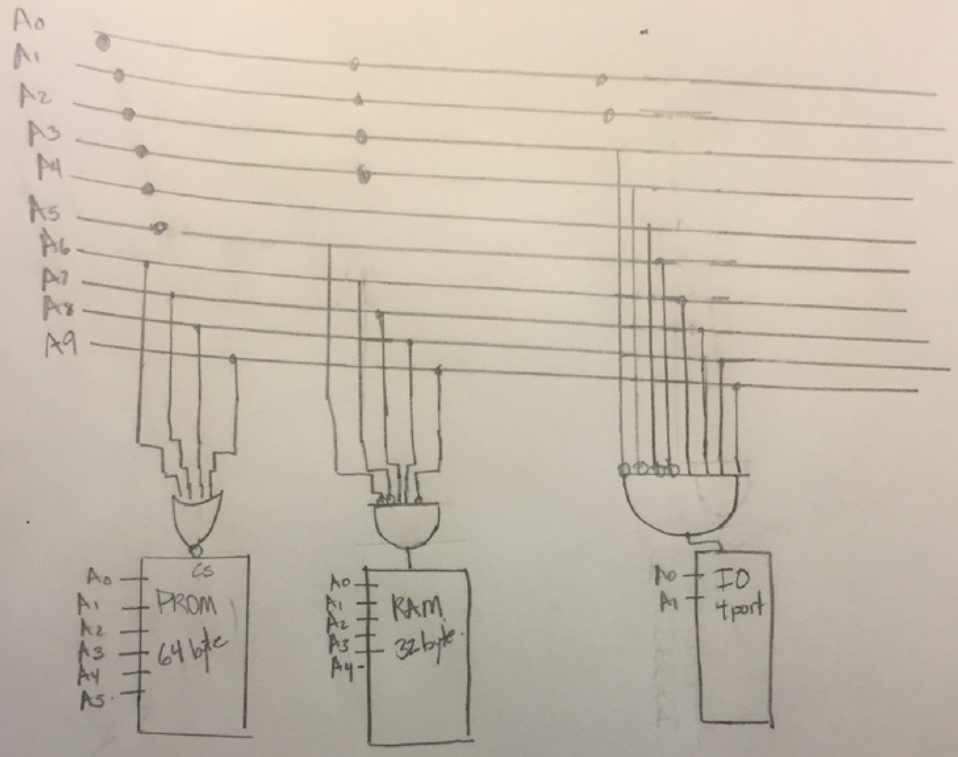
PROM 6 add lines → chip
4 → chip selected.

RAM 5 add lines → chip
5 → chip selected.

4-Port IO 2 add lines → chip
4 → chip selected.

cont.

a.) Draw full address decoding

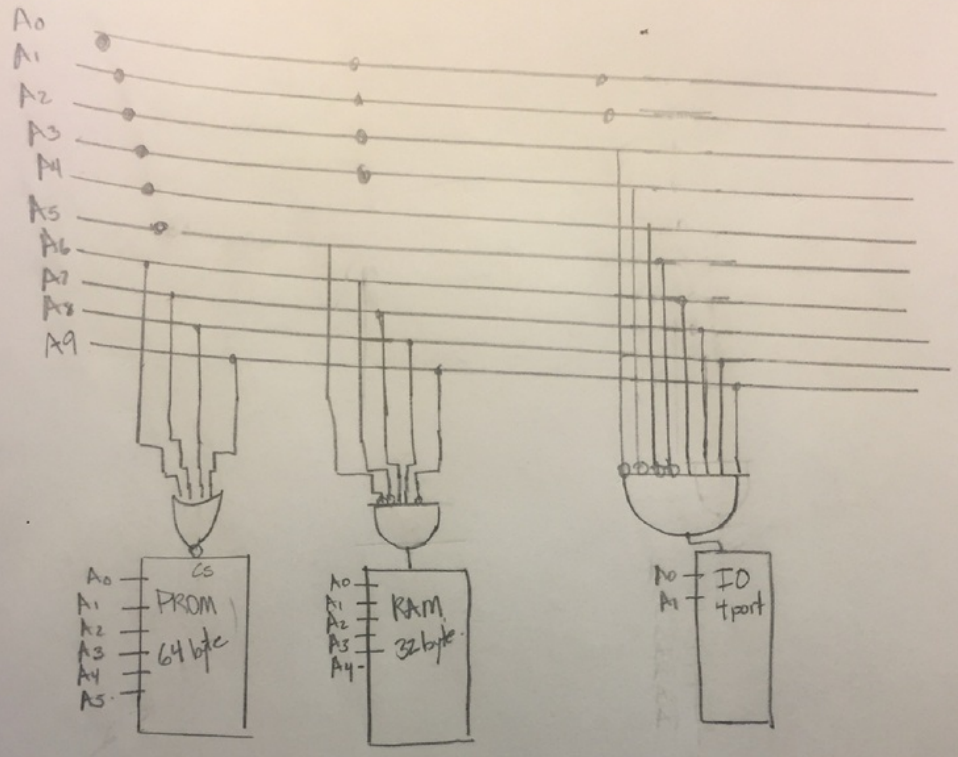


b.) Include a table similar to 11.47.

Device			
PROM 64byte	00 0000 0000	00 0011 1111	00 00XX XXXX
RAM	01 1000 0000	01 1001 1111	01 10XX XXXX
I/O	11 0000 0000	11 1100 0011	11 1100 00XX

d.) Yes because there is available memory space.

a.) Draw full address decoding



b.) Include a table similar to 11.47.

Device			
PROM 64byte	00 0000 0000	00 0011 1111	00 00XX XXXX
RAM	01 1000 0000	01 1001 1111	01 10XX XXXX
I/O	11 0000 0000	11 1100 0011	11 1100 00XX

d.) Yes because there is available memory space.

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GRADEMARK REPORT

FINAL GRADE

49/50

GENERAL COMMENTS

Instructor

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Comment 1

Don't cares

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1A DT &KMAP 3 / 3

FULL CREDIT
(3)

MINUS 1
(2)

MINUS 2
(1)

MINUS 3
(0)

NO CREDIT
(0)

1A CIRCUIT 2 / 2

FULL CREDIT
(2)

MINUS 1
(1)

MINUS 2
(0)

MINUS 3
(0)

NO CREDIT
(0)

1B DT KMAP 3 / 3

FULL CREDIT
(3)

MINUS 1
(2)

MINUS 2
(1)

MINUS 3
(0)

NO CREDIT
(0)

1B CIRCUIT 2 / 2

FULL CREDIT
(2)

MINUS 1
(1)

MINUS 2
(0)

MINUS 3
(0)

NO CREDIT
(0)

2 LOGIC DIA 3 / 3

FULL CREDIT
(3)

MINUS 1
(2)

MINUS 2
(1)

MINUS 3
(0)

NO CREDIT
(0)

2 DESIGN TAB 3 / 3

FULL CREDIT
(3)

MINUS 1
(2)

MINUS 2
(1)

MINUS 3
(0)

NO CREDIT
(0)

2 STATE X DIA 4 / 4

FULL CREDIT
(4)

MINUS 1
(3)

MINUS 2
(2)

MINUS 3
(1)

NO CREDIT
(0)

3 DESIGN TAB 3 / 3

FULL CREDIT
(3)

MINUS 1
(2)

MINUS 2
(1)

MINUS 3
(0)

NO CREDIT
(0)

3 KMAP & TRMS 3 / 4

FULL CREDIT
(4)

MINUS 1
(3)

MINUS 2
(2)

MINUS 3
(1)

NO CREDIT
(0)

3 CIRCUIT 3 / 3

FULL CREDIT
(3)

MINUS 1
(2)

MINUS 2
(1)

MINUS 3
(0)

NO CREDIT
(0)

4A STATES 3 / 3

FULL CREDIT
(3)

MINUS 1
(2)

MINUS 2
(1)

MINUS 3
(0)

NO CREDIT
(0)

4B XS / STATE 3 / 3

FULL CREDIT
(3)

MINUS 1
(2)

MINUS 2
(1)

MINUS 3
(0)

NO CREDIT
(0)

4C TOTAL XS 4 / 4

FULL CREDIT
(4)

MINUS 1
(3)

MINUS 2
(2)

MINUS 3
(1)

NO CREDIT
(0)

5A BUS- CHIP 2 / 2

FULL CREDIT
(2)

MINUS 1
(1)

MINUS 2
(0)

MINUS 3
(1)

NO CREDIT
(0)

5A ANDS 2 / 2

FULL CREDIT
(2)

MINUS 1
(1)

MINUS 2
(0)

MINUS 3
(0)

NO CREDIT
(0)

5B ADDRESS 2 / 2

FULL CREDIT
(2)

MINUS 1
(1)

MINUS 2
(0)

MINUS 3
(0)

NO CREDIT
(0)

5C MEMORY MAP 2 / 2

FULL CREDIT
(2)

MINUS 1
(1)

MINUS 2
(0)

MINUS 3
(0)

NO CREDIT
(0)

5D ADD CHIPS? 2 / 2

FULL CREDIT
(2)

MINUS 1
(1)

MINUS 2
(0)

MINUS 3
(0)

NO CREDIT
(0)