Surround Gate Transistor With Epitaxially Grown Si Pillar and Simulation Study on Soft Error and Rowhammer Tolerance for DRAM

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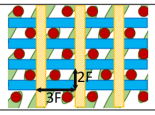
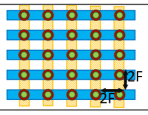
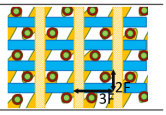
***Abstract*— A new dynamic random access memory (DRAM) memory cell transistor is fabricated, and its soft-error immunity and rowhammer tolerance are studied. The vertical channel is formed by selective epitaxial growth of silicon pillar, and the surround gate forms a fully depleted (FD) channel, which can suppress floating-body effects, such as hysteresis. A TCAD simulation study compares this device and conventional bulk saddle FinFET in terms of soft error immunity and rowhammer tolerance. The confined channel limits soft error because of its thin channel volume for charge generation due to alpha and neutron particles. The surround gate device is inherently free from rowhammer attack as each silicon body of any memory cell transistor is fully isolated from neighboring word lines.**

***Index Terms*— Epitaxial growth, rowhammer, soft-error, surround gate transistor (SGT), TCAD simulation.**

TABLE I
COMPARISON OF SADDLE FINFET AND CONVENTIONAL AND PROPOSED SGT

	Saddle FinFET	Previous SGT	SGT in this work
Layout WL, BL, SN Silicon body n^+ bridge			
Unit Cell Size	6F2	4F2	6F2
Channel formation	Etched silicon	Etched silicon	Epitaxial silicon
BL material	Metal	Buried n^+	Metal
Body isolation	Tied	Isolated	Isolated
Sensitive volume	Large	Small	Small

I. INTRODUCTION

As dynamic random access memory (DRAM) technology scales beyond 1z-nm node, difficulties in fabricating cell transistor and capacitor impede further downscaling. There are two reliability issues attributed to device miniaturization in the current saddle FinFET as a cell transistor. A soft error is an accidental bit-flip error due to radioactive alpha contamination of package material and cosmic rays, such as neutron. The control of soft error is getting difficult because voltage scaling and capacitance reduction are inevitable for low-power operation [1]. A rowhammer is an accidental bit-flip error due to repeated activation of neighboring cells. The control of rowhammer is challenging because the cells are tightly packed [2]. In this article, a cell transistor structure combining gate-all-around and vertical silicon pillar is examined in terms of soft-error immunity and rowhammer tolerance.

As an alternative to the current saddle FinFET, a vertical pillar transistor (VPT) consisting of a surround gate has been proposed to achieve both longer physical gate length and higher cell density at a given footprint [3]–[5]. However, there are two issues: floating-body effect and high bitline (BL) resistance along 512 or 1024 rows. The conventional VPTs [3]–[5] use high-energy and high-dose ion implantation (IIP) to form a buried n^+ region for BL. The high resistance of n^+ diffusion BL can limit the timing parameters and the maximum size of a subarray [6]. The high-energy and high-dose IIP often cause generation and recombination trap centers [7], degrading memory performance [8]. In addition, the deep n^+ IIP inevitably requires higher p-type body doping of at least $\sim 10^{17}/cm^3$ to compensate for the tail of the n^+ profile, as shown by the secondary ion mass spectroscopy (SIMS) profile in [9]. The high body doping reduces depletion width, forming a partially depleted (PD) body, and the resulting history effect limits the core frequency [10].

Manuscript received September 28, 2020; revised December 4, 2020; accepted December 16, 2020. Date of publication January 6, 2021; date of current version January 22, 2021. This work was supported by the National Research Foundation of Korea (NRF) Grant Funded by the Korea Government (MSIT) under Grant 2020R1G1A1099554. The review of this article was arranged by Editor T.-H. Kim. *(Corresponding author: Jin-Woo Han.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2020.3045966.

Digital Object Identifier 10.1109/TED.2020.3045966

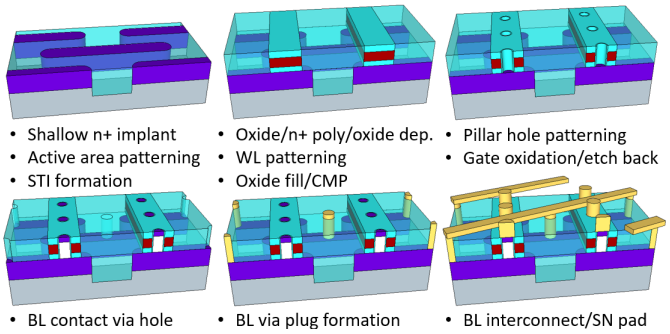

Fig. 1. Schematic illustration of the fabrication steps of the proposed SGT.

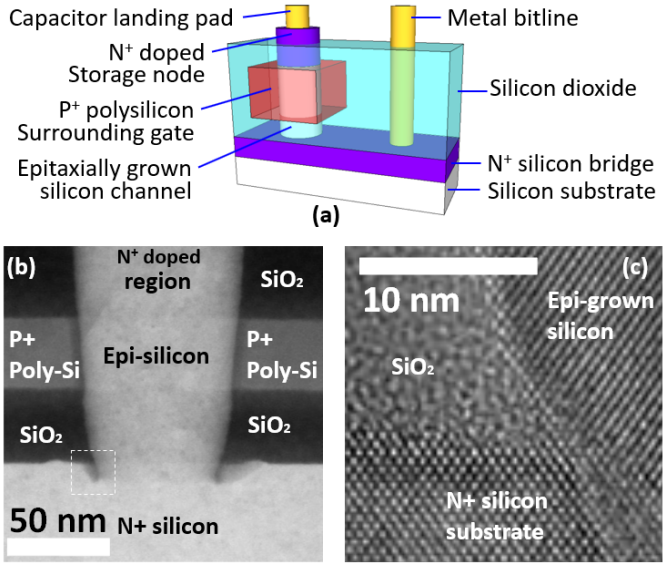

Fig. 2. (a) Schematic illustration of the final structure, (b) cross-sectional TEM image of the fabricated SGT, and (c) magnified view of the boxed region of (b).

The motivation of this article is twofold, as summarized in TableI. The first is to propose a potential fabrication method to suppress the body doping concentration and a novel layout to improve the BL resistance compared with the previous surround gate transistor (SGT). Whereas buried n^+ BL (often referred to as 4F2 cell) and etched channel are used in previous SGTs, a metal tungsten BL and epitaxially grown channel are proposed here (6F2 cell). The device fabricated here is the cell transistor before the cell capacitor integration. After the transfer and output characteristics are measured, the memory characteristics are estimated using TCAD by integrating the cell capacitor [11]. The second goal is to demonstrate for the first time the superiority of SGT in terms of rowhammer-free operation and higher soft error immunity compared with the bulk saddle FinFET. With the aid of TCAD, the rowhammer-free operation and the soft error immunity are attributed to the fully isolated body and the limited channel volume sensitive to ionizing particles, respectively.

II. Device Fabrication of SGT

The SGT fabrication process flow has been devised to take advantage of the significant foundation set by 3-D NAND in search of channel selective epitaxial growth (SEG). The simplified SGT flow lends itself to fast turnaround and extensive experimental split [12].

Fig. 1 shows an example of how the SGT would be integrated into a production flow. A high-dose and low-energy n^+ IIP is conducted to form the n^+ junction of the cell at the wafer surface. The shallow junction enables higher concentration and lower lattice damage than the high-dose and high-energy IIP of buried n^+ BL. The buried n^+ region serves as the conductive bridge between the metal BL and the junction of the cell transistor. Shallow trench isolation (STI) is patterned and filled with silicon dioxide (SiO_2) to isolate adjacent n^+ junctions. Then, the interlayer SiO_2, the *in situ* p^+ poly-Si (or a Si_3N_4 as a sacrificial layer for replacement metal gate) word line (WL) and the top SiO_2 film are subsequently deposited and patterned. A train of holes is patterned within the WL layer, and the thermal gate oxide is grown on the sidewall of the WL. After the oxide on the bottom surface is etched to expose the n^+ region, SEG forms a silicon pillar in the holes. Then, the n^+ IIP is carried out on the top region on the Si pillar. The top n^+ region serves as the storage node (SN) contact for the stack capacitor. Finally, metal contacts for the source (BL) and drain (SN) are formed. The common BL metal is connected to individual cell channels through a buried n^+ conductive bridge.

In this demonstration, p^+ poly-Si was used for threshold voltage (V_t) greater than 1 V. However, it will be shown later that p^+ poly-Si WL turned out to be an improper choice due to boron segregation and diffusion into the silicon pillar. This fact accidentally nullifies one benefit of using the undoped epitaxially grown channel. Thus, a high workfunction metal WL will be desirable in order to prevent the counter doping of the channel. Nevertheless, it is still valid that the epitaxially grown silicon pillar can offer an undoped channel in contrast to the etched silicon pillar if boron segregation were properly inhibited. Nonetheless, the focal points of this article, i.e., soft-error immunity and rowhammer tolerance, are not hampered by the boron segregation as its benefit is attributed to the sensitive channel volume and its full isolation. Finally, though the discussion covers memory array structure, the actual experimental portion is only the unit cell transistor here.

Fig. 2(a) labels the cell transistor. Fig. 2(b) shows the transmission electron microscopy (TEM) cross section image of the fabricated device. A similar SEG silicon channel formation process was demonstrated for NAND flash memory applications elsewhere [12]. Fig. 2(c) shows the magnified TEM view near the Si seed region. No signature of lattice misfits or dislocations is found. The diameter of the channel is 54 nm, the physical gate length is 50 nm, and the gate oxide thickness is 3 nm.

III. Measurement of Epitaxial Channel SGT

Fig. 3 shows the measured transfer and output characteristics. The OFF-state current ($V_{gs} = 0$ V and $V_{ds} = 1.2$ V) is below the noise floor of our measurement equipment. No gate

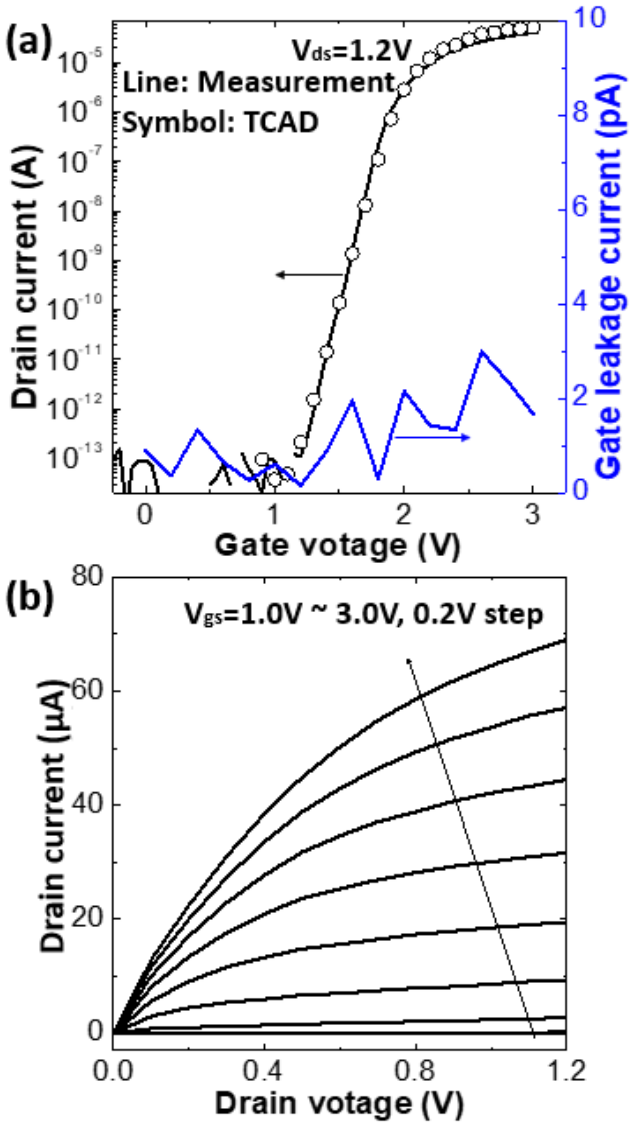

Fig. 3. (a) Measured transfer curve and gate leakage current and (b) output characteristics of the SGT. TCAD simulation was used to fit the subthreshold behavior. The results suggest boron segregation from the heavily doped p^+ gate and counter doping into the pillar to be the cause of high V_t.

induced drain leakage (GIDL) current is observed down to $V_{gs} = -1$ V at $V_{ds} = 1.2$ V. The gate leakage current was also measured and found to be of the order of pA. The ON-state current ($V_{gs} = 3$ V and $V_{ds} = 1.2$ V) is 60 μA. No kink is found in the saturation region of the output characteristics, providing indirect evidence of the mitigation of the floating-body effect. When the diameter of the channel becomes thinner than the depletion width, the device is referred to as the fully depleted transistor. The depletion width (W_{dep}) is proportional to $N_s^{-1/2}$, where N_s is the body doping concentration. This model implies that a lighter body doping is favored for the fully depleted (FD) transistor. In such a transistor, no neutral region is provided for the majority carriers to accumulate, i.e., *holes* in the p-type body, nullifying the history effect [13]. This fact was a key enabler of FD-silicon on insulator (SOI) technology for high-frequency and low-power logic applications [14], [15]. Likewise, the same mechanism can be a key requirement for DRAM cell transistors with a floating body. Therefore, it is established that the epitaxially grown silicon pillar has the potential to offer a fully depleted channel and high immunity against hysteresis. Nevertheless, it is possible that the experimental device may be a PD device due to its large diameter and boron counterdoping in the channel. However, an FD transistor has been known to offer greater soft-error immunity than a PD transistor. In other words, with the soft-error immunity of the PD-SGT against the bulk saddle FinFET demonstrated in this article, the same conclusion can be extended to the FD-SGT. Furthermore, with the rowhammering immunity originating from the surrounding gate nature, the same conclusion will hold to both PD and FD-SGT.

The fabricated device here showed an unusually high V_t. Various design parameters can affect V_t. Among various causes, physical dimensions, such as gate length, channel diameter, and gate oxide thickness, are obviously known from the TEM images. However, the parameters related to the doping are not straightforward. The doping could be estimated by SIMS. However, SIMS beam spot size is too large to focus on the small area of silicon pillar. At this juncture, TCAD simulation was used to match the experimental transfer curve [see Fig. 3(a)] to gain understanding. By varying the interface trap density, effective gate length and junction profile, body doping concentration, source/drain doping level, and abruptness, it is concluded that high V_t could be attributed to the Si pillar being counterdoped by boron from p^+ poly-Si. Since we used a heavily doped poly-Si gate, the subsequent thermal process seems to have caused boron segregation into the channel and inevitably altered the doping level. The TCAD estimation showed the pillar surface doping concentration to be close to $10^{18}/cm^3$. Therefore, this result suggests that a high work function metal gate, such as TiN, must be used in future fabrication.

Verifying the charge conduction path would be valuable to provide an understanding of whether the carrier conducts through the surface or the center of the pillar. Fig. 4(a) shows the ON-state drain current (I_{ds}) distribution for various Si pillar diameters. The larger Si pillar diameter showed a greater drive current. The I_{ds} distribution of Fig. 4(a) is redrawn as a box plot as a function of diameter, as shown in Fig. 4(b). While the box-plot data are the measurement result, the two lines labeled by perimeter and by area are estimated. These two lines are estimated as follows. First, a median value of I_{ds} from $D =$ 65 nm is selected as a reference. Herein, $D = 65$ nm was the largest in the experimental split. Then, each line is respectively drawn by scaling the reference current (I_{ds} @ $D = 65$ nm) by perimeter, i.e., $I_{ds}(D) = I_{ds}(D = 65\text{ nm}) \times \pi \cdot D / \pi \cdot 65$, and by area, i.e., $I_{ds}(D) = I_{ds}(D = 65\text{ nm}) \times \pi \cdot (D/2)^2 / \pi \cdot (65/2)^2$. The measurement statistics follows more closely with the area scaling trend rather than the perimeter scaling. This suggests the device operation to be in the volume inversion regime.

IV. Simulation of Rowhammer and Soft Error

Rowhammer has been a major reliability challenge since its first report in [2]. It can be illicitly used to hack PCs, cloud

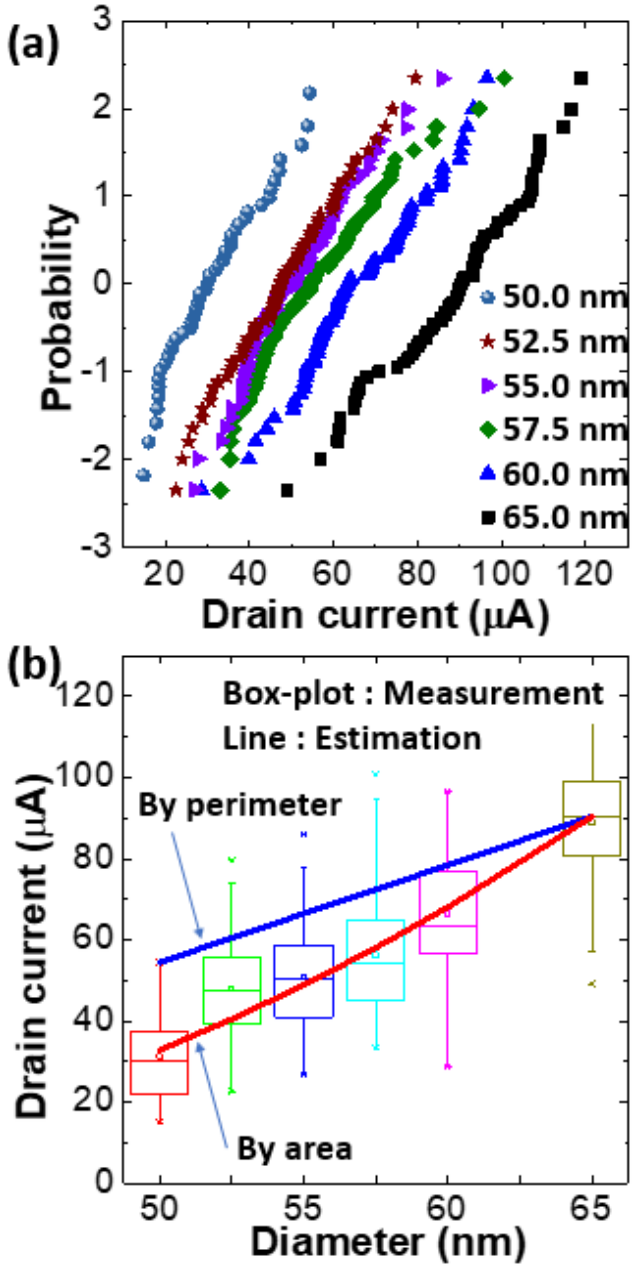

Fig. 4. (a) ON-state I_{ds} distribution (I_{ds} @ $V_{gs} = 3$ V and $V_{ds} = 1.2$ V) for various Si pillar diameters. The larger diameter showed a greater ON-state current. (b) Box plot of I_{ds} distribution (error bar) and estimated I_{ds} scaled according to the perimeter (blue line) and area (red line).

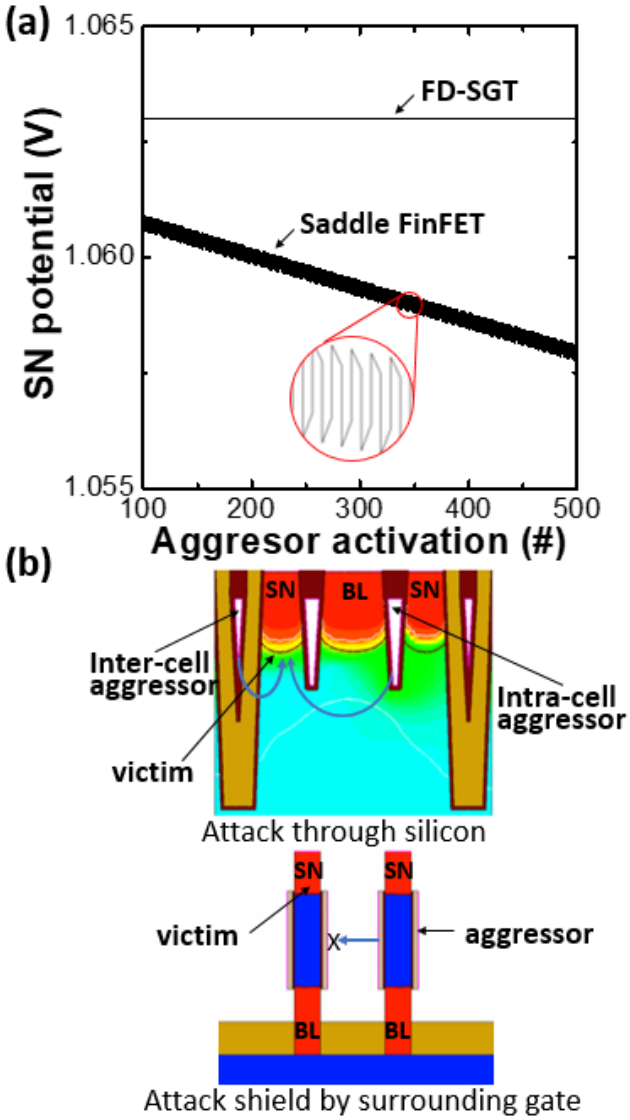

Fig. 5. (a) TCAD simulation result of rowhammer characteristics and (b) SGT and saddle FinFET device structures used in the simulations. The SN voltage drops due to the repeated activation of the intracell aggressor in the saddle FinFET and the aggressor in the SGT are monitored.

servers, and mobile systems [16]–[19]. TCAD simulation was carried out to verify the superior rowhammer immunity of the SGT over the conventional saddle FinFET. The saddle FinFET model used in [20] was borrowed, and the SGT model was newly built and calibrated with the experimental result, using the rowhammer simulation method in [21].

Fig. 5(a) shows the simulation result of the SN potential drift due to repeated activation of adjacent WL. Such adjacent WLs that attack and the target are referred to as the aggressor. Whereas a gradual potential loss is found in the saddle FinFET, the SN potential is not affected in SGT. In the current DRAM technology, rowhammer is attributed to the fact that the shared BL makes one active region for two cells, as illustrated in Fig. 5(b). In addition, two additional WLs are passing in the proximity of the sidewalls of the active area as labeled in the intercell aggressor and within the same active fin as labeled in the intracell aggressor, respectively. When the aggressor is repeatedly activated in the saddle FinFET, the stored charges in the target cell (victim) are lost as a result of generated leakage current and resultantly lowered threshold voltage [19]. The advantage of the SGT is straightforward that each Si pillar is entirely surrounded by only one dedicated WL, which is fully decoupled from neighboring aggressors. In other words, if the entire surface of the body region is dedicated to only its own WL, no perturbation from an aggressor is expected. Consequently, when the DRAM technology eventually migrates to the surround gate, the rowhammer problem will inherently be removed.

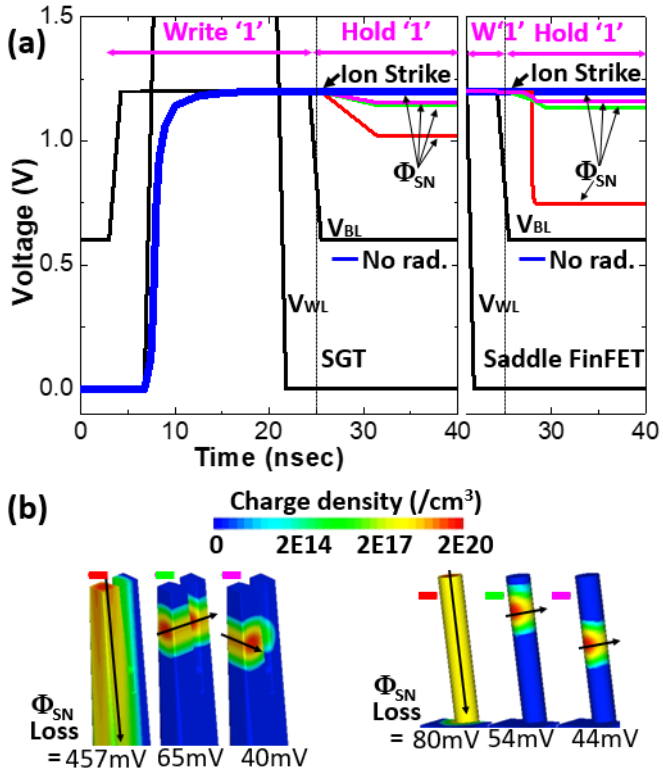

Fig. 6. (a) Simulation result of write "1" and Φ_{SN} loss due to ionizing radiation along with various ion incident angles and (b) ionized charge density for respective conditions. The red, pink, and green indices correspond to the red, pink, and green lines of Φ_{SN} in (a), respectively.

The architectural advantage of the SGT is addressed next. As technology scales down, the critical charge (minimum charge to bit-flip) is reduced accordingly [22]. The greater soft error susceptibility in bulk FinFETs compared with surround gate FET is known [23] from a logic technology perspective. The soft error immunity of the FD-SOI is due to its limited sensitive volume [24]. Similarly, the soft error tolerance of the FD-SGT is compared against the saddle FinFET.

Fig. 6(a) shows the SN potential (Φ_{SN}) change due to write "1" operation followed by ionizing radiation with linear energy transfer (LET) of 1 MeV·cm^2/mg during hold "1" condition. The ionizing particles can transverse in any random direction in nature. In this simulation, however, three representative incident angles are considered. These directions and locations are shown in Fig. 6(b). The quantitative value of the SN potential loss, $\Delta\Phi_{SN}$, is disclosed for each corresponding cases. When the ion transverses through in-plain direction (green and pink lines), both saddle FinFET and SGT show small and similar Φ_{SN} loss due to the limited transverse silicon length. However, when the ion vertically strikes through the SN (red line), i.e., worst case, a significantly different result is seen. The saddle FinFET lost $\Delta\Phi_{SN} = 457$ mV, whereas the SGT lost only $\Delta\Phi_{SN} = 80$ mV. This is due to the fact that the radiation-sensitive volume is bound by the S/D junctions and the surround gate in the SGT, whereas the bulk volume in the saddle FinFET offers greater ionization.

Future work should consider SEG process variability, gate length variability, BL disturb characteristics, and the impact of BL-to-SN parasitic capacitance. As this article is limited to only unit transistors by skipping the STI step, further work on memory array fabrication, capacitor integration and data retention, and operation timing parameter analysis needs to be done to assess a higher level of feasibility. Also, when the epitaxially grown channel is used, process variability induced crystal imperfections, such as dislocations, may cause leakage current. Even a high leakage current of a weak transistor tends to be lower than the noise floor of a parametric analyzer. Likewise, a high level of GIDL current of an individual transistor might not have been measured with our present test capability. In this case, an array of transistors connected in parallel can provide the total leakage current at a measurable level, and such an in-depth leakage analysis with a modified test structure will be necessary for future work. As illustrated in Fig. 5(b), the WL is buried inside the trenched channel in the saddle FinFET. This means that there is no WL-to-WL coupling. However, a pair of adjacent WLs is directly facing each other in the SGT array, which may suffer from a significant WL-to-WL coupling capacitance. Therefore, the impact of WL-to-WL coupling capacitance needs to be deeply investigated in terms of crosstalk, timing delay, and power consumption. As the SGT features a large surface-to-volume ratio in its channel, surface-related challenges, such as random telegraph noise (RTN) and low-frequency noise (LFN), would become important aspects. Such attributes are common for all gate-all-around nanowire FETs, and RTN and LFN issues in nanowire FETs have been addressed before [25]–[28]. The specific impact of RTN and LFN on DRAM operation needs further consideration in the future.

V. Conclusion

A new SGT is presented for a DRAM cell. An epitaxially grown channel is attained with a gate-all-around structure. In the proposed cell, the metal BL would be connected to the cell transistor through a buried n^+ conductive bridge, overcoming the large resistance of buried n^+ diffusion BL compared with previous SGTs. TCAD simulation results show favorable rowhammer and soft-error characteristics. The fully isolated Si pillar demonstrates rowhammer-free operation. The limited body volume makes the SGT more soft-error tolerant compared with saddle FinFETs.

Acknowledgment

The electronic design automation (EDA) Tool was supported by the IC Design Education Center.

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