TECHNISCHE UNIVERSITÄT
CHEMNITZ

Professur
Betriebssysteme

Embedded Software Lab

Lab 5 - Plug-Fest

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In this lab, you will test your code for interoperability. It is a good idea to solve task 5.1 before implementing Layer 4 to find subtle bugs preventing interoperability.

Initial Remarks

The tasks should be solved in the given order. If you do not manage to solve all tasks in preparation of the next lab meeting, make sure that you solve them afterwards. Your final grade at the end of the semester depends on the availability of *all* solutions in your code repository.

The presentation of your results during the lab slot is oral. There is *no need for preparing slides* or any other kind of written material.

Be ready to answer questions, both from the peer group reviewing you and the supervisors. Have your code, positive and negatives experiences and according documentation available.

Both team mates must participate in the presentation and discussion of results.

For the coding part, please avoid playing with the boot / read / write lock bits, playing with the Fuse bits or writing to the boot loader memory. Writing to EEPROM regions is also not needed at the moment.

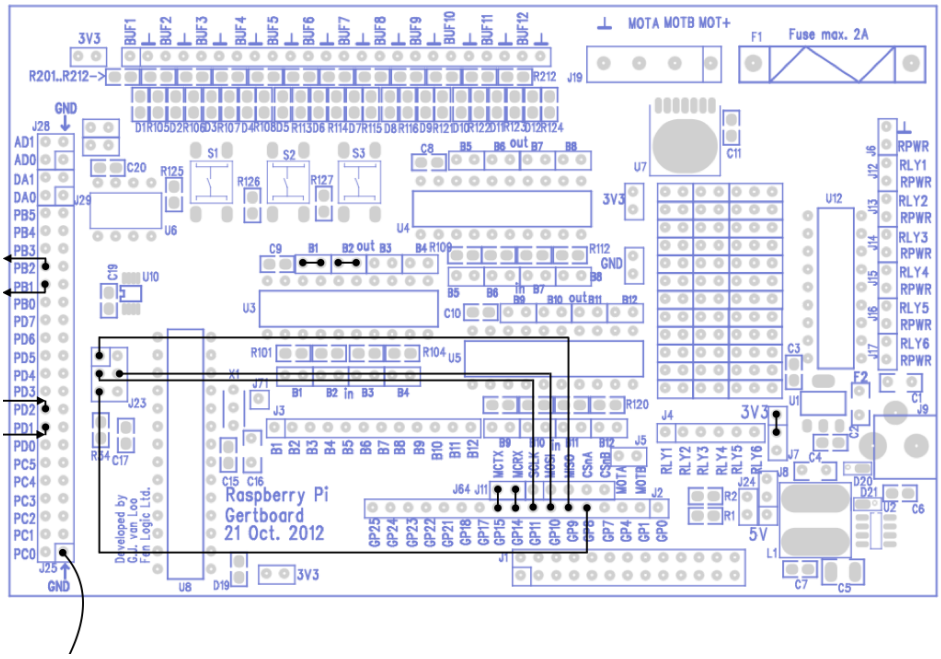

Figure 1: Gertboard wiring scheme for group collaboration.

Task 5.1

Prepare the Gertboard wiring according to Figure 1. If a wiring already exists, check it for correctness.

Based on this wiring scheme, test your implementation against yourself. For that take a second (not used by another student) Pi. Copy your code onto it and test, if interoperability with yourself works. Try to remove the data cable while your code is running, so that the message cannot be send to the receiver or the ACK-message cannot be send to the sender.

Task 5.2

Based on this wiring scheme, test your implementation against the implementation of another group. Try to remove the data cable while your code is running, so that the message cannot be send to the receiver or the ACK-message cannot be send to the sender.

References