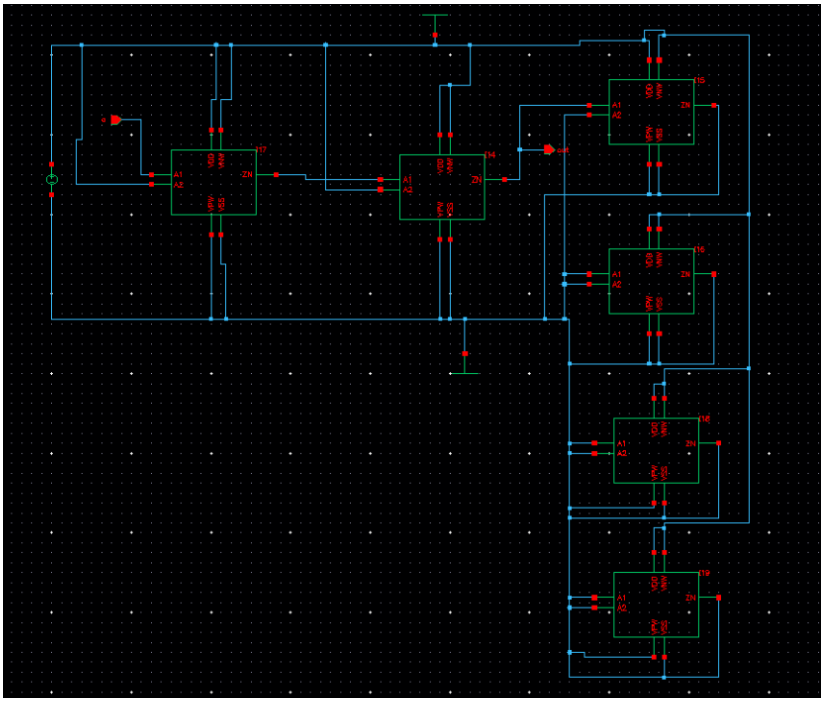
Phillip Seaton

FO1: delay = g+p

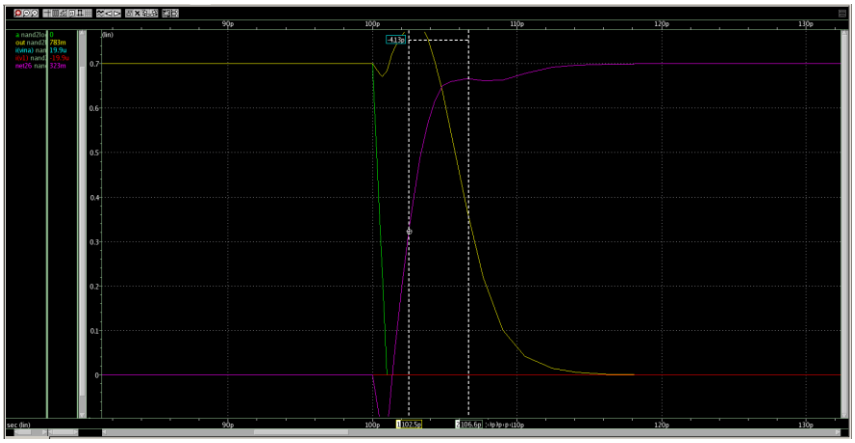
FO4: delay = 4g+p

Solving systems of equations for each case

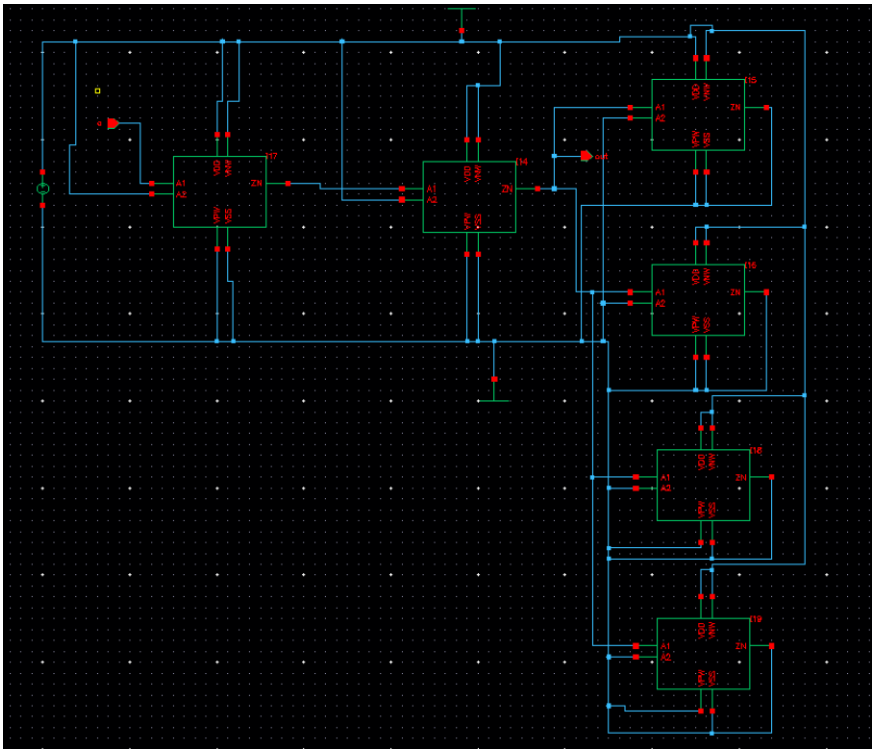
	FO1 Delay	FO4 Delay	G	P
NAND2x1	4.13 ps	8.46 ps	1.44ps	2.68ps
NAND2x2	4.15 ps	8.62 ps	1.49ps	2.66ps
NAND3x1	5.62 ps	10.87 ps	1.75ps	3.87ps
NAND3x2	5.75 ps	11.08 ps	1.78ps	3.97ps
NAND4x1	7.05 ps	13.47 ps	2.14ps	4.91ps
NAND4x2	7.14 ps	13.66 ps	2.17ps	4.97ps



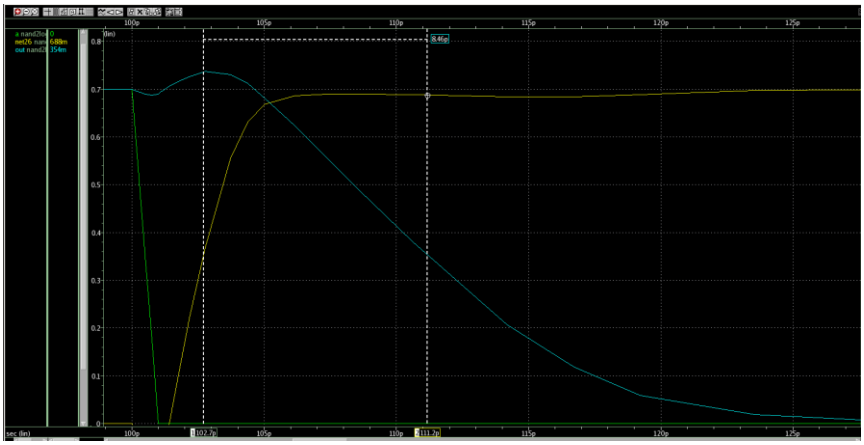
Nand2 with FO1, the three other nand gates' inputs are connected to ground



Nand2 FO1 results



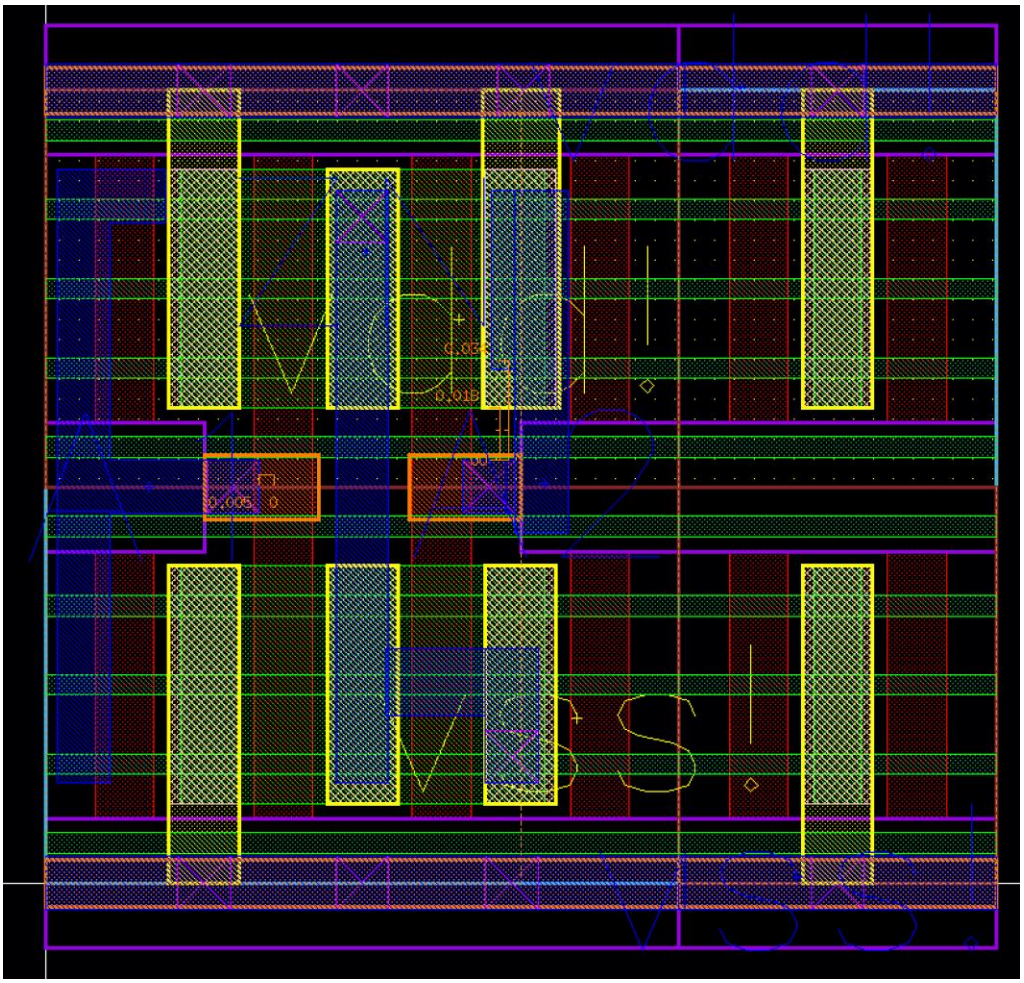
Nand2 with FO4, The output goes into 4 inputs

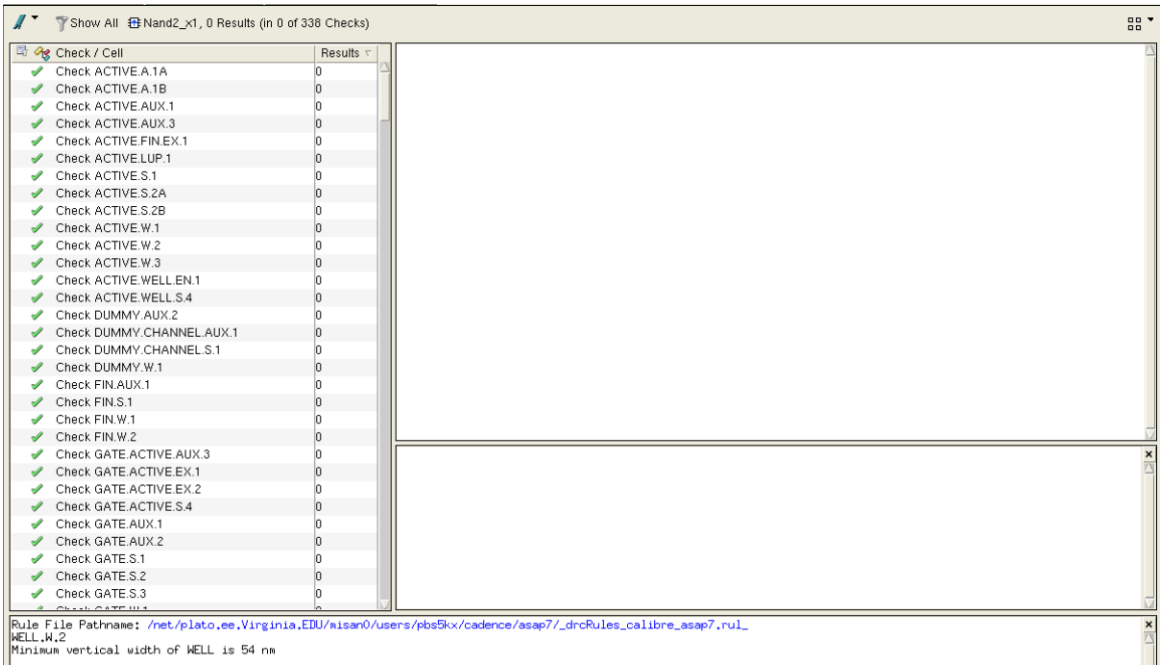


Nand2 FO4 results

LAYOUTS

Nand2_x1




Show All
Nand2_x1, 0 Results (in 0 of 338 Checks)
Check / Cell
Results
Check ACTIVE.A.1A 0
Check ACTIVE.A.1B 0
Check ACTIVE.AUX.1 0
Check ACTIVE.AUX.3 0
Check ACTIVE.FIN.EX.1 0
Check ACTIVE.LUP.1 0
Check ACTIVE.S.1 0
Check ACTIVE.S.2A 0
Check ACTIVE.S.2B 0
Check ACTIVE.W.1 0
Check ACTIVE.W.2 0
Check ACTIVE.W.3 0
Check ACTIVE.WELL.EN.1 0
Check ACTIVE.WELL.S.4 0
Check DUMMY.AUX.2 0
Check DUMMY.CHANNEL.AUX.1 0
Check DUMMY.CHANNEL.S.1 0
Check DUMMY.W.1 0
Check FIN.AUX.1 0
Check FIN.S.1 0
Check FIN.W.1 0
Check FIN.W.2 0
Check GATE.ACTIVE.AUX.3 0
Check GATE.ACTIVE.EX.1 0
Check GATE.ACTIVE.EX.2 0
Check GATE.ACTIVE.S.4 0
Check GATE.AUX.1 0
Check GATE.AUX.2 0
Check GATE.S.1 0
Check GATE.S.2 0
Check GATE.S.3 0
Rule File Pathname: /net/plato.ee.Virginia.EDU/misan0/users/pbs5kx/cadence/asap7/_drcRules_calibre_asap7.rul_
WELL.W.2
Minimum vertical width of WELL is 54 nm

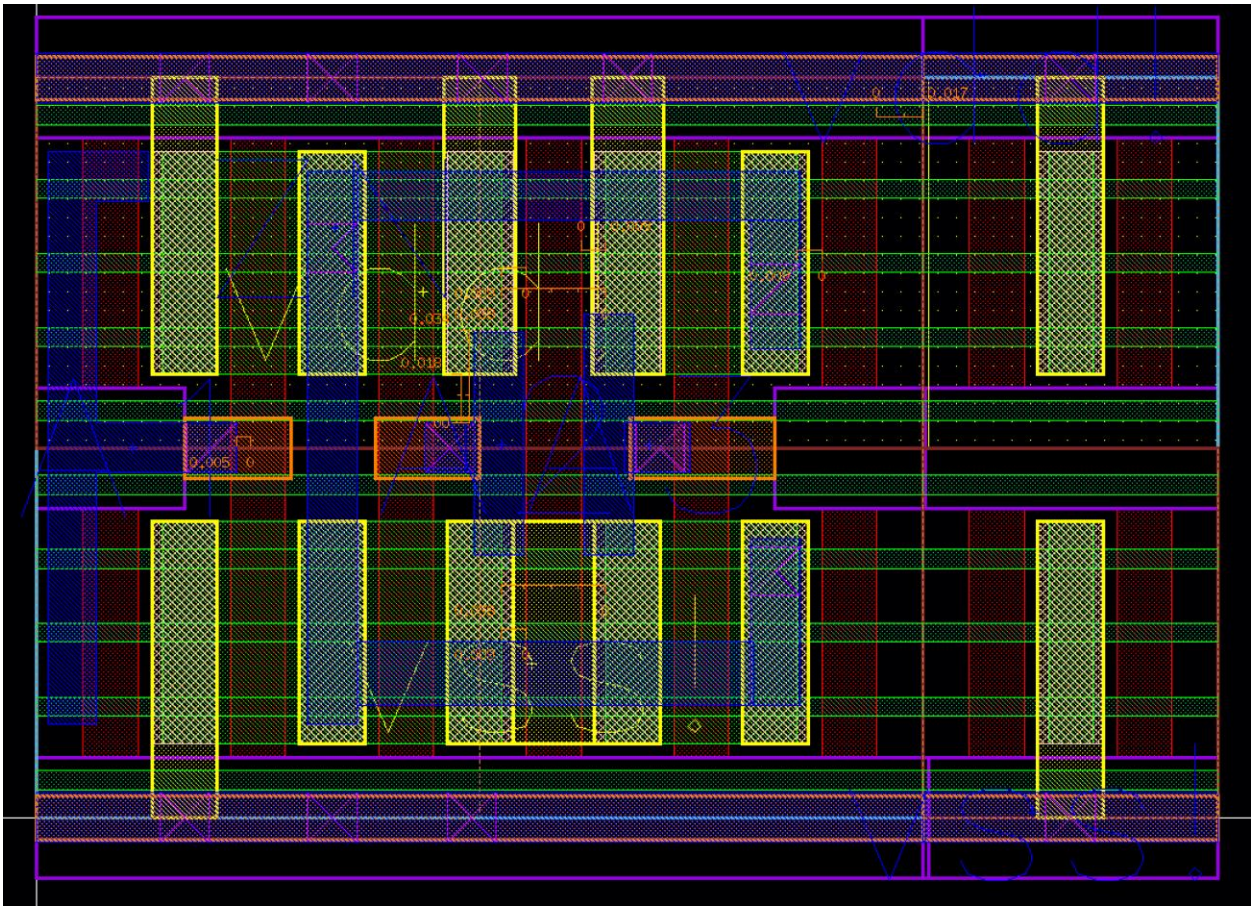
Comparison Results ×

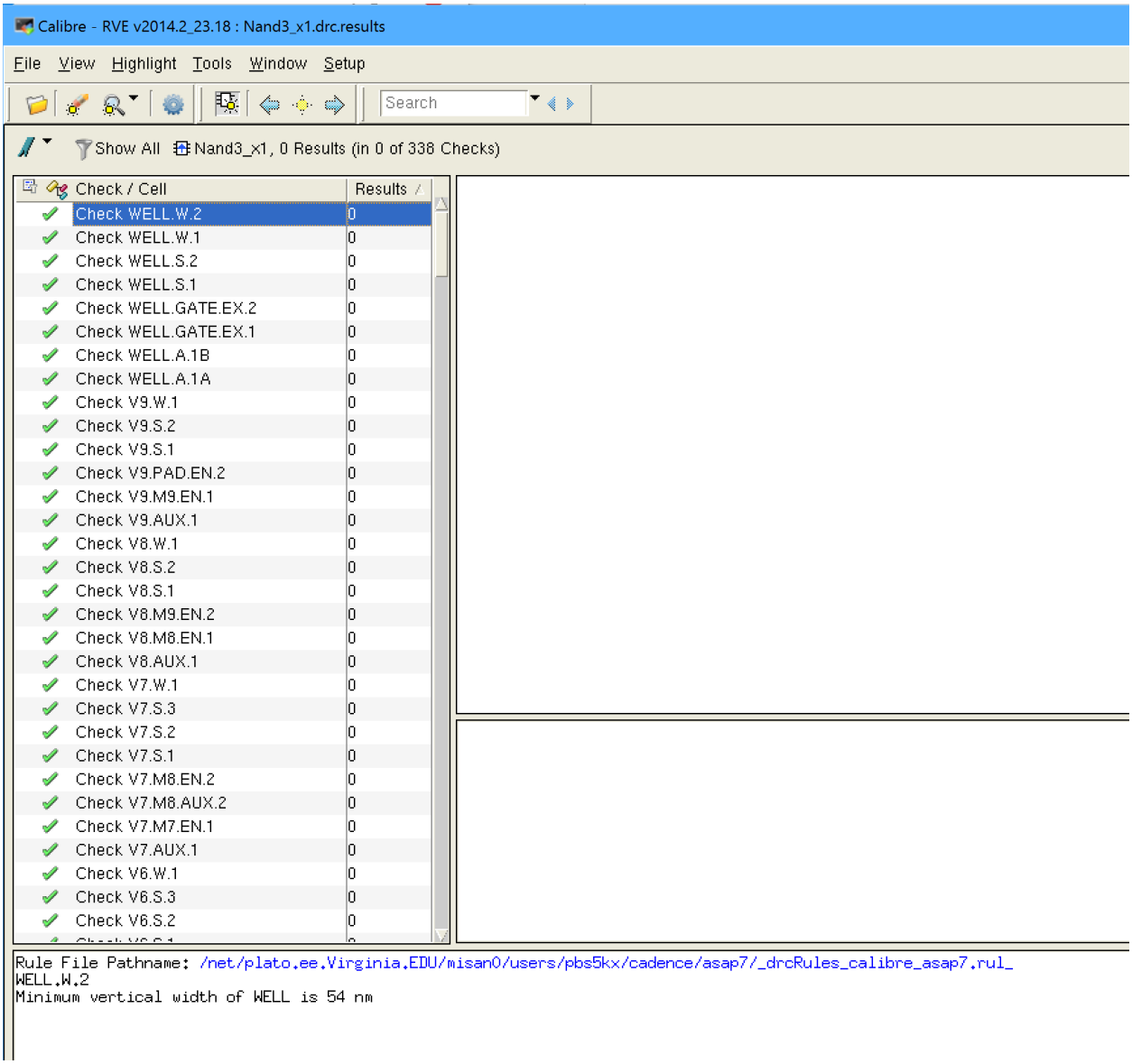
Layout Cell / Type	Source Cell	Nets	Instances
Nand2_x1	Nand2_x1	5L, 5S	1L, 1S

Cell Nand2_x1 Summary (Clean)

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                       #       ###################       _   _
                      #        #                 #       *   *
                    #   #      #     CORRECT     #         |
                     # #       #                 #       \___/
                      #        ###################


LAYOUT CELL NAME:         Nand2_x1
SOURCE CELL NAME:         Nand2_x1

------------------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               6         6

 Instances:          2         2         MN (4 pins)
                     2         2         MP (4 pins)
                ------    ------
 Total Inst:         4         4


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              5         5

 Nets:               5         5
```

Nand3_x1




Calibre - RVE v2014.2_23.18 : Nand3_x1.drc.results
File View Highlight Tools Window Setup
Search
Show All
Nand3_x1, 0 Results (in 0 of 338 Checks)
Check / Cell
Results
Check WELL.W.2 0
Check WELL.W.1 0
Check WELL.S.2 0
Check WELL.S.1 0
Check WELL.GATE.EX.2 0
Check WELL.GATE.EX.1 0
Check WELL.A.1B 0
Check WELL.A.1A 0
Check V9.W.1 0
Check V9.S.2 0
Check V9.S.1 0
Check V9.PAD.EN.2 0
Check V9.M9.EN.1 0
Check V9.AUX.1 0
Check V8.W.1 0
Check V8.S.2 0
Check V8.S.1 0
Check V8.M9.EN.2 0
Check V8.M8.EN.1 0
Check V8.AUX.1 0
Check V7.W.1 0
Check V7.S.3 0
Check V7.S.2 0
Check V7.S.1 0
Check V7.M8.EN.2 0
Check V7.M8.AUX.2 0
Check V7.M7.EN.1 0
Check V7.AUX.1 0
Check V6.W.1 0
Check V6.S.3 0
Check V6.S.2 0
Rule File Pathname: /net/plato.ee.Virginia.EDU/misan0/users/pbs5kx/cadence/asap7/_drcRules_calibre_asap7.rul_
WELL.W.2
Minimum vertical width of WELL is 54 nm

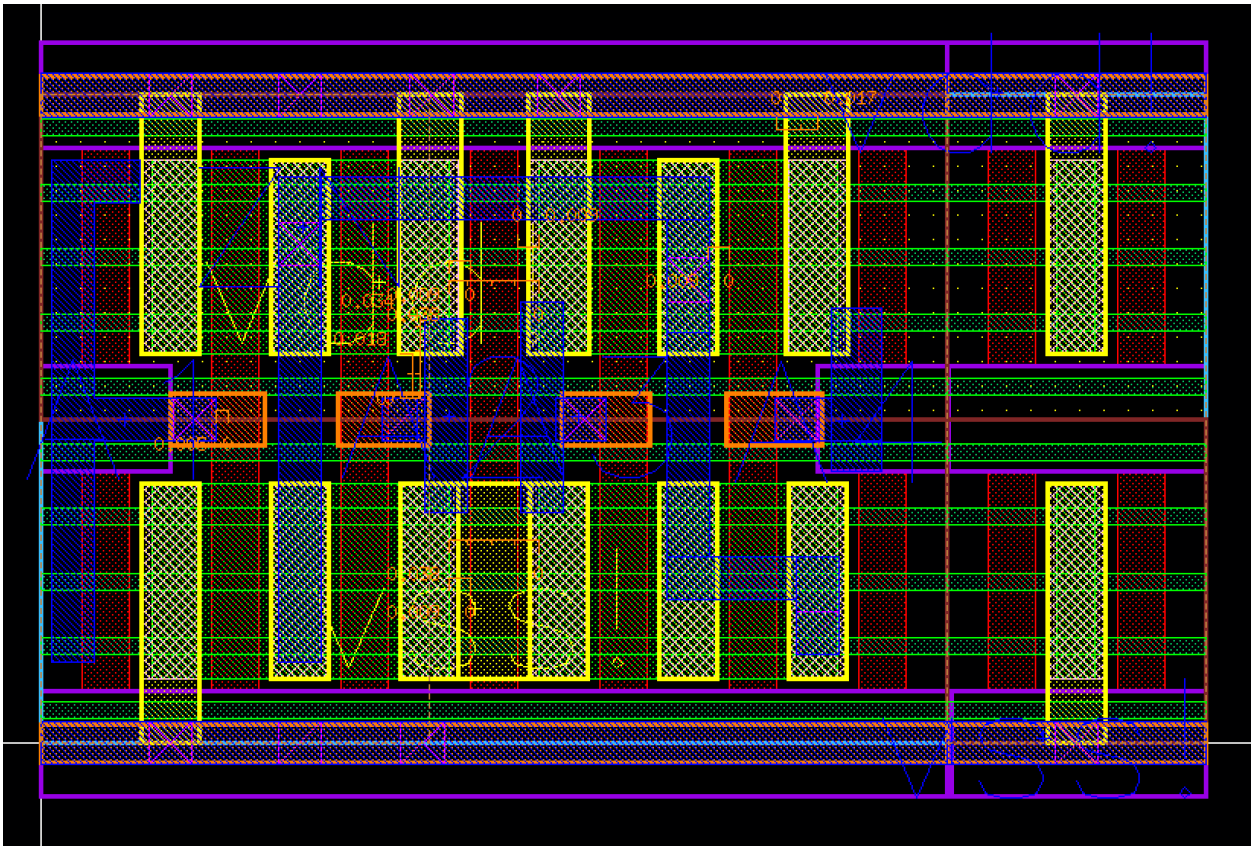
Comparison Results ×

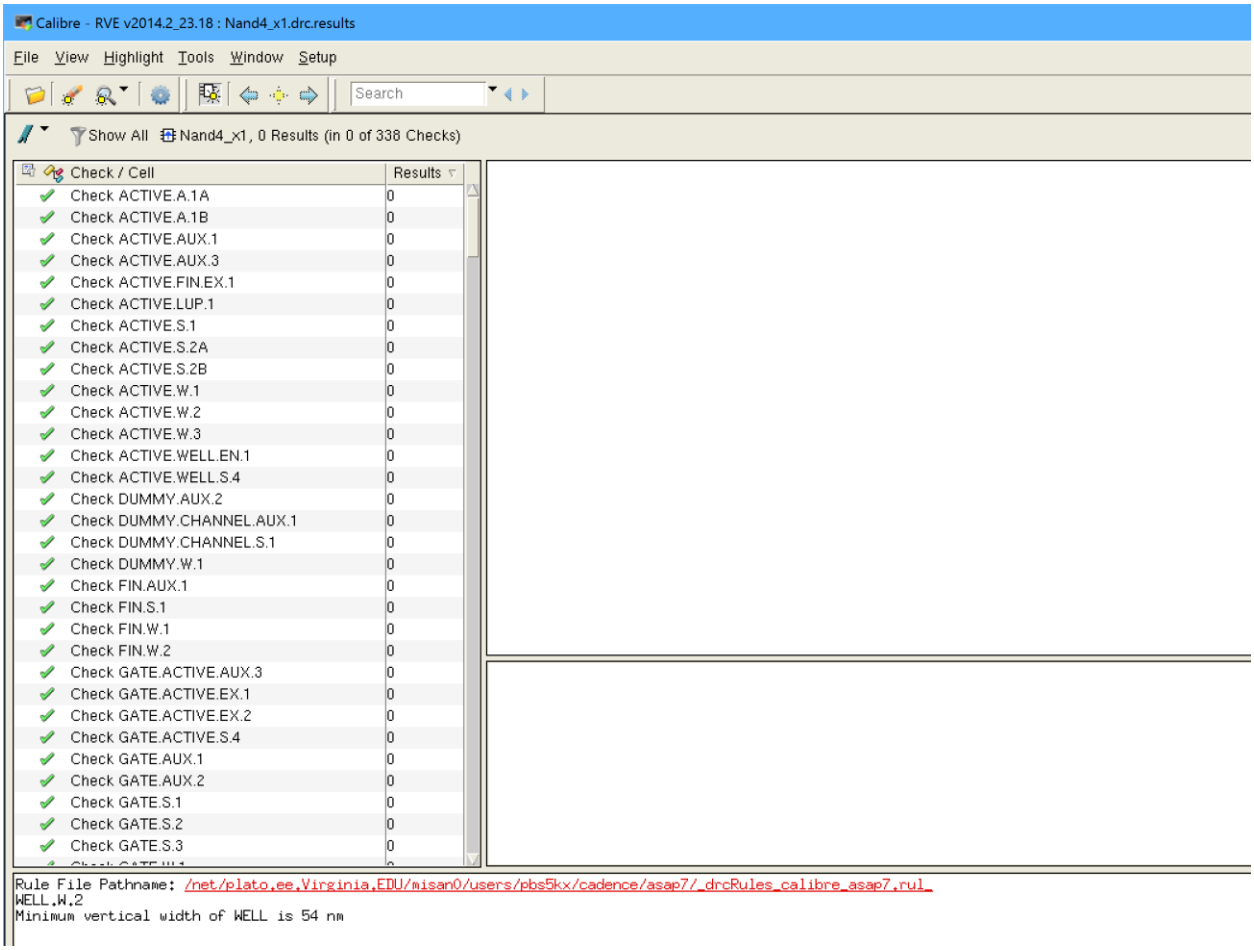
Layout Cell / Type	Source Cell	Nets	Instances	Ports
Nand3_x1	Nand3_x1	6L, 6S	1L, 1S	6L, 6S

Cell Nand3_x1 Summary (Clean)

```
                  CELL COMPARISON RESULTS ( TOP LEVEL )


                       #       ###################       _   _
                     #         #                 #       *   *
                  #    #       #     CORRECT     #         |
                   # #         #                 #       \___/
                    #          ###################


LAYOUT CELL NAME:         Nand3_x1
SOURCE CELL NAME:         Nand3_x1

-------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              6         6

 Nets:               8         8

 Instances:          3         3         MN (4 pins)
                     3         3         MP (4 pins)
                ------    ------
 Total Inst:         6         6

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              6         6

 Nets:               6         6
```

Nand4_x1




Calibre - RVE v2014.2_23.18 : Nand4_x1.drc.results
File View Highlight Tools Window Setup
Search
Show All Nand4_x1, 0 Results (in 0 of 338 Checks)
Check / Cell
Results
Check ACTIVE.A.1A 0
Check ACTIVE.A.1B 0
Check ACTIVE.AUX.1 0
Check ACTIVE.AUX.3 0
Check ACTIVE.FIN.EX.1 0
Check ACTIVE.LUP.1 0
Check ACTIVE.S.1 0
Check ACTIVE.S.2A 0
Check ACTIVE.S.2B 0
Check ACTIVE.W.1 0
Check ACTIVE.W.2 0
Check ACTIVE.W.3 0
Check ACTIVE.WELL.EN.1 0
Check ACTIVE.WELL.S.4 0
Check DUMMY.AUX.2 0
Check DUMMY.CHANNEL.AUX.1 0
Check DUMMY.CHANNEL.S.1 0
Check DUMMY.W.1 0
Check FIN.AUX.1 0
Check FIN.S.1 0
Check FIN.W.1 0
Check FIN.W.2 0
Check GATE.ACTIVE.AUX.3 0
Check GATE.ACTIVE.EX.1 0
Check GATE.ACTIVE.EX.2 0
Check GATE.ACTIVE.S.4 0
Check GATE.AUX.1 0
Check GATE.AUX.2 0
Check GATE.S.1 0
Check GATE.S.2 0
Check GATE.S.3 0
Rule File Pathname: /net/plato.ee.Virginia.EDU/misan0/users/pbs5kx/cadence/asap7/_drcRules_calibre_asap7.rul_
WELL.W.2
Minimum vertical width of WELL is 54 nm

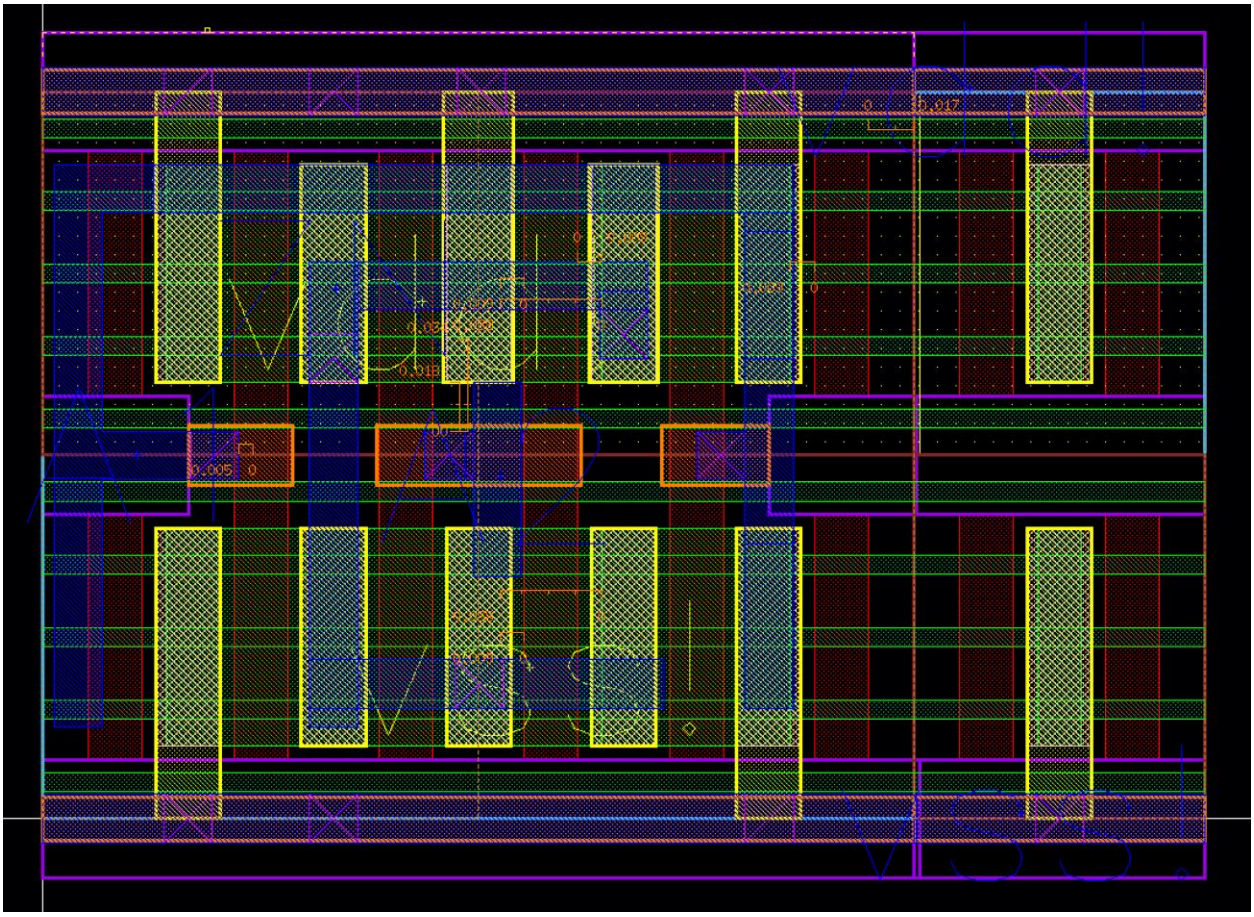
Comparison Results ×

Layout Cell / Type	Source Cell	Nets	Instances	Ports
Nand4_x1	Nand4_x1	7L, 7S	1L, 1S	7L, 7S

Cell Nand4_x1 Summary (Clean)

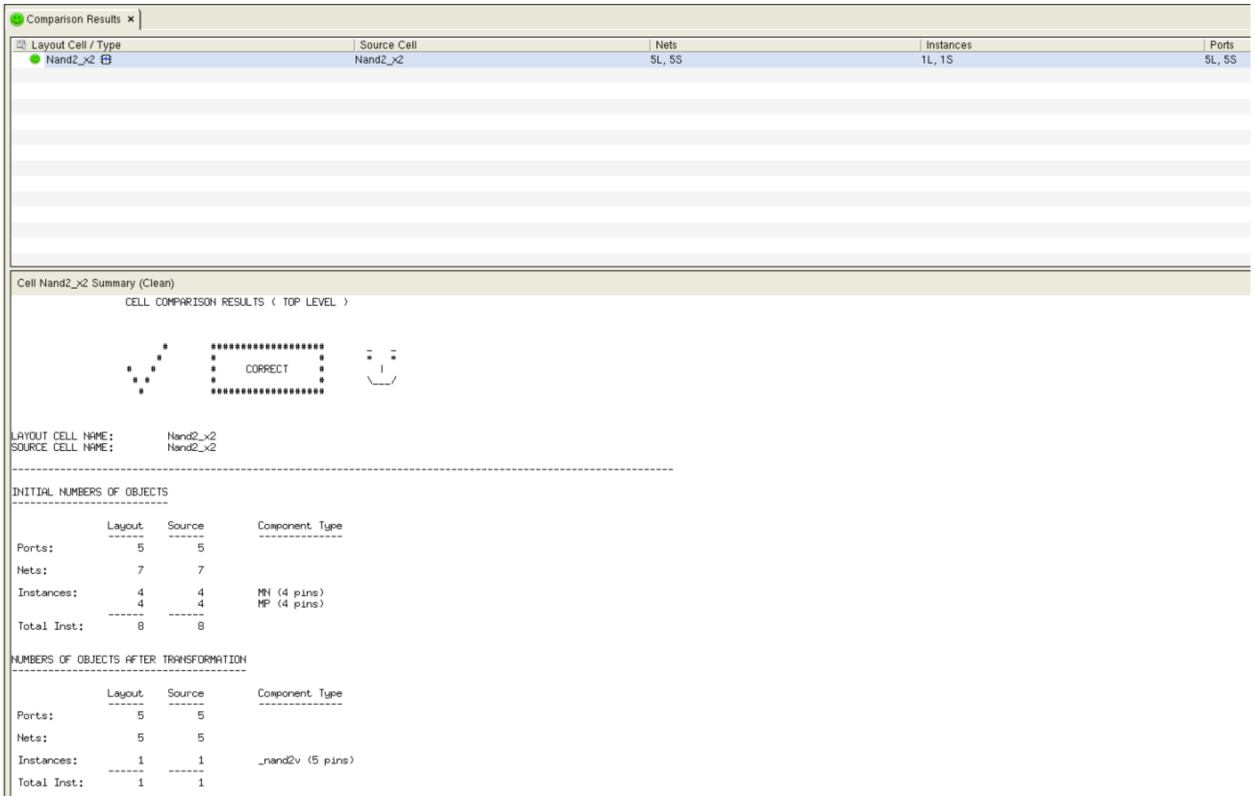
```
                  CELL COMPARISON RESULTS ( TOP LEVEL )


                       #       ###################       _   _
                      #        #                 #       *   *
                  #   #        #     CORRECT     #         |
                   # #         #                 #       \___/
                    #          ###################


LAYOUT CELL NAME:         Nand4_x1
SOURCE CELL NAME:         Nand4_x1

-------------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              7         7

 Nets:              10        10

 Instances:          4         4         MN (4 pins)
                     4         4         MP (4 pins)
                ------    ------
 Total Inst:         8         8

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              7         7

 Nets:               7         7
```

Nand2_x2



Check / Cell	Results
Check WELL.W.2	0
Check WELL.W.1	0
Check WELL.S.2	0
Check WELL.S.1	0
Check WELL.GATE.EX.2	0
Check WELL.GATE.EX.1	0
Check WELL.A.1B	0
Check WELL.A.1A	0
Check V9.W.1	0
Check V9.S.2	0
Check V9.S.1	0
Check V9.PAD.EN.2	0
Check V9.M9.EN.1	0
Check V9.AUX.1	0
Check V8.W.1	0
Check V8.S.2	0
Check V8.S.1	0
Check V8.M9.EN.2	0
Check V8.M8.EN.1	0
Check V8.AUX.1	0
Check V7.W.1	0
Check V7.S.3	0
Check V7.S.2	0
Check V7.S.1	0
Check V7.M8.EN.2	0
Check V7.M8.AUX.2	0
Check V7.M7.EN.1	0
Check V7.AUX.1	0
Check V6.W.1	0
Check V6.S.3	0
Check V6.S.2	0
Check V6.S.1	0
Check V6.M7.EN.2	0
Check V6.M7.AUX.2	0
Check V6.M6.EN.1	0

Rule File Pathname: /net/plato.ee.Virginia.EDU/misan0/users/pbs5kx/cadence/asap7/_drcRules_calibre_asap7.rul_
WELL.W.2
Minimum vertical width of WELL is 54 nm



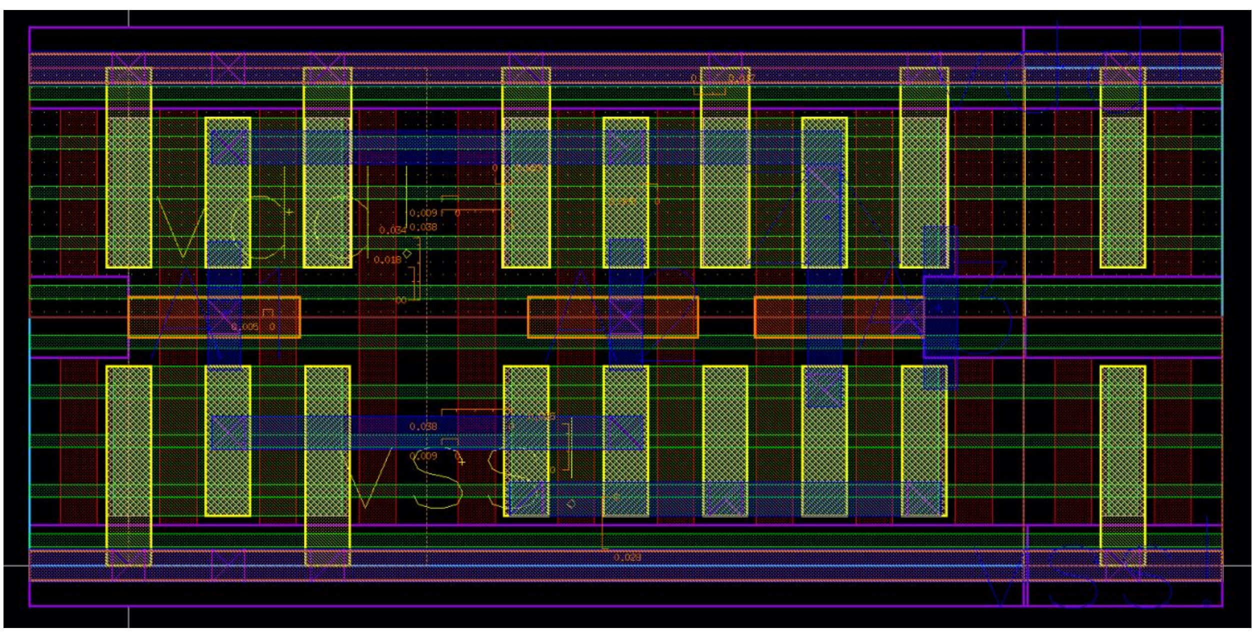
Comparison Results

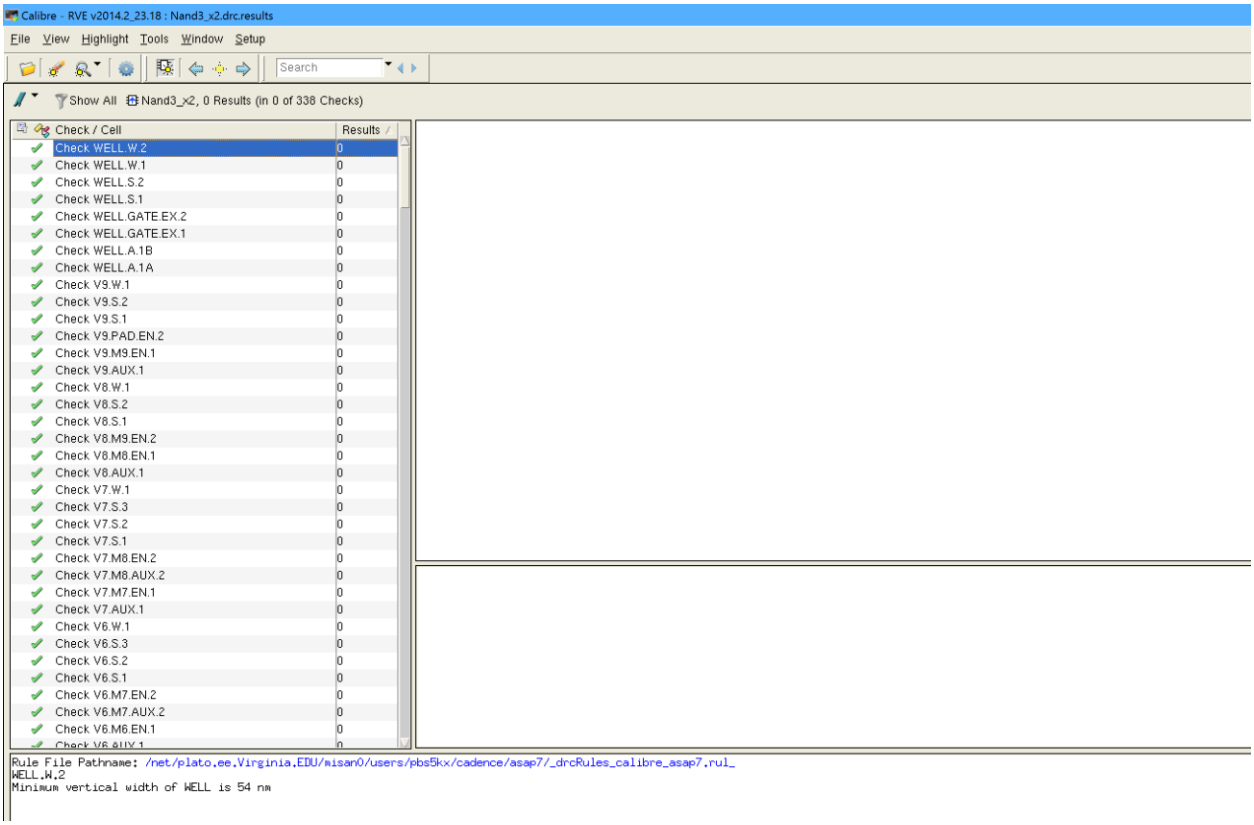
Layout Cell / Type	Source Cell	Nets	Instances	Ports
Nand2_x2	Nand2_x2	5L, 5S	1L, 1S	5L, 5S

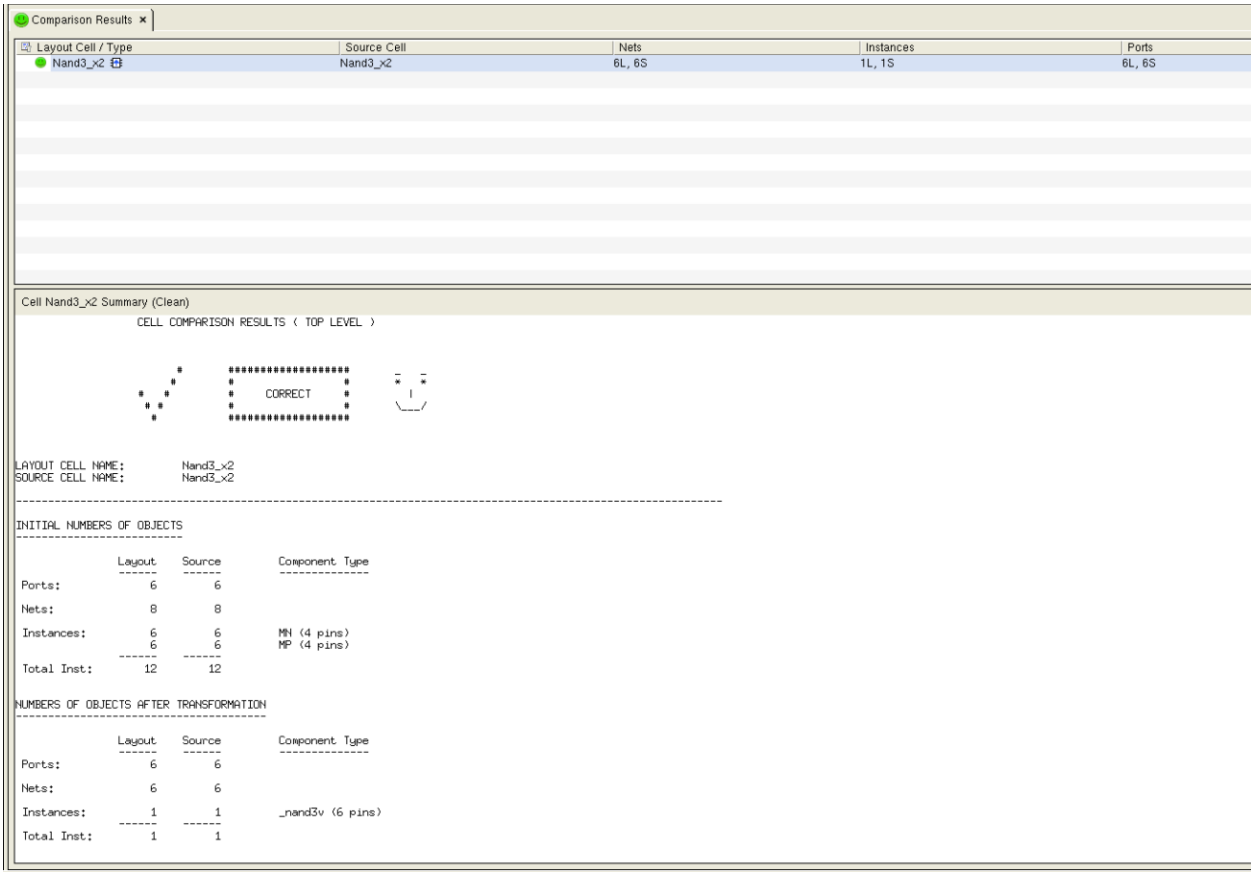
Cell Nand2_x2 Summary (Clean)

```
                CELL COMPARISON RESULTS ( TOP LEVEL )

                        #################
                        #               #
                        #    CORRECT    #
                        #               #
                        #################

LAYOUT CELL NAME:        Nand2_x2
SOURCE CELL NAME:        Nand2_x2

--------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:            5         5

 Nets:             7         7

 Instances:        4         4           MN (4 pins)
                   4         4           MP (4 pins)
                ------    ------
 Total Inst:       8         8

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:            5         5

 Nets:             5         5

 Instances:        1         1           _nand2v (5 pins)
                ------    ------
 Total Inst:       1         1
```

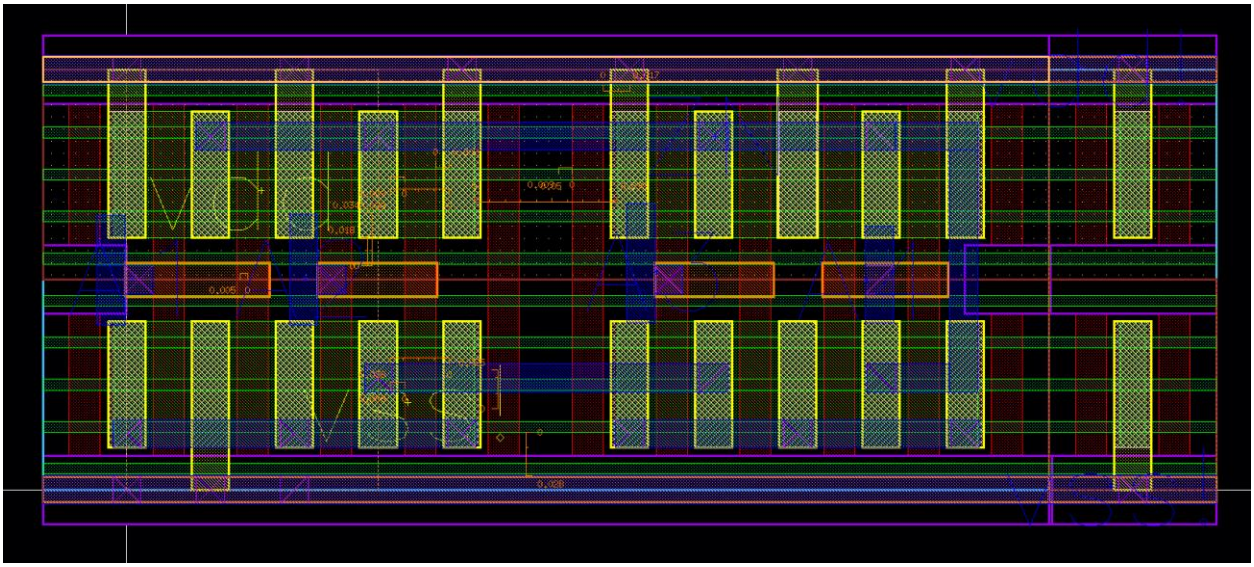
Nand3_x2




Calibre - RVE v2014.2_23.18 : Nand3_x2.drc.results
File View Highlight Tools Window Setup
Search
Show All
Nand3_x2, 0 Results (in 0 of 336 Checks)
Check / Cell
Results
Check WELL.W.2 0
Check WELL.W.1 0
Check WELL.S.2 0
Check WELL.S.1 0
Check WELL.GATE.EX.2 0
Check WELL.GATE.EX.1 0
Check WELL.A.1B 0
Check WELL.A.1A 0
Check V9.W.1 0
Check V9.S.2 0
Check V9.S.1 0
Check V9.PAD.EN.2 0
Check V9.M9.EN.1 0
Check V9.AUX.1 0
Check V8.W.1 0
Check V8.S.2 0
Check V8.S.1 0
Check V8.M9.EN.2 0
Check V8.M8.EN.1 0
Check V8.AUX.1 0
Check V7.W.1 0
Check V7.S.3 0
Check V7.S.2 0
Check V7.S.1 0
Check V7.M8.EN.2 0
Check V7.M8.AUX.2 0
Check V7.M7.EN.1 0
Check V7.AUX.1 0
Check V6.W.1 0
Check V6.S.3 0
Check V6.S.2 0
Check V6.S.1 0
Check V6.M7.EN.2 0
Check V6.M7.AUX.2 0
Check V6.M6.EN.1 0
Rule File Pathname: /net/plato.ee.Virginia.EDU/misan0/users/pbs5kx/cadence/asap7/_drcRules_calibre_asap7.rul_
WELL.W.2
Minimum vertical width of WELL is 54 nm


Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
Nand3_x2
Nand3_x2
6L, 6S
1L, 1S
6L, 6S
Cell Nand3_x2 Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: Nand3_x2
SOURCE CELL NAME: Nand3_x2
INITIAL NUMBERS OF OBJECTS
Layout Source Component Type
Ports: 6 6
Nets: 8 8
Instances: 6 6 MN (4 pins)
6 6 MP (4 pins)
Total Inst: 12 12
NUMBERS OF OBJECTS AFTER TRANSFORMATION
Layout Source Component Type
Ports: 6 6
Nets: 6 6
Instances: 1 1 _nand3v (6 pins)
Total Inst: 1 1

Nand4_x2



Show All Nand4_x2, 0 Results (in 0 of 338 Checks)

Check / Cell	Results
Check WELL.W.2	0
Check WELL.W.1	0
Check WELL.S.2	0
Check WELL.S.1	0
Check WELL.GATE.EX.2	0
Check WELL.GATE.EX.1	0
Check WELL.A.1B	0
Check WELL.A.1A	0
Check V9.W.1	0
Check V9.S.2	0
Check V9.S.1	0
Check V9.PAD.EN.2	0
Check V9.M9.EN.1	0
Check V9.AUX.1	0
Check V8.W.1	0
Check V8.S.2	0
Check V8.S.1	0
Check V8.M9.EN.2	0
Check V8.M8.EN.1	0
Check V8.AUX.1	0
Check V7.W.1	0
Check V7.S.3	0
Check V7.S.2	0
Check V7.S.1	0
Check V7.M8.EN.2	0
Check V7.M8.AUX.2	0
Check V7.M7.EN.1	0
Check V7.AUX.1	0
Check V6.W.1	0
Check V6.S.3	0
Check V6.S.2	0
Check V6.S.1	0
Check V6.M7.EN.2	0
Check V6.M7.AUX.2	0
Check V6.M6.EN.1	0

Rule File Pathname: /net/plato.ee.Virginia.edu/misan0/users/pbs5kx/cadence/_drcRules_calibre_asap7.rul_
WELL.W.2
Minimum vertical width of WELL is 54 nm

Comparison Results ×

Layout Cell / Type	Source Cell	Nets	Instances
Nand4_x2	Nand4_x2	7L, 7S	1L, 1S

Cell Nand4_x2 Summary (Clean)

```
                CELL COMPARISON RESULTS ( TOP LEVEL )


                      #       ###################       _   _
                     #        #                 #       *   *
                   #   #      #     CORRECT     #         |
                    # #       #                 #       \___/
                     #        ###################


LAYOUT CELL NAME:         Nand4_x2
SOURCE CELL NAME:         Nand4_x2

-------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             7         7

 Nets:             10        10

 Instances:         8         8         MN (4 pins)
                    8         8         MP (4 pins)
                ------    ------
 Total Inst:       16        16

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:             7         7

 Nets:              7         7

 Instances:         1         1         _nand4v (7 pins)
                ------    ------
 Total Inst:        1         1
```