COMPUTER ARCHITECTURE & DESIGN

3

HARDWARE DESCRIPTION LANGUAGE

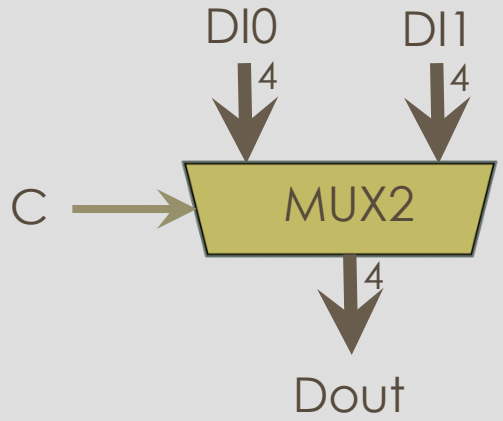
- For simulation and synthesis
  - VHDL
  - Verilog
- VHDL used for this class
  - VHDL is an acronym for VHSIC Hardware Description language
  - VHSIC is an acronym for Very High Speed Integrated Circuit

VHDL TERMS

- Every component is a ***design entity*** in VHDL
- Every design entity has two parts
  - ***Entity declaration***
    - Defines the design entity's interface
  - ***Architecture body***
    - Defines the design entity's internal behavior or structure
- Each design entity has only one entity declaration
- Each design entity may have one or more architecture bodies

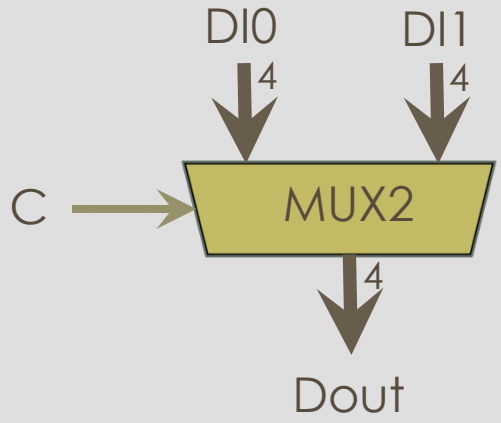
MULTIPLEXER EXAMPLE

- Consider a 2-to-1 Mux



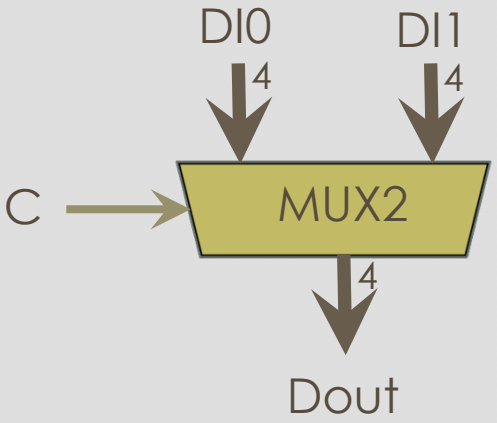
Each of the data busses is 4-bits wide

VHDL MUX ENTITY DECLARATION




```
ENTITY MUX2 IS
  PORT(DI0, DI1 : IN std_logic_vector(3 DOWNTO 0);
       Dout     : OUT std_logic_vector(3 DOWNTO 0);
       C        : IN std_logic);
END ENTITY MUX2;
```

VHDL MUX ARCHITECTURE




```
ARCHITECTURE Behavior OF MUX2 IS
BEGIN
  PROCESS(DI0, DI1, C)
  BEGIN
    IF (C = '0') THEN
      Dout <= DI0;
    ELSIF (C = '1') THEN
      Dout <= DI1;
    ELSE
      Dout <= "XXXX";
    END IF;
  END PROCESS;
END ARCHITECTURE Behavior;
```

SIMULATION OF TIME DELAYS

```
ARCHITECTURE Behavior OF MUX2 IS
BEGIN
  PROCESS(DI0, DI1, C)
  BEGIN
    IF (C = '0') THEN
      Dout <= DI0 AFTER 10ns;
    ELSIF (C = '1') THEN
      Dout <= DI1 AFTER 10ns;
    ELSE
      Dout <= "XXXX";
    END IF;
  END PROCESS;
END ARCHITECTURE Behavior;
```

Add an "AFTER" clause to the signal assignments

When this statement is processed, the value of DI1 at that time is scheduled to be assigned to Dout 10ns in the future.

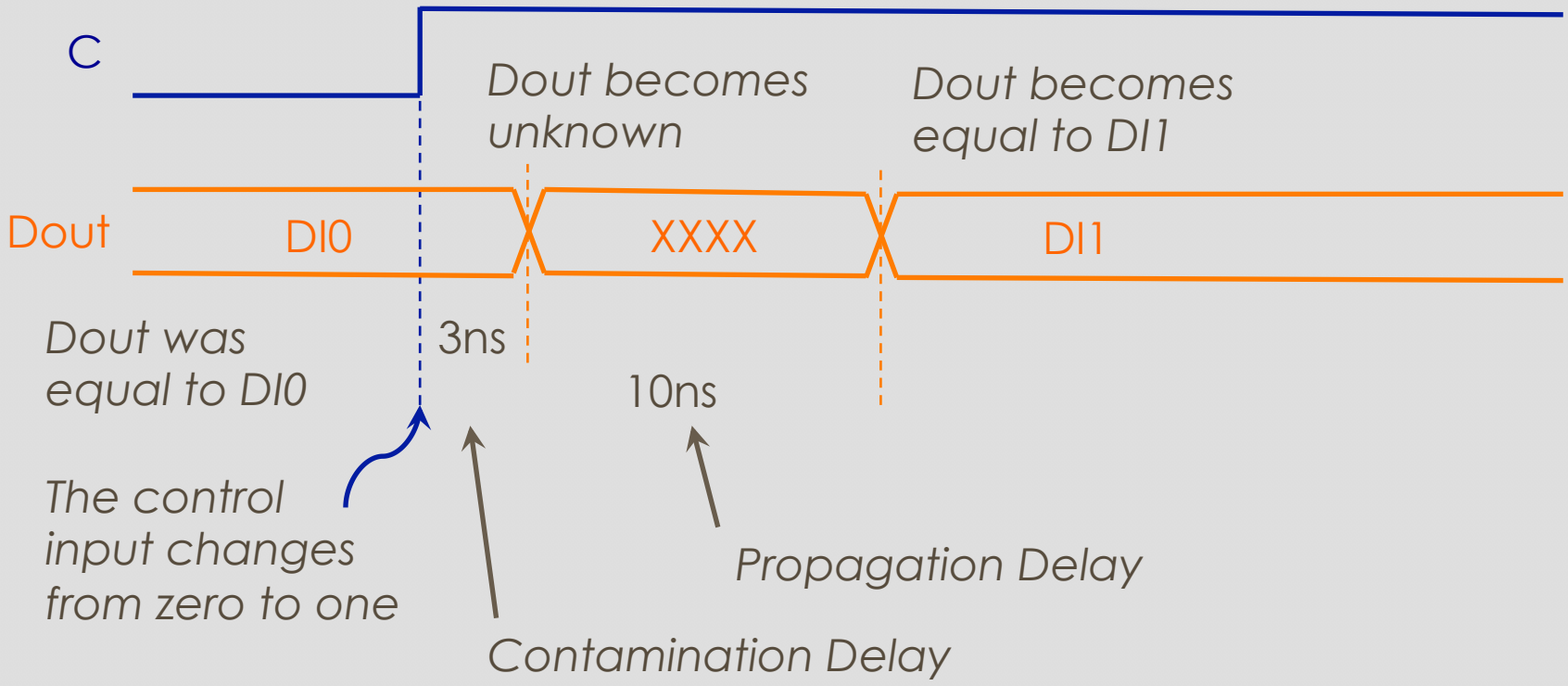
SIMULATING CONTAMINATION DELAYS

```
ARCHITECTURE Behavior OF MUX2 IS
BEGIN
  PROCESS(DI0, DI1, C)
  BEGIN
    IF (C = '0') THEN
      Dout <= "XXXX" AFTER 3ns, DI0 AFTER 10ns;
    ELSIF (C =
      Dout <= "XXXX" AFTER 3ns, DI1 AFTER 10ns;
    ELSE
      Dout <= "XXXX";
    END IF;
  END PROCESS;
END ARCHITECTURE Behavior;
```

When the signal assignment statement is executed, two assignments to Dout are scheduled.

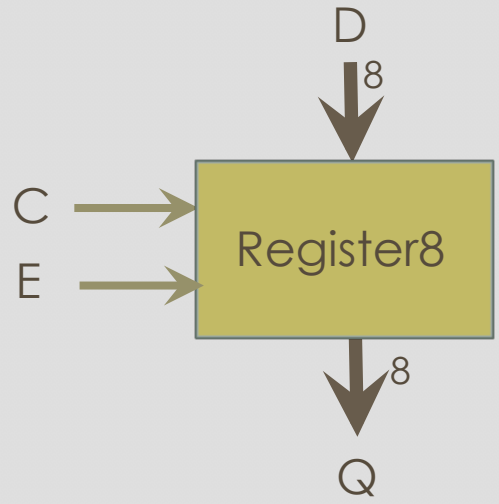
TIMING OF SIGNAL CHANGES

```
Dout <= "XXXX" AFTER 3ns, DI1 AFTER 10ns;
```



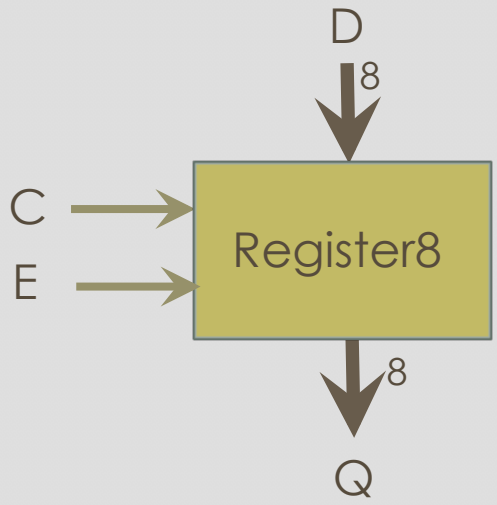
MODELING STORAGE

- Consider an 8-bit register



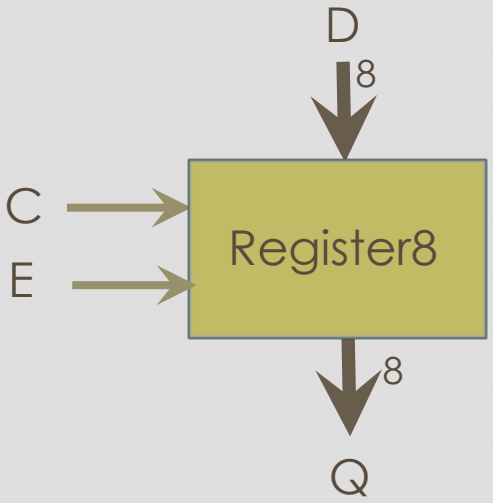
Register is rising-edge-triggered with enable.

VHDL REGISTER ENTITY DECLARATION




```
ENTITY Register8 IS
  PORT(D : IN std_logic_vector(7 DOWNTO 0);
       Q : OUT std_logic_vector(7 DOWNTO 0);
       C, E : IN std_logic);
END ENTITY Register8;
```

VHDL REGISTER ARCHITECTURE




```
ARCHITECTURE Behavior OF Register8 IS
BEGIN
  PROCESS(C)
  BEGIN
    IF (rising_edge(C) AND E='1') THEN
      Q <= D AFTER 10ns;
      ASSERT D'STABLE(2ns)
        REPORT "Setup Violation"
        SEVERITY WARNING;
    END IF;
  END PROCESS;
END ARCHITECTURE Behavior;
```

CHECK HOLD TIME

- Add another process to the architecture

```
PROCESS(C'DELAYED(1ns))
  BEGIN
    IF (rising_edge(C'DELAYED(1ns))) THEN
      ASSERT D'STABLE(1ns)
        REPORT "Hold Violation"
        SEVERITY WARNING;
    END IF;
  END PROCESS;
```

STD_LOGIC

- std_logic is not part of the VHDL language
  - It is provided in a library
- At the top of your file, you need:

```
LIBRARY IEEE;
USE ieee.std_logic_1164.all;
```