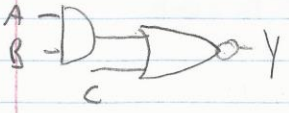
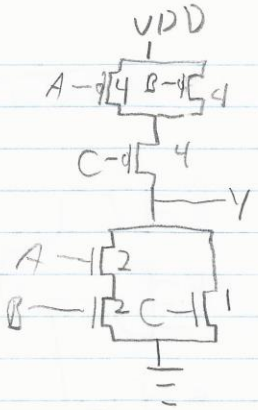
1. AOI21





$Y = \overline{AB + C}$

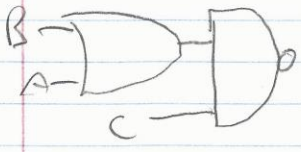
$g_A = \frac{4+2}{3} = 2$

$g_B = \frac{4+2}{3} = 2$

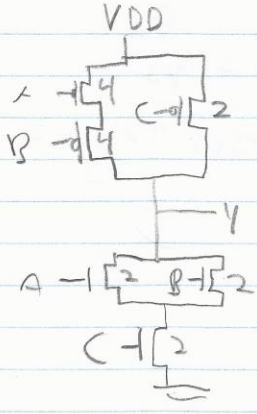
$g_C = \frac{4+1}{3} = \frac{5}{3}$

$P = \frac{4+2+1}{3} = \frac{7}{3}$

OAI21



$Y = \overline{(A+B)C}$



$g_A = \frac{6}{3} = 2$

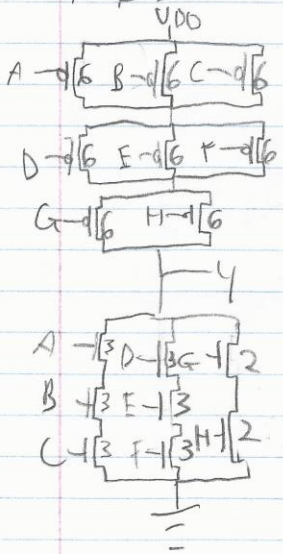
$S_5 = \frac{6}{3} = 2$

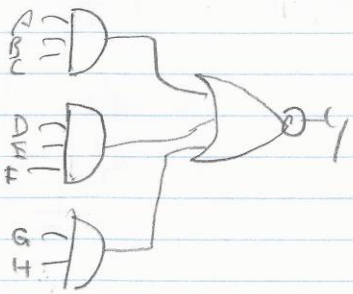
$g_C = \frac{4}{3}$

$P = \frac{(4+2+2+2)}{3} = \frac{10}{3}$

AOI 3 3 2

$Y = \overline{ABC + DEF + GH}$





$g_A = 9/3 = 3$

$g_B = 9/3 = 3$

$g_C = 9/3 = 3$

$g_D = 9/3 = 3$

$g_E = 9/3 = 3$

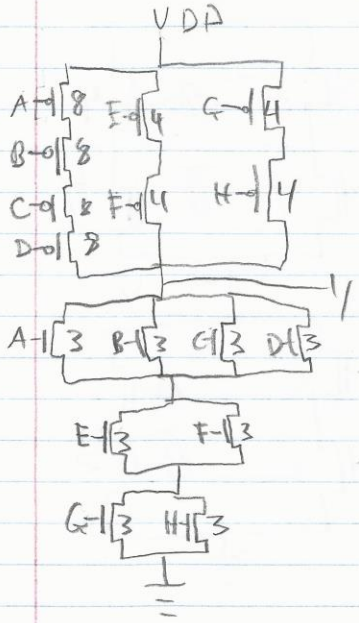
$g_F = 9/3 = 3$

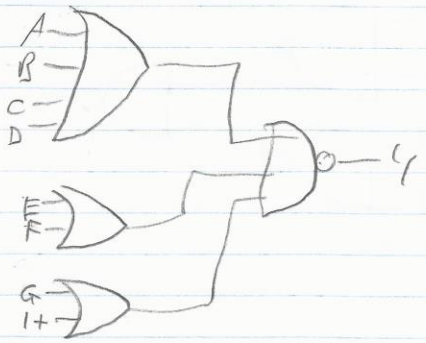
$g_G = 8/3$

$g_H = 8/3$

$P = (6+6+3+3+2)/3 = 20/3$

OAF427 $Y = \overline{(A+B+C+D)(E+F)(G+H)}$



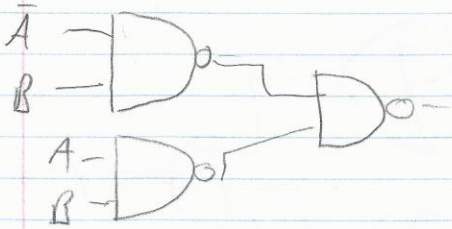


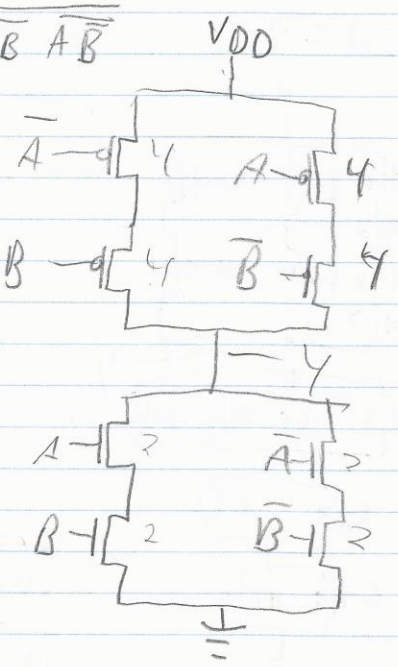
$g_A = 11/3$
$g_B = 11/3$
$g_C = 11/3$
$g_D = 11/3$
$g_E = 7/3$
$g_F = 7/3$
$g_G = 7/3$
$g_H = 7/3$

$P = (8+4+4+3+3+3+3+3)/3 = 28/3$

Xor

$A \oplus B = \bar{A}B + A\bar{B}$ $\quad Y = \overline{\overline{\bar{A}B}\ \overline{A\bar{B}}}$





$g_A = 6/3 = 2$

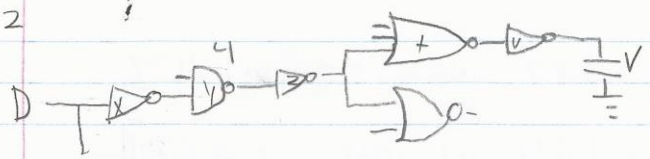
$g_{\bar{A}} = 6/3 = 2$

$g_B = 6/3 = 2$

$g_{\bar{B}} = 6/3 = 2$

$P = \frac{12}{3} = 4$

2



$G = 1 \cdot \frac{4}{3} \cdot 1 \cdot \frac{7}{3} \cdot 1 = 28/9$

$B = \frac{Con + Coff}{Con} = \frac{7+5}{7} = 12/7 \quad H = \frac{10000}{9}$

$F = GBH = \frac{28}{9} \cdot \frac{12}{7} \cdot \frac{10000}{9} = 5925.9$

$\hat{F} = \sqrt{5925.93} = 5.68$

$u = \frac{V \cdot 9V}{\hat{F}} = \frac{10000}{5.68} = 1760.6$

$t = \frac{u \cdot gt}{\hat{F}} = \frac{(1760.6)(7/3)}{5.68} = 723.3$

$z = \frac{t \cdot b \cdot 5z}{\hat{F}} = \frac{723.3(12/7) \cdot 1}{5.68} = 218.3$

$y = \frac{2 \, 5y}{\hat{F}} \quad \frac{218.3 \cdot 4/3}{5.68} = 51.2$

$x = \frac{51.2 \cdot 1}{5.68} \approx 9$

We do not include the branching when the D input goes to the three input and because it is not driven from the output of a gate and the capacitance starts at the inverter after D

V: $3s = 1760$ $s = 587$ $n_V = 587$ $p_V = 1174$

T: $7s = 723$ $s = 104$ $n_T = 104$ $p_T = 624$

Z: $3s = 218$ $s = 73$ $n_Z = 73$ $p_Z = 146$

Y: $4s = 512$ $s = 13$ $n_Y = 26$ $p_Y = 26$

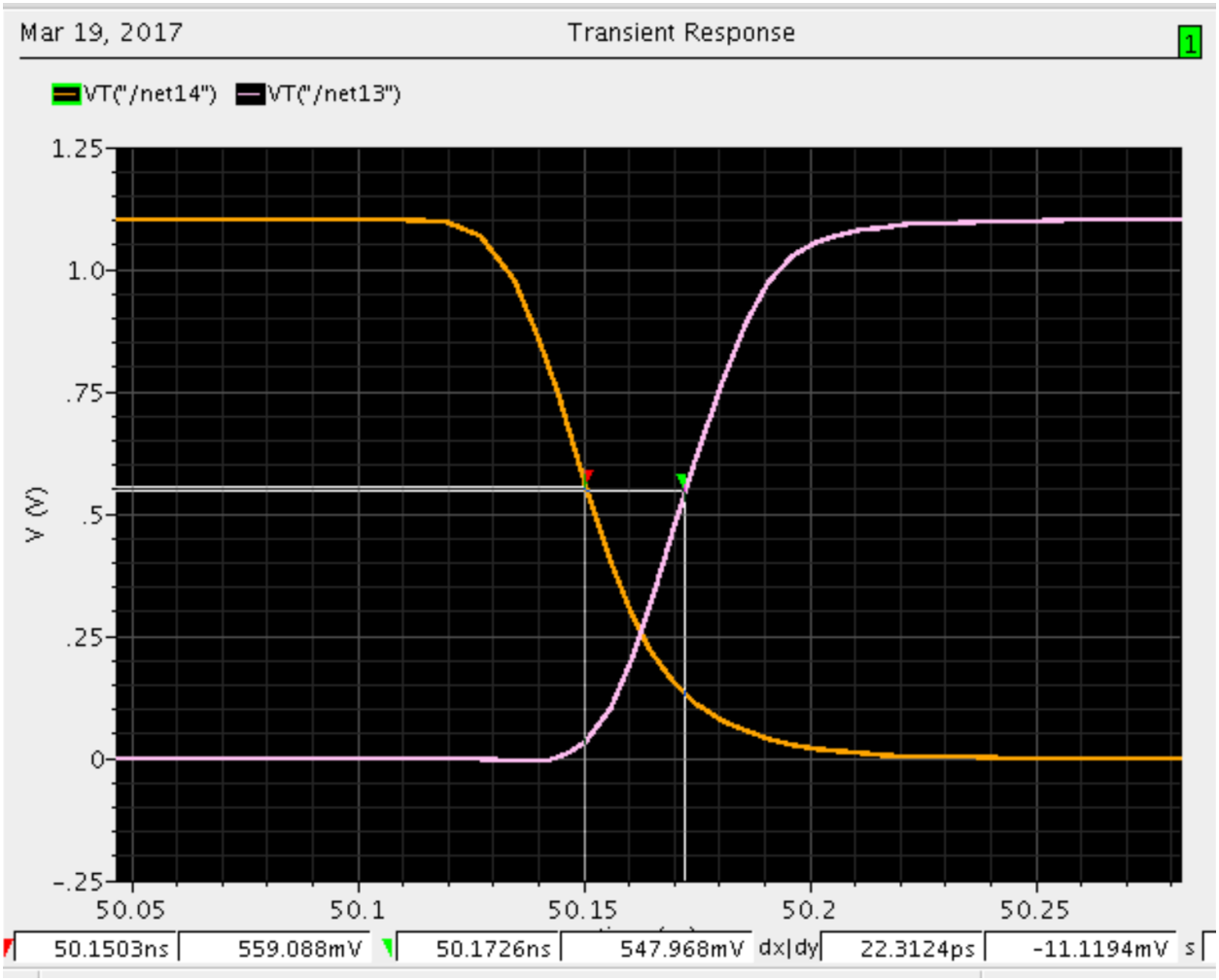
X $3s = 9$ $s = 3$ $n_X = 3$ $n_Y = 6$

$D = N\hat{t} + p$ $p = 1+1+1+2+3 = 8$

$D = 5(5.68) + 8 = 36.4$

One way to lower the delay is to reduce the output cap from 10000 to 1000 which makes $\hat{t} = 3.58$ and $D = 5*3.58+8 = 25.9$

3. For all the simulations, I took the delay between the two curves a 0.55V. All of the simulations looked similar to the Picture below.



FO4 Delay = 4g+p

F01 Delay = g+p

Solving systems of equations for each case

Given that FO4 inverter Delay is 15 ps. Which makes 15 = 4 * 1 +P P=11 for parasitic delay for inverter

Inverter

F04 D=18.21ps F01 D=14.96ps

G=1.08 This value is very close where the theoretical is 1

P=13.87ps This is very close to 1 * 11ps=11ps which is the theoretical delay

2-input nand

F04 D=26.326ps F01 D=22.312ps

G=1.336 This value is very close where the theoretical is 4/3

P=20.97ps This is very close to 2 * 11ps=22ps which is the theoretical delay

3-input nand

F04 D=34.52ps F01 D=29.63ps

G=1.63 This value is fairly close to the theoretical value of 5/3

P=27.9ps This value is close to the theoretical value of 3*11ps=33ps

2-input nor

F04 D=31.545ps F01 D=26.22ps

G=1.775 This value is fairly close to the theoretical value of 5/3

P=24.45ps This value is close to the theoretical value of 2*11ps=22ps

3-input nor

F04 D= 39.82ps F01 D=32.92ps

G=2.304 This value is fairly close to the theoretical value of 7/3

P=30.62ps This value is close to the theoretical value of 3*11ps=33ps

OAI21

F04 D=36.57ps F01 D=31.14ps

G=1.81 This value is fairly close to the theoretical value of 5/3

P=29.34ps This value is close to the theoretical value of(7/3)*11ps=25.7ps

4.

Critical path for circuit from problem 2

I used 1.2pF for output cap since a 90nm cmos had capacitance of 0.12fF. The input inverter is 9x the 90nm cap so the capacitance is 1.08fF. The output cap is (10000/90)*1.08fF=1.2pF

I found the delay to be: D=108.64ps

Our theoretical normalized delay was 36.4 and the normalized FO4 was 5.

So the Theoretical delay in ps is (36.4/5)*F04 inverter delay = 7.28 * 18.21ps = 132.569ps

132.6ps is fairly close to the 108.64ps simulated delay.