COMPUTER ARCHITECTURE & DESIGN
LAB 10

Objectives

The objective of this lab is to design the execution stage of the five-stage execution pipeline for the project ISA. The target instruction set architecture is described in the ISA document provided on the class web site.

This stage must receive inputs from the instruction decode and operand fetch stage designed in a previous lab. It must include an interface to provide jump and branch target addresses back to the instruction fetch stage. It must also produce a jump signal that goes back to the instruction fetch stage. Further, it must contain and manage the condition code register. Finally, it must provide outputs to the data memory stage that is next in the pipeline.

Tasks to be completed

- Determine the interfaces for this pipeline stage
- Build the datapath for your design using ModuleWare components
- Test your pipeline stage to confirm that it operates correctly

In Lab

Show your datapath to your TA. Describe the operation of the pipeline stage, and demonstrate that the pipeline stage works. Explain to your TA the range of tests that you have performed.