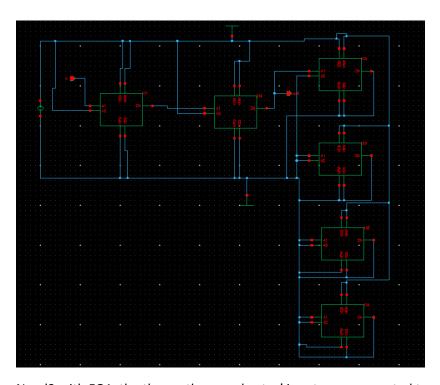
Phillip Seaton

FO1: delay = g+p

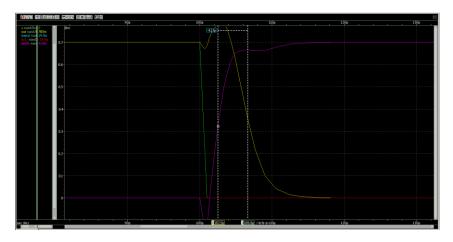
FO4: delay = 4g+p

Solving systems of equations for each case

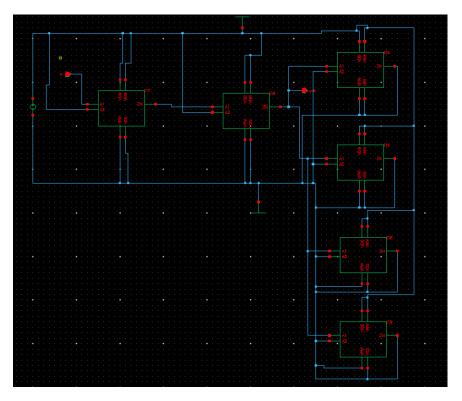
	FO1 Delay	FO4 Delay	G	Р
NAND2x1	4.13 ps	8.46 ps	1.44ps	2.68ps
NAND2x2	4.15 ps	8.62 ps	1.49ps	2.66ps
NAND3x1	5.62 ps	10.87 ps	1.75ps	3.87ps
NAND3x2	5.75 ps	11.08 ps	1.78ps	3.97ps
NAND4x1	7.05 ps	13.47 ps	2.14ps	4.91ps
NAND4x2	7.14 ps	13.66 ps	2.17ps	4.97ps



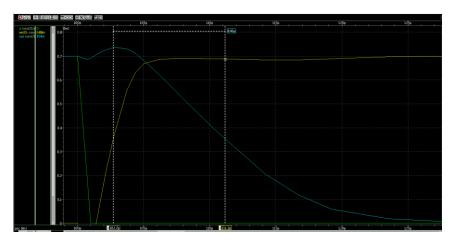
Nand2 with FO1, the three other nand gates' inputs are connected to ground



Nand2 FO1 results



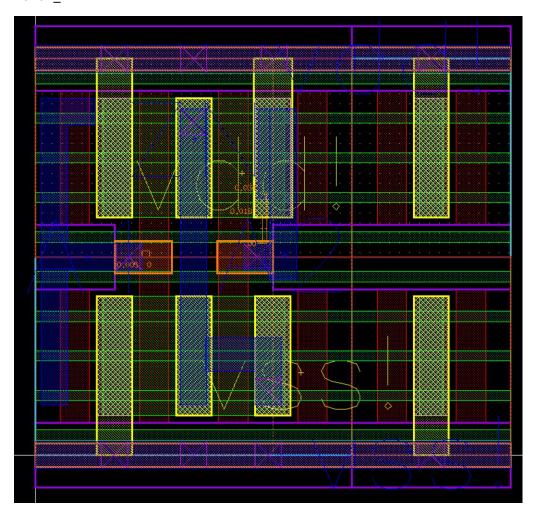
Nand2 with FO4, The output goes into 4 inputs

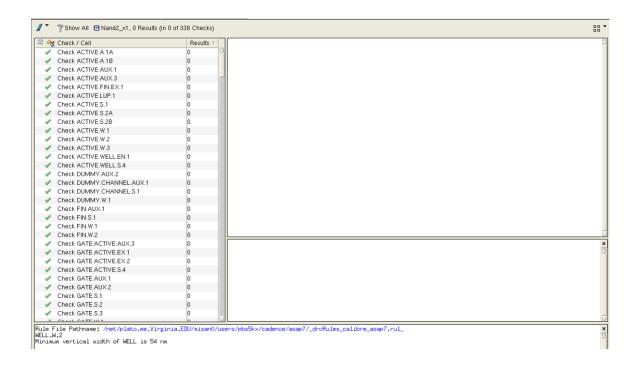


Nand2 FO4 results

LAYOUTS

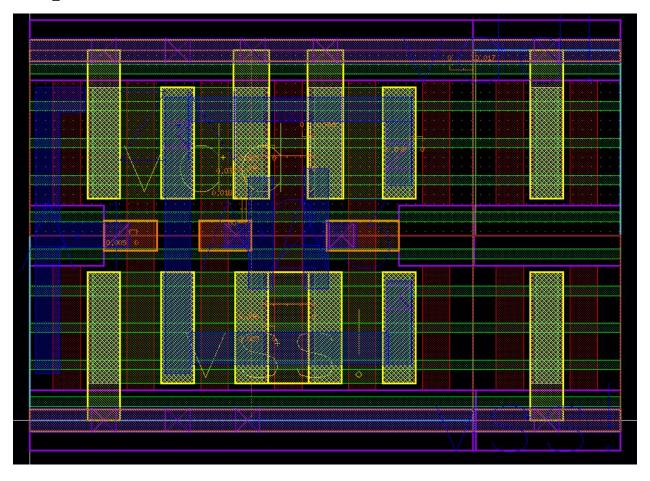
Nand2_x1

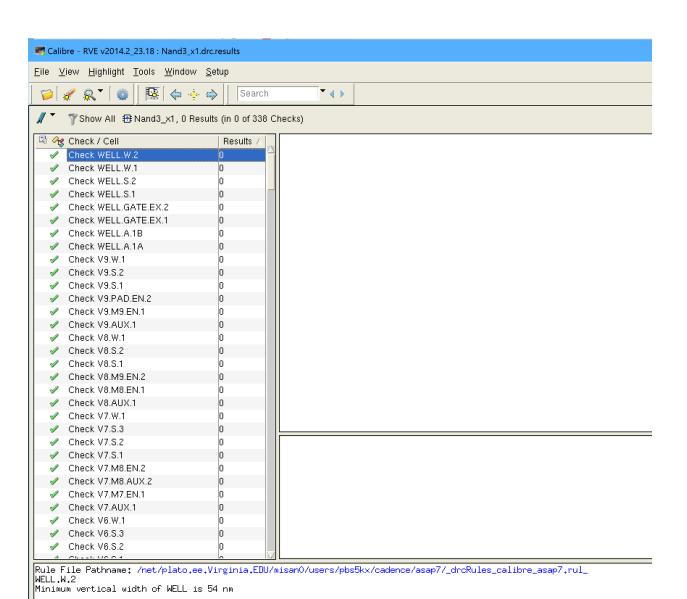




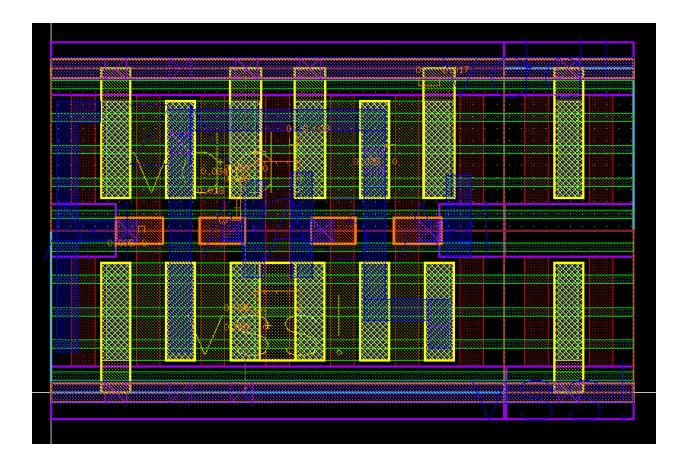
😃 Comparison Results 🗴 Source Cell 🖺 Layout Cell / Type Nets Instances Nand2_x1 ## Nand2_x1 5L, 5S 1L, 1S Cell Nand2_x1 Summary (Clean) CELL COMPARISON RESULTS (TOP LEVEL) ************** CORRECT **************** LAYOUT CELL NAME: SOURCE CELL NAME: Nand2_ $\times1$ Nand2_x1 INITIAL NUMBERS OF OBJECTS Layout Source Component Type 5 Ports: 5 6 6 Nets: 2 2 MN (4 pins) MP (4 pins) Instances: 4 Total Inst: NUMBERS OF OBJECTS AFTER TRANSFORMATION Component Type Layout Source Ports: 5 5 5 Nets:

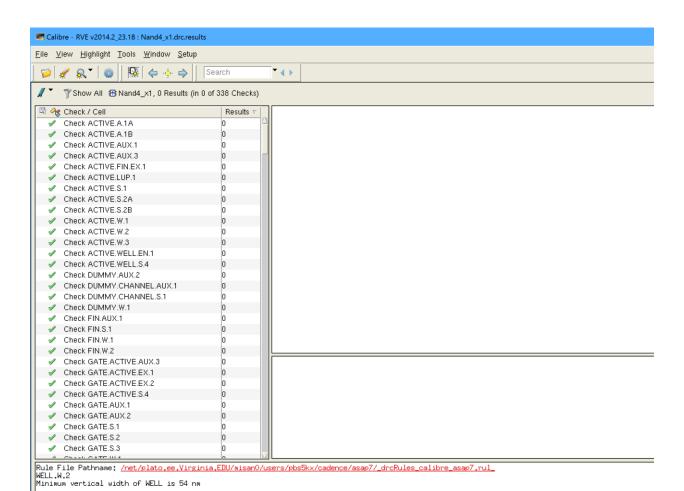
Nand3_x1





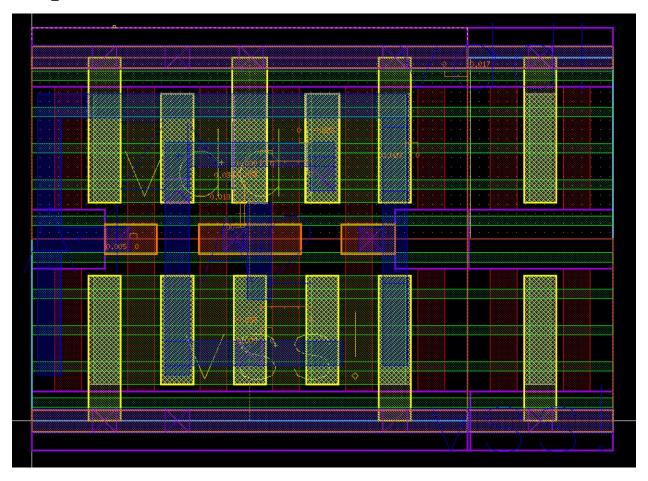
😃 Comparison Results 🗴 🖺 Layout Cell / Type Source Cell Nets Instances Ports Nand3_x1 ## Nand3_x1 6L, 6S 1L, 1S 6L, 6S Cell Nand3_x1 Summary (Clean) CELL COMPARISON RESULTS (TOP LEVEL) **************** CORRECT LAYOUT CELL NAME: SOURCE CELL NAME: Nand3_x1 Nand3_x1 INITIAL NUMBERS OF OBJECTS Layout Component Type Ports: 8 Nets: 8 3 --6 MN (4 pins) MP (4 pins) 3 --6 Instances: Total Inst: NUMBERS OF OBJECTS AFTER TRANSFORMATION Source -----6 Component Type Layout 6 Ports: Nets: 6 6





😃 Comparison Results 🗴 🛂 Layout Cell / Type Source Cell Nets Instances Ports Nand4_x1 ## Nand4_x1 7L, 7S 1L, 1S 7L, 7S Cell Nand4_x1 Summary (Clean) CELL COMPARISON RESULTS (TOP LEVEL) ************** CORRECT **************** LAYOUT CELL NAME: SOURCE CELL NAME: Nand4_×1 Nand4_×1 INITIAL NUMBERS OF OBJECTS Source -----7 Layout -----7 Component Type Ports: Nets: 10 10 4 4 4 4 MN (4 pins) MP (4 pins) Instances: Total Inst: 8 NUMBERS OF OBJECTS AFTER TRANSFORMATION Layout Source Component Type 7 7 Ports: Nets: 7

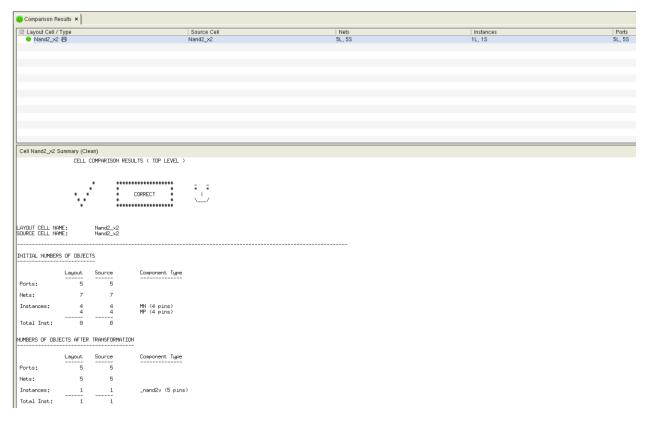
Nand2_x2



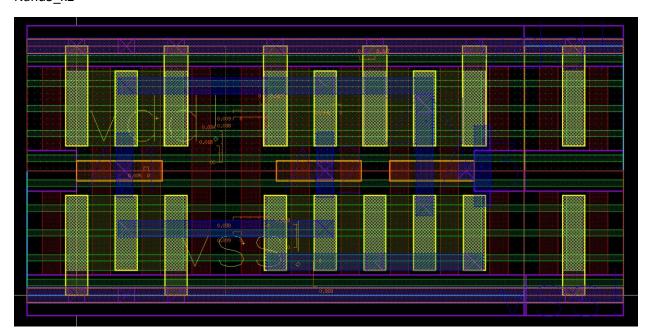
Check / Cell Results / Cell Cell	- Λ.		
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Check WELLS 2 Check WELLS 1 Check WELL GATE EX 2 Check WELL GATE EX 2 Check WELL GATE EX 1 Check WELL A 1B Check V9 WELL A 1B Check V9 WELL A 1A Check V9 WELL A 1A Check V9 WELL A 1A Check V9 WELL A 1B Check V9 S 2 Check V9 S 2 Check V9 S 3 Check V9 MELL 1 Check V9 WELL A 1B Check V8 WELL A 1B Check V7 WELL A 1B Check V8 WELL A 1B Che			
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✓ Check V6.M7.AUX.2 0 ✓ Check V6.M6.EN.1 0	1	Check V6.S.1	0
✓ Check V6.M6.EN.1 0	1	Check V6.M7.EN.2	0
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Rule File Pathname: /net/plato.ee.Virginia.ED			lo V

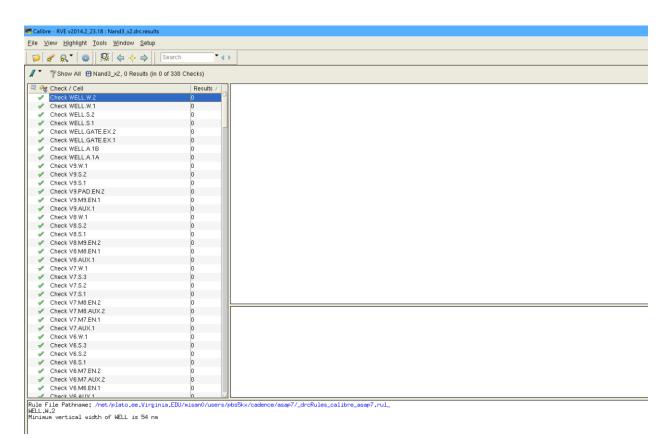
Rule File Pathname: /net/plato.ee.Virginia.EDU/misanO/users/pbs5kx/cadence/asap7/_drcRules_calibre_asap7.rul_ MELL.W.2

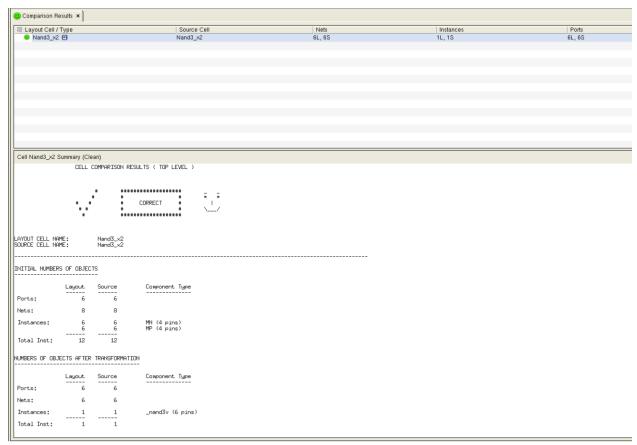
MELL.W.2 Minimum vertical width of WELL is 54 nm



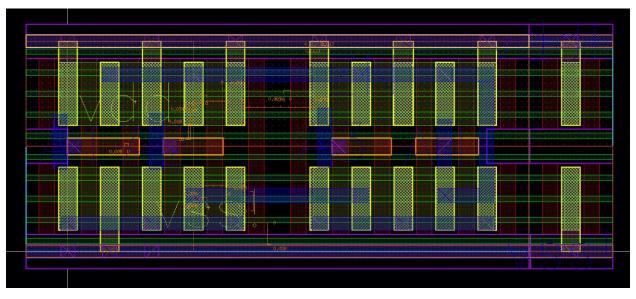
Nand3_x2

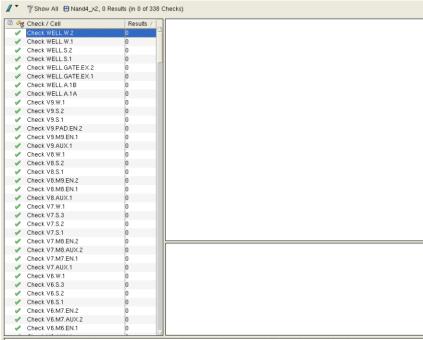






Nand4_x2





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