COMPUTER ARCHITECTURE & DESIGN

41 – REVIEW FOR TEST 3

TOPICS FROM TESTS 1 & 2

- Test 3 will not focus on topics that were tested by tests 1 and 2
- Test 3 may rely on and use topics that were tested by tests 1 and 2

MEMORY SYSTEMS

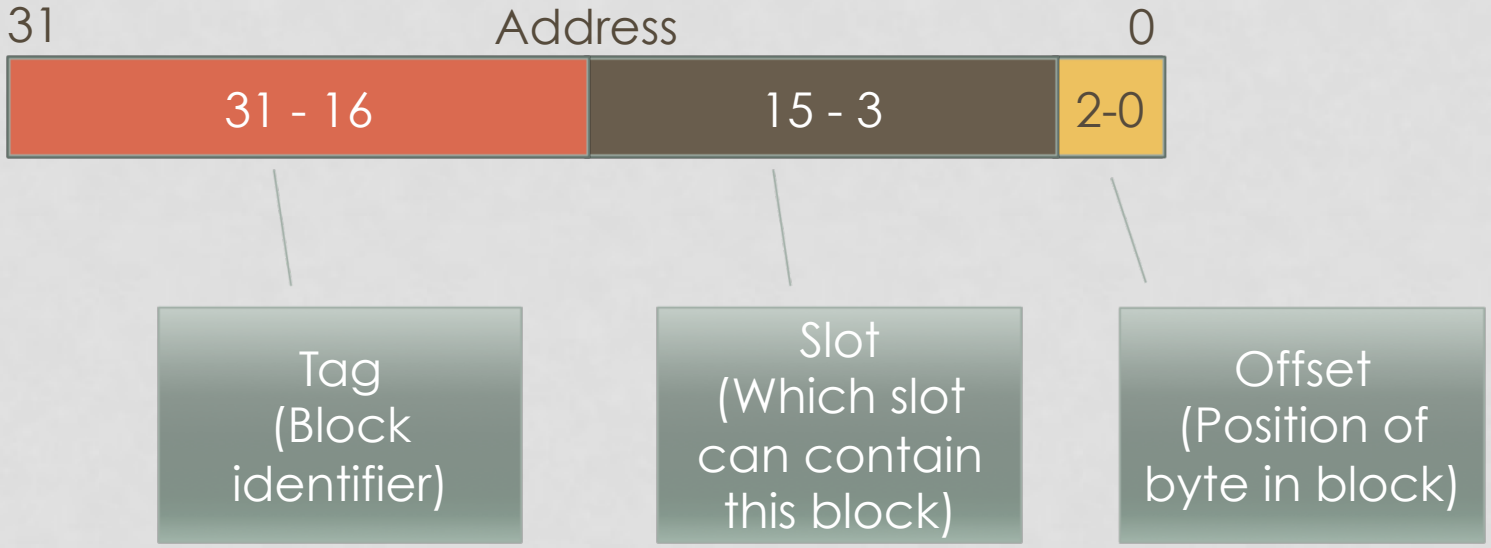
- Desired characteristic triad
- Memory hierarchy
- Locality of reference
  - Temporal
  - Spatial
- Average memory access time

CACHE QUESTIONS

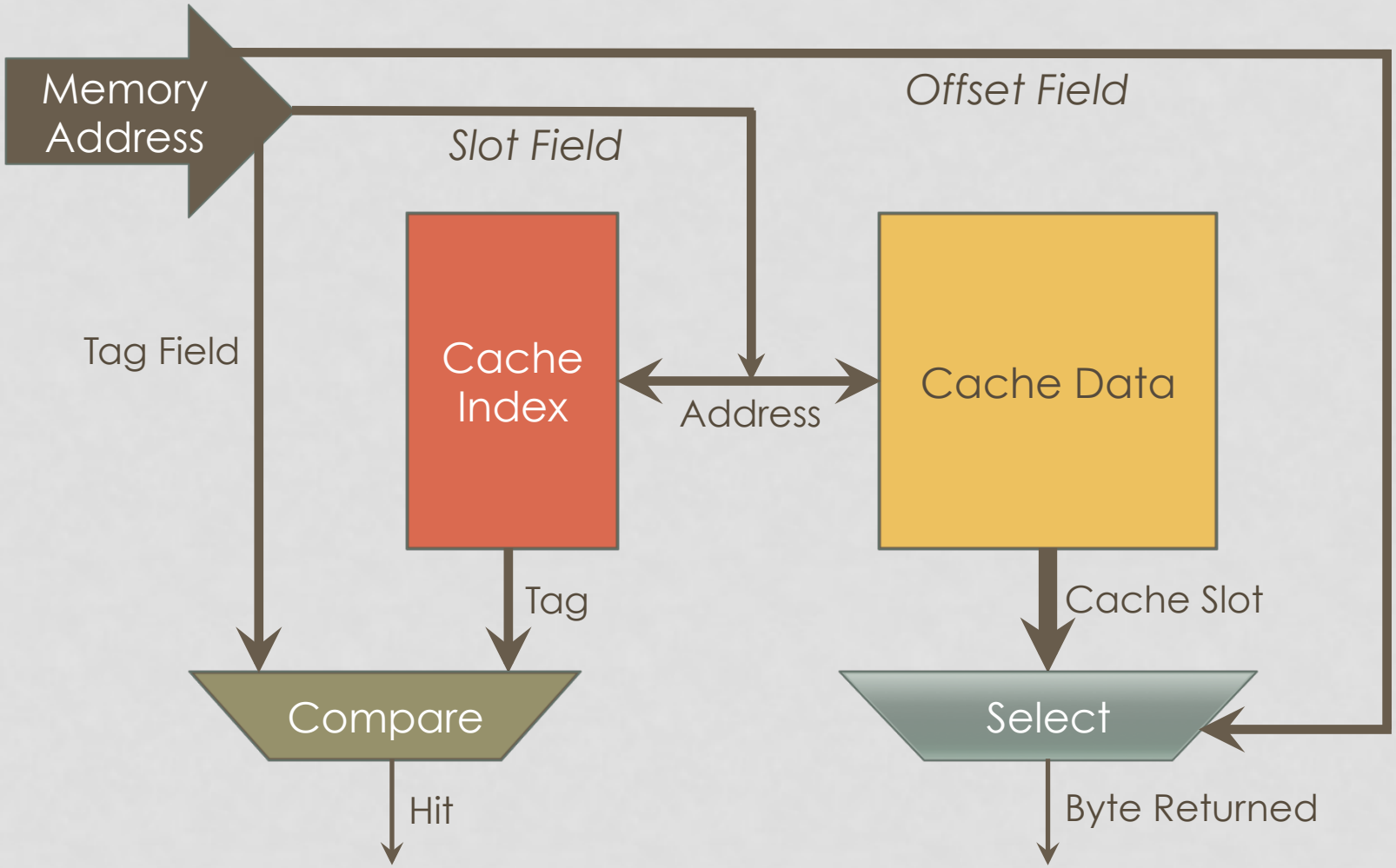
- Where should each data item be placed in the cache?
- How do we find the data in the cache?
- How do we replace the data in the cache?

CACHE MAPPING SCHEMES

- Direct mapped
- Fully associative
- Set associative
- Mapping blocks to slots: Tag-Slot-Offset



DIRECT MAPPED CACHE READ



CONTENT ADDRESSABLE MEMORY

- A limit to fully associative cache implementation
- What is CAM?
  - What is the problem with CAM?

CACHE OPERATIONS

- Read miss
- Writes
  - Write through
  - Write back
  - Write around

CACHE PERFORMANCE

- Elements of cache performance
  - Access time
  - Miss rate
  - Miss penalty
- Decreasing hit access time
- Causes for misses
  - Compulsory
  - Capacity
  - Conflict
- Cache design changes to decrease miss rate

DECREASING CACHE MISS PENALTY

- Adding cache layers
- Victim cache
- Wider memory access

VIRTUAL MEMORY

- Cache makes the memory system appear to be faster
- Virtual memory makes the memory system appear larger
- Virtual memory provides memory protection between programs

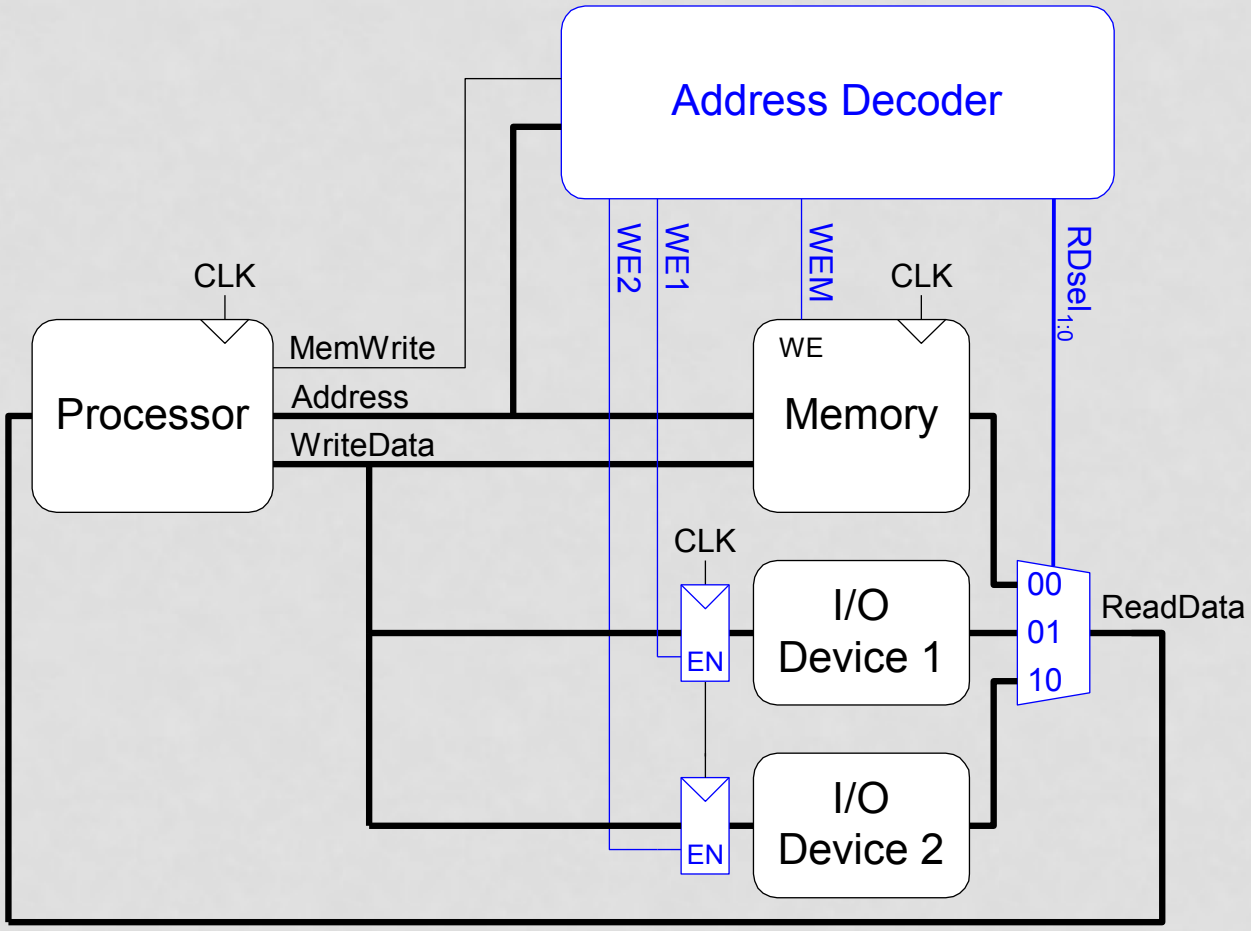
VIRTUAL ADDRESSES

- Virtual addresses are different from physical addresses
  - Each program has its own virtual address space
  - Entire virtual address space is stored on disk
  - A subset of virtual addresses is also in physical memory
- There is a mapping between virtual addresses and physical addresses
- Virtual to physical address translation is performed through the page table
  - The virtual page number serves as an index into the page table

PAGING THE PAGE TABLE

- The large page table may also be paged
- Virtual memory and paged page tables increase the number of memory accesses for each data transfer
- A translation look aside buffer (TLB) reduces these memory accesses

MEMORY MAPPED I/O



USB

- Objectives
- Tiered star topology
- Only the host or one device transmits at a time
- USB transactions are composed of packets
- Configuration sequence involves escalating information transfer

INCREASED INSTRUCTION LEVEL PARALLELISM

- Superscalar basics – parallel pipelines
  - Ideal performance
- Hazards with superscalar
  - Structural and the reservation station (ready stage)
  - Data hazards and register renaming
  - Control hazards and the difference between finishing and retiring

BRANCH PREDICTION

- Static – Dynamic
- Dynamic
  - Local history
  - Global history
  - Hybrid
  - Hysteresis
- Tournament predictor
- Branch target buffer

VLIW

- Very long instruction word processor
- Smaller, simpler, lower-power than Superscalar with comparable processing capability
- Complex compiler required to handle conflicts