Low-power MEMS tri-axial accelerometer digital output sensor

KEY FEATURE

- Three-axis accelerometer
- Supply voltage, 2.0V to 3.6V
- Programmable ±2g/±4g/±8g/±16g
- Power save modes
- HPF/LPF digital filter, interrupt mode
- Calibration possibility for offset and sensitivity
- 16bit ADC resolution
- SPI/I²C Digital interface
- Sleep to wakeup function
- Low power consumption
- Capable output data rate 25Hz to 3KHz
- Support Free fall function and Motion Detection function

Applications

- Black Box(Impact Recognition and logging)
- Shock detection
- Robot Vacuum
- Gaming Device
- Pedometer
- Display Orientation
- Digital cameras and camcorders
- Navigation devices
- Handheld devices

General description

The SGA100 is a low-power and high performance tri-axial, low-g accelerometer with digital SPI / I²C serial interface standard output, aiming for low-power consumer market applications

The Sensor allow measurement of accelerations in 3 perpendicular axes and thus senses tilt, motion, shock, and vibration handhelds, computer peripherals, Black Box and Robot vacuum.

The device features low-power operational modes that allow advanced power saving and smart sleep to wake-up functions.

The SGA100 has dynamically user selectable full scales of ±2g/±4g/±8g/±16g and it is capable of measuring accelerations with output data rates from 25Hz to 3KHz.

The SGA100 is available in small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

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List of Figures

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List of Tables

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1. Block Diagram and Pin Description

1.1. Block Diagram

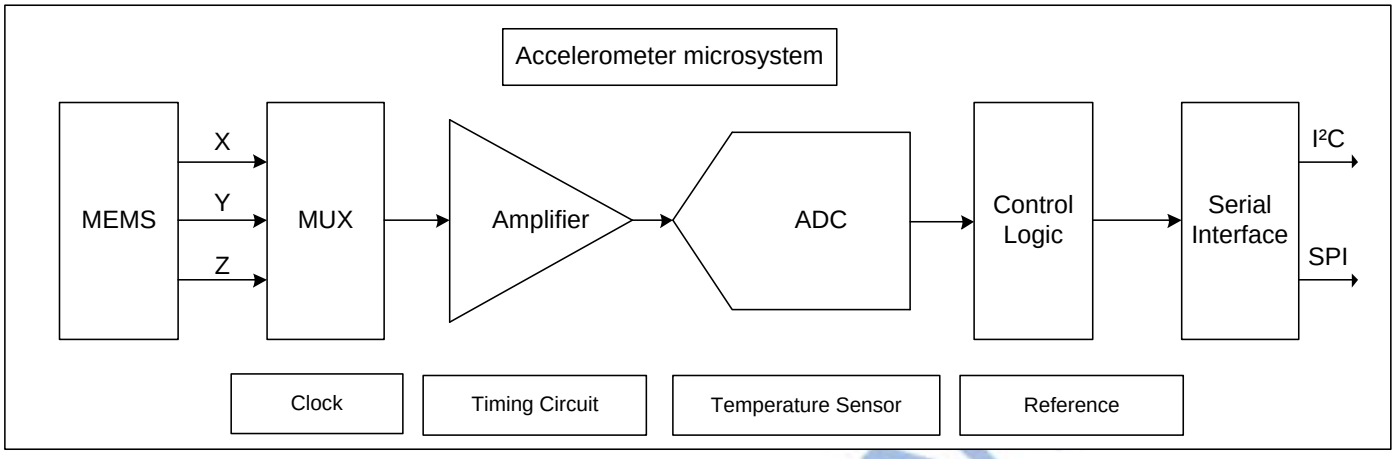

Figure 1. Block Diagram

1.2. Pin Connection And Description

1.2.1. Pin Connection

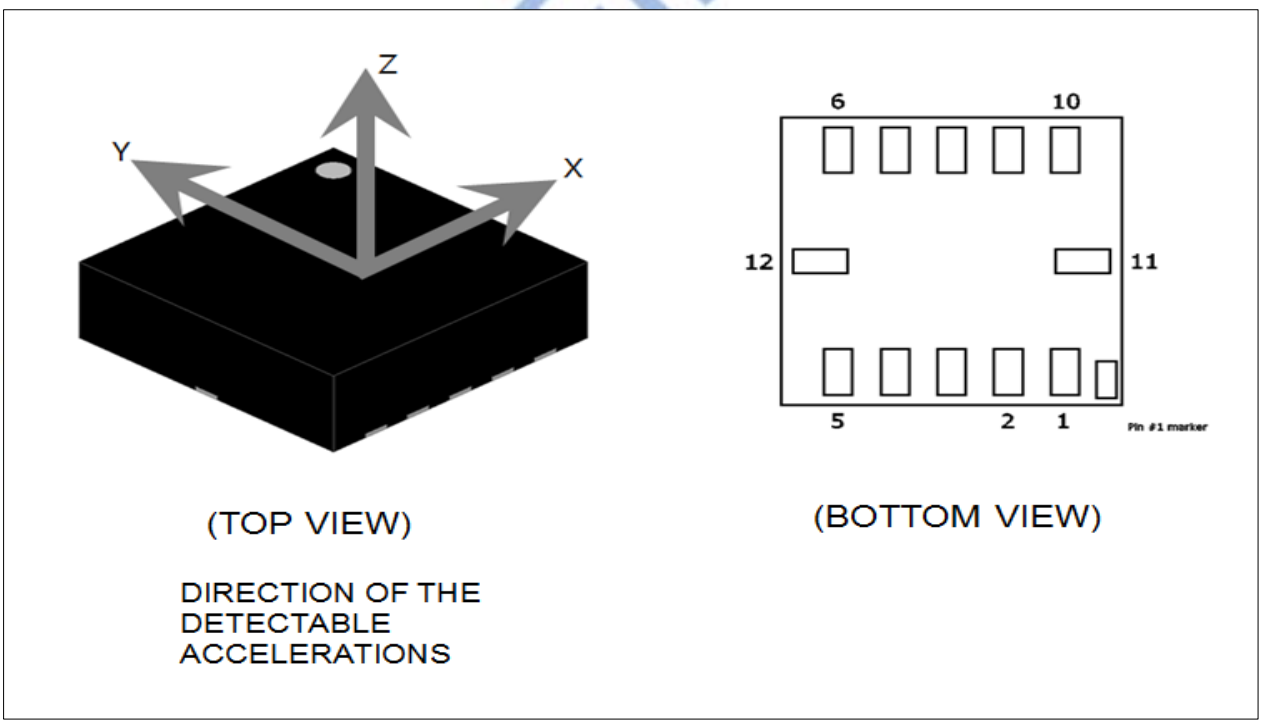

Figure 2. Pin Connection

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1.2.2. Pin Description

Table 1. Pin Description

Pin#	Pin Name		Description
1	Reserved		NC(Not Connected)
2	VDDA		Power supply 3.3V for Analog
3	GND		Analog ground
4	INT1		Interrupts
5	CS		I²C/SPI Mode Selection(1:I²C mode 0:SPI Enable)
6	SCK	SCL	I²C Serial Clock
		SPC	SPI Serial Port Clock
7	SDO	SDO	SPI Serial Data Output
8	SDI	SDA	I²C serial data access
		SDI	SPI Serial data Input
9	VDDIO		Power supply 3.3V for IO Pins
10	Reserved		NC(Not Connected)
11	Reserved		NC(Not Connected)
12	Reserved		NC(Not Connected)

The Recommended value: between GND and VDDA (VDDIO) a 22nF (100nF) capacitor should be connected.

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2. Device specifications

2.1. Mechanical characteristics

Typical specification is not guaranteed. VDDA=2.5v, T=25℃

Table 2. Mechanical characteristics

Symbol	Parameters	Conditions	Min	Typical	Max	Units
S	Sensitivity	FS 00(±2g)		16384		LSB/g
		FS 01(±4g)		8192		
		FS 10(±8g)		4096		
		FS 11(±16g)		2048		
FS	Acceleration Range	FS 00		±2		g
		FS 01		±4		
		FS 10		±8		
		FS 11		±16		
AO	Acceleration output resolution	2´s component			16	bit
TCS	Temperature Coefficient of Sensitivity	FS 00		0.02		%/ ºC
TCO	Temperature Coefficient of Offset	FS 00		±1		mg/ ºC
ZO	Zero-g offset accuracy	FS 00 T=25 ºC		±80		mg
ND	Noise density	FS 00 T=25 ºC ODR 50Hz		250		μg/√Hz
OT	Operating Temperature		-40		85	ºC
NL	Non Linearity	FS 00 T=25 ºC		±1		%FS
CS	Cross Axis Sensitivity	FS 00 T=25 ºC ODR 50Hz		2		%

- The product is factory calibrated at 2.5 V.
- The operational power supply range is from 2.0V to 3.6 V.

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2.2. Electrical characteristics

Typical specification is not guaranteed. VDDA=2.5v, T=25℃

Table 3. Electrical characteristics

Symbol	Parameters	Conditions	Min	Typical	Max	Units
VDD	Supply voltage		2.0	2.5	3.6	V
VDDIO	I/O pin supply Voltage		1.6	2.5	3.6	V
CCN	Current Consumption in Normal mode	T=25 ºC ODR 50hz		250		µA
CCL	Current Consumption in Low-power mode	Sleep=10Hz T=25 ºC ODR 1.6khz		11		µA
CCPD	Current Consumption in Power-down mode			1		µA
ODR	Output Data Rate In Normal mode	DR bit Set to 000		25		Hz
		DR bit Set to 001		50		
		DR bit Set to 010		100		
		DR bit Set to 011		200		
		DR bit Set to 100		400		
		DR bit Set to 101		780		
		DR bit Set to 110		1600		
		DR bit Set to 111		3000		
TOT	Turn On Time	ODR max		3		ms
WUT	Wake Up Time	From Low Power Mode , ODR 1.6Khz		1.5		ms
BW	System Bandwidth			ODR/2		Hz
OTR	Operating Temperature Range		-40		85	ºC
STS	Temperature Sensor Slope			0.5		ºC/LSB
OTS	Temperature Sensor Offset			±2		ºC

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2.3. Absolute Maximum ratings

Stresses above absolute maximum ratings may cause permanent damage to device. Exceeding the specified Characteristics may affect device reliability or cause mal-function.

Table 4. Absolute Maximum ratings

Symbol	Ratings	Maximum value	Units
VDD	Supply voltage	-0.3 to 4.25	V
VDDIO	I/O pin supply Voltage	-0.3 to 4.8	V
OTR	Operating Temperature Range	-40 to 85	℃
ESD	Electrostatic discharge protection(HBM)	2	KV
STG	Storage Temperature range	-50 to 150	℃
MS	Mechanical Shock (<1ms)	3000	g

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3. Digital Interfaces

The SGA100 provides two different digital interfaces the I²C and SPI Serial interface.
The registers may be accessed through both the I²C and SPI serial interfaces for reading and writing.
The serial interfaces are mapped onto the same pads. To select I²C interface, CS line must be tied high

3.1. SPI Interface

3.1.1. SPI Operation

The SPI Interface Uses 4-wires: SPC(Serial port Clock),SDI(serial data input),SDO(Serial data Output) and CS(chip select).
CS is controlled by the SPI Master. Multiple read out is Possible.
SPI Transmission starts when CS goes to low and stops when CS goes to high: CS is Active low.
When CS is Active low, Data on SDI is latched by SGA100 at SPC Rising edge and SDO is changed at SPC falling edge(SPI Mode3).

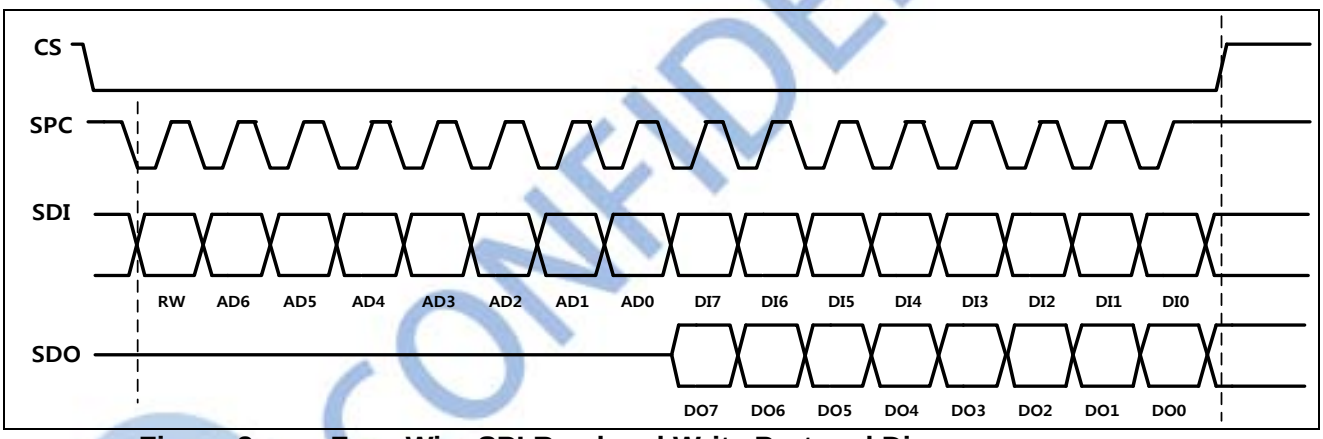

Figure 3. Four-Wire SPI Read and Write Protocol Diagram

Bit Definitions:

RW: SPI read and write mode significant bit flag. When RW is 0, the data(DI7-DI0) is written into the device.
When RW is 1, the data(DO7-DO0) is read from the device.
AD6-AD0: The address(7bit) of the device register.
DI7-DI0: The data(8bit) is written into the device.
DO7-DO0: The data(8bit) is read from the device.

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3.1.2. SPI Write

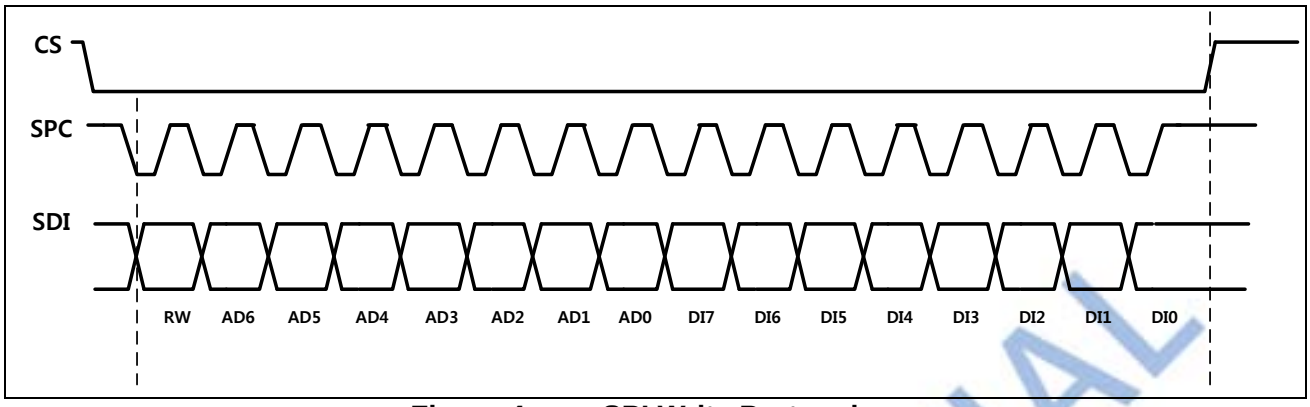

Figure 4. SPI Write Protocol

Bit Definitions:

RW: SPI write mode bit flag. The Value is 0

AD(6-0): The address of the device register.

DI(7-0): The data is written into the device.(MSB first)

The SPI Write command is performed with 16 clock pulses through SDI line as long as CS stays active low. When write is required, two sequential bytes are necessary: one control byte to define the address to be written and the one data byte.

Table 5. SPI Single Write Operation

Start	RW	Address1(0x11)							Write Data(0xAA)								Stop
CS=0	0	0	0	1	0	0	0	1	1	0	1	0	1	0	1	0	CS=1

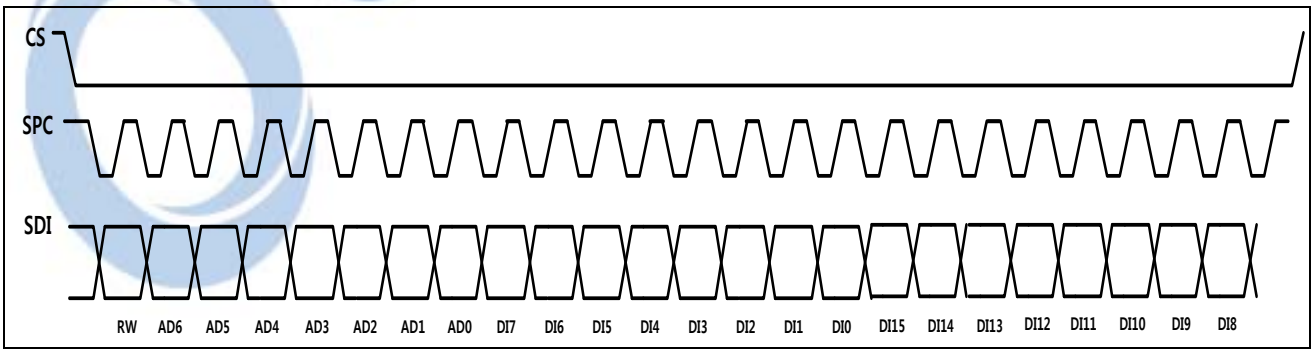

Figure 5. SPI Multiple write protocol Diagram

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Bit Definitions:

RW: SPI Write mode bit flag. The Value is 0

AD(6-0): The address of the device register.

DI(7-0): The data is written into the device.(MSB first)

DI(15-8): Further data in multiple byte writing.(MSB first)

The SPI Multiple write mode also supported. After each byte of data is received, the register address is internally incremented by one.

If a lot of data are transmitted and the highest address reached, the address will roll over to lowest address and the previously written data will be overwritten.

Table 6. SPI Multiple Write Operation

Start	RW	Address1(0x11)								Address(0x11)-Write Data(0xAA)								Address(0x12)-Write Data(0xA1)								stop
CS=0	0	0	0	1	0	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	1	CS=1

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3.1.3. SPI Read

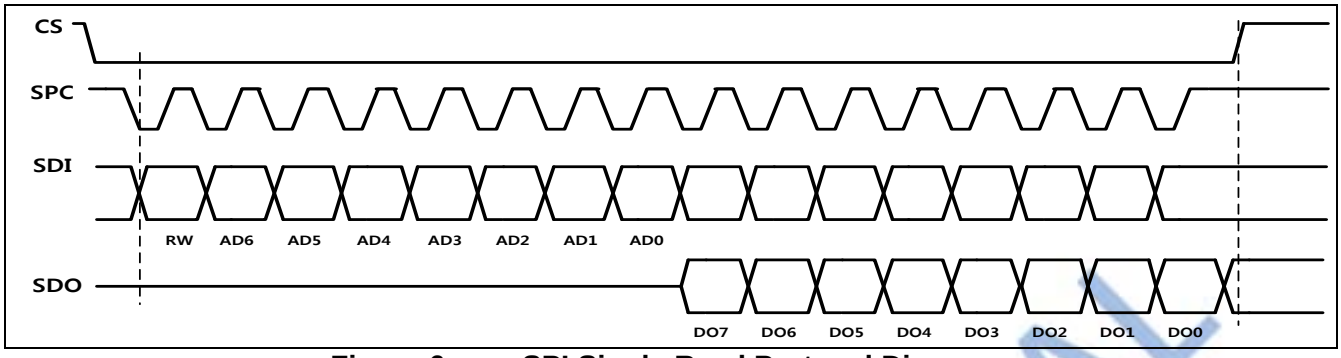

Figure 6. SPI Single Read Protocol Diagram

Bit Definitions:

RW: SPI Read mode bit flag. The Value is 1

AD(6-0): The address of the device register.

DO (7-0): The data is read from the device. (MSB first)

The SPI Read command is performed with 16 clock pulses through SDI and SDO line as long as CS stays active low.

When Read access is required ,one control byte to define the address to be read followed by data byte.

Table 7. SPI Single Read Operation

Start	RW	Address1(0x11)							Read Data(0x1A)								Stop
CS=0	1	0	0	1	0	0	0	1	0	0	0	1	1	0	1	0	CS=1

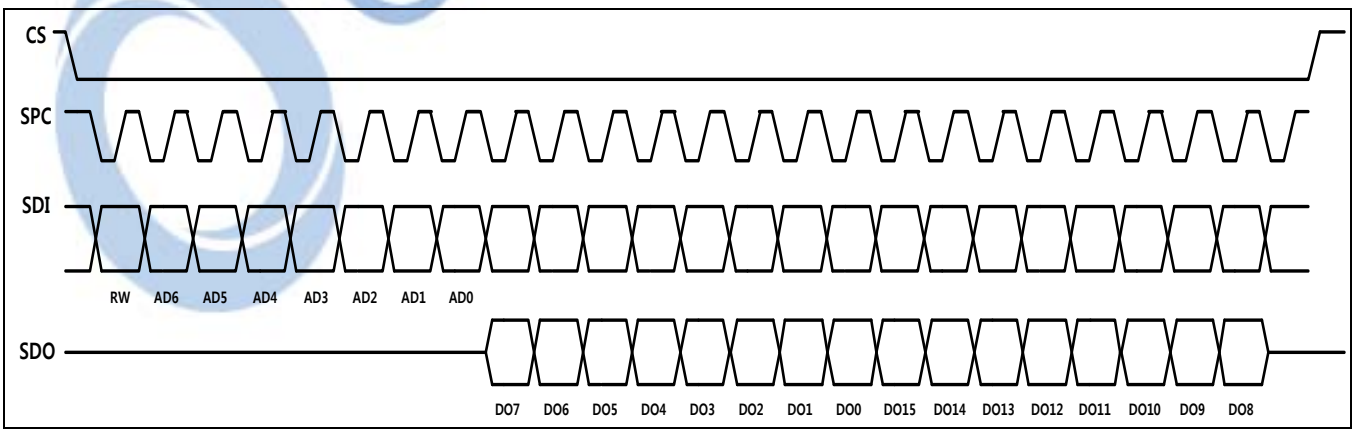

Figure 7. SPI Multiple Read Protocol Diagram

Bit Definitions:

RW: SPI Read mode bit flag. The Value is 1

AD(6-0): The address of the device register.

DO(7-0): The data is read from the device.(MSB first)

DO(15-8): Further data in multiple byte reading.(MSB first)

Addresses are automatically incremented as long as CS stays active low**.** If the highest address reached, the address will roll over to lowest address**.**

Table 8. SPI Multiple Read Operation

Start	RW	Address1 (0x11)							Address1(0x11)-Read Data(0x1A)								Address2(0x12)-Read Data(0x12)								Stop
CS=0	1	0	0	1	0	0	0	1	0	0	0	1	1	0	1	0	0	0	0	1	0	0	1	0	CS=1

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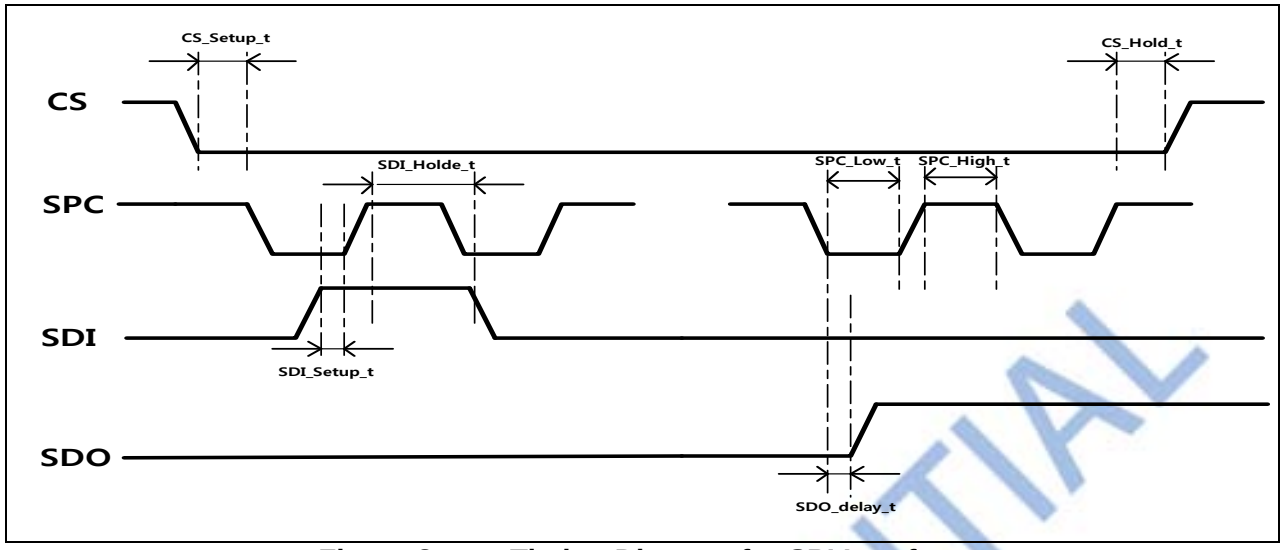

Figure 8. Timing Diagram for SPI Interface

Table 9. SPI Timings

Parameter	Symbols	Conditions	Min	Typical	Max	Unit
SPC Clock frequency	SCF				10	MHz
SPC Low Clock Time	SPC_Low_t		20			ns
SPC High Clock Time	SPC_High_t		20			ns
SDI Setup Time	SDI_Setup_t		20			ns
SDI Hold Time	SDI_Hold_t		20			ns
CS Setup Time	CS_Setup_t		20			ns
CS Hold Time	CS_Hold_t		40			ns
SDO Delay time	SDO_Delay_t				30	ns

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3.2. I²C Interface

The SGA100 I²C is a bus slave.

I²C Write Address of SGA100 is 11001000(0xC8), Read Address is 11001001(0xC9)

Only two bus lines are required; a serial data line (SDA) and a serial clock line (SPC).

Both lines are connected to VDDIO external via pull-up resistors. When the bus is free, both the lines are high.

CSB is not used and must be connected to VDDIO.

These signals make it possible to support serial transmission of 8-bit bytes of data and 7-bit device addresses.

Data on the I2C-bus can be transferred at rates of up to 100kbit/s in the Standard-mode, up to 400kbit/s.

The I2C master is the CPU or microcontroller in the system.

Some microcontrollers even feature hardware to implement the I²C protocol.

You can also build an all-software implementation using a pair of general-purpose I/O pins.

3.2.1. I²C Operation

- START and STOP Condition

START and STOP conditions are always generated by the master

All Transactions begin with START and are terminated by a STOP.

The Data Transfer on the bus Begins through a START signal.

Each data transfer must be terminated by the generation of a STOP condition.

A START condition is defined as a HIGH to LOW (falling edge) transition on SDA (SDI) while SPC is HIGH.

Stop Condition is LOW to HIGH (rising edge) transition on the SDA (SDI) while SPC is HIGH.

The START and repeated START conditions are functionally identical

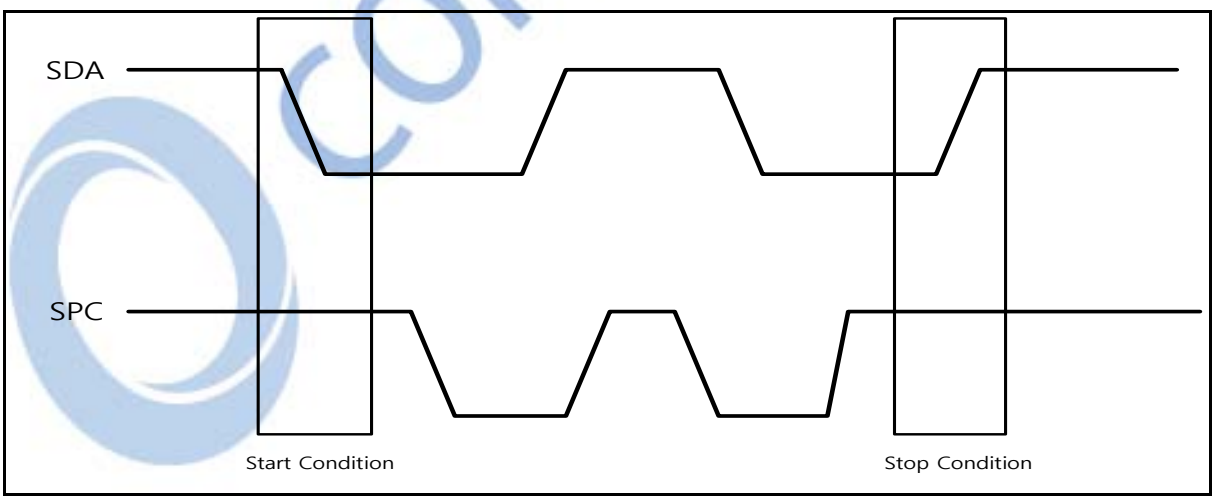

Figure 9. I²C Start and Stop Timing diagram

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■ Data Transfer

One clock pulse(SPC) is generated for each data bit transferred.

The data on the SDA line must be stable during the HIGH period of the Serial port clock (SPC).

The HIGH or LOW state of the data line can only change when the clock signal on the SPC line is LOW.

Data is transferred with the Most Significant Bit (MSB) first.

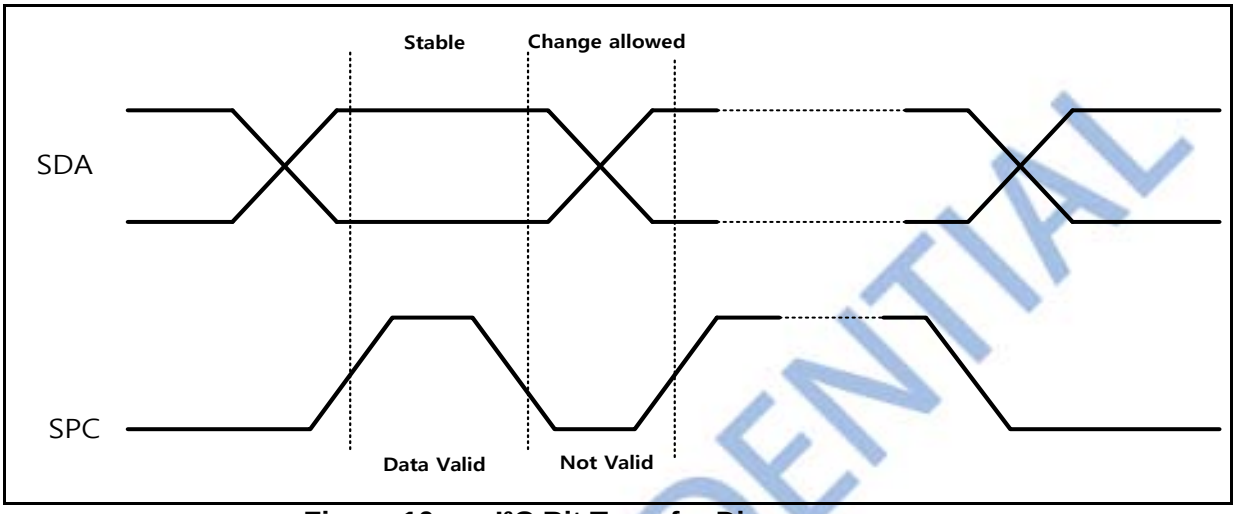

Figure 10. I²C Bit Transfer Diagram

■ Acknowledge& Not Acknowledge

The acknowledge takes place after every bytes.

The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received And another byte may be sent.

The master generates all clock pulses, including the Acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA Line LOW and it remains stable LOW during the HIGH period of this clock pulse. (Acknowledge signal)

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal

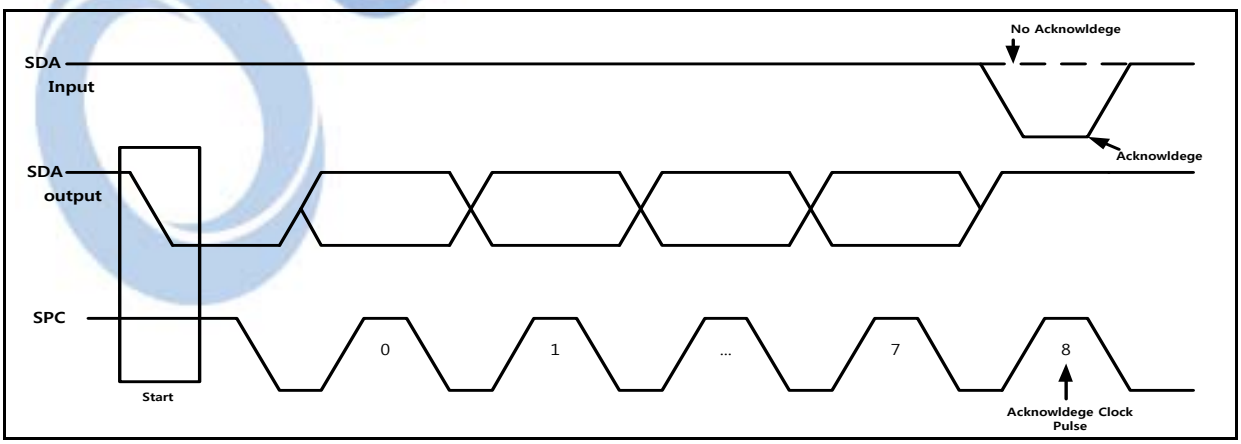

Figure 11. I²C Acknowledgement on SDA

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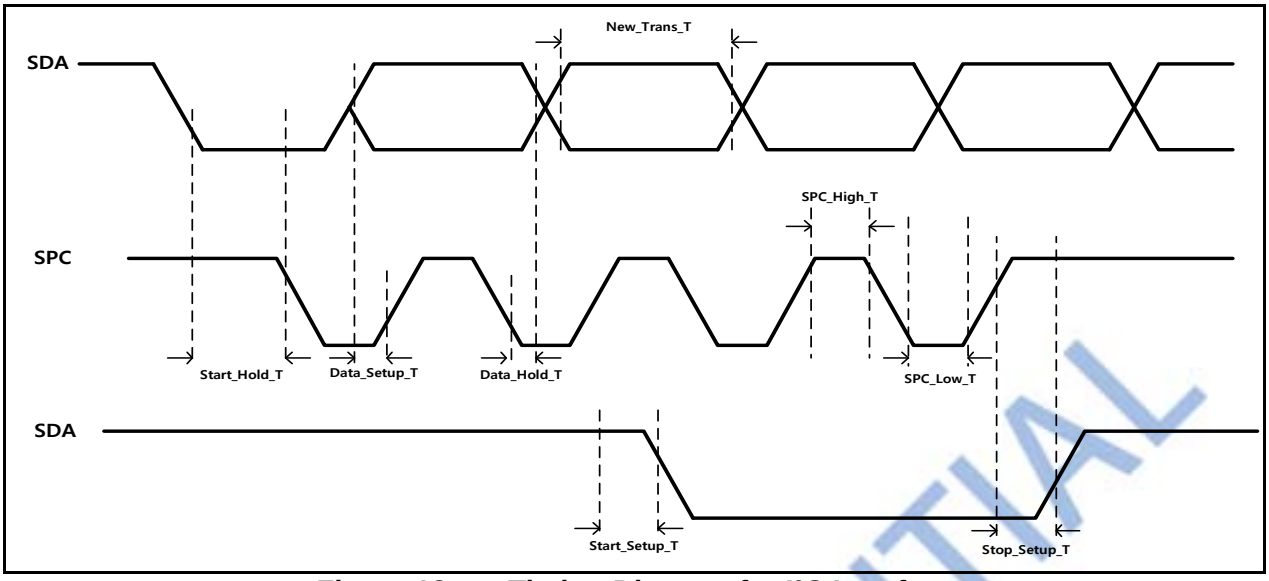

Figure 12. Timing Diagram for I²C Interface

Table 10. I²C Timings

Parameter	Symbols	Con	Min	Typical	Max	Unit
SPC Clock Frequency	ICF			400		KHz
Start Setup Time	Start_Setup_T		160			ns
Start Hold Time	Start_Hold_T		160			ns
Stop Setup Time	Stop_Setup_T		160			ns
SDA Setup Time	Data_Setup_T		10			ns
SDA Hold Time	Data_Hold_T		10		70	ns
SPC High Time	SPC_Hight_T		60			ns
SPC Low Time	SPC_Low_T		160			ns
New Data Transmit enable time	New_Trans_T		100			ns

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3.2.2. I²C Write

After the START condition , a slave address is sent.
This address is seven bits long followed by an eighth bit which is a data direction bit (R/W):
a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ)
Master-transmitter transmits to slave-receiver. The transfer direction is not changed
The slave receiver acknowledges each byte.
A data transfer is always terminated by a STOP condition generated by the master.

Table 11. I²C Single Write Operation

Device	Conditions							
Master	START	Slave Address+ W(0)		Register Address		Data		STOP
Salve			Ack		Ack		Ack	

After a start condition, a slave address(7bit) + W(zero) must be send.
If the slave acknowledge (ACK) has been returned, and then Data transfer is enabled.
The Master Transmitter is send to slave receiver one byte (register address): the 7 LSB represent
The actual register address and one dummy bit.

After Register address slave acknowledge (ACK), the Master is send to the slave receiver
one byte (register data).
It will be written to the register.

The I2C Multiple write mode also supported. After each byte of data is received, the register address is internally incremented by one. If a lot of data are transmitted and the highest address reached, the address will roll over to lowest address and the previously written data will be overwritten.

Table 12. I²C Multiple Write Operation

Device	Conditions									
Master	START	Slave Address+W(0)		Register Address		Data		Data		STOP
Salve			Ack		Ack		Ack		Ack	

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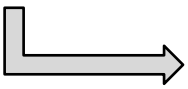
3.2.3. I²C Read

A data transfer is always terminated by a STOP condition generated by the master.
However, if a master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Table 13. I²C Single Read Operation

Device	Conditions							
Master	START	Slave Address+W(0)		Register Address		Repeated Start	Slave Address+R(1)	
Salve			Ack		Ack			Ack

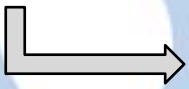


Conditions		
	No Ack	STOP
Data		

After a start condition, a slave address(7bit) + W(zero) must be send.
If the slave acknowledge (ACK) has been returned, and then Data transfer is enabled.
Master reads slave(SLAVE+R) immediately after first byte(Repeated START).
At the moment of the first acknowledge, the master-transmitter becomes a master-receiver and the slave-receiver becomes a slave-transmitter.
This first acknowledge is still generated by the slave.
The master generates subsequent acknowledges.
The STOP condition is generated by the master, which send a not-acknowledge just before the STOP condition.

Table 14. I²C Multiple Read Operation

Device	Conditions							
Master	START	Slave Address+W(0)		Register Address		Repeated Start	Slave Address+R(1)	
Salve			Ack		Ack			Ack



Conditions						
	Master Ack		Master Ack		No Ack	STOP
Data		Data		Data		

After Repeated START and slave address+ R (one) acknowledge, address is automatically incremented.
If Master is Read data from SDA Line and Send Master Acknowledge to the slave, then slave automatically send to next register address data On SDA Line.

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4. Register Map

4.1. List of the Registers

The table given below provides a listing of the 8 bit registers embedded in the device and the related address.

Table 15.Register Address Map

Address	Name	Description	Type	Default
01h	DEV_ID	Device ID	R	0xA1
02h	STATUS	Device Status	R	-
03h	CTRL_REG1	Control Register 1	RW	0x61
04h	CTRL_REG2	Control Register 2	RW	0xFC
05h	CTRL_REG3	Control Register 3	RW	0x1A
06h~0Fh	-	Reserved	-	-
10h	INT1_CTRL	Interrupt 1 Control	RW	0x1A
11h	INT1_MAP_FUNC	Interrupt1 Function Mapping	RW	0x00
12h	OUT_DATA_XL	Low Bytes of X- Axis Acceleration Data	R	-
13h	OUT_DATA_XH	High Bytes of X- Axis Acceleration Data	R	-
14h	OUT_DATA_YL	Low Bytes of Y- Axis Acceleration Data	R	-
15h	OUT_DATA_YH	High Bytes of Y- Axis Acceleration Data	R	-
16h	OUT_DATA_ZL	Low Bytes of Z- Axis Acceleration Data	R	-
17h	OUT_DATA_ZH	High Bytes of Z- Axis Acceleration Data	R	-
18h	OUT_DATA_TEMP	8bit Temperature Data	R	-
19h	USR_GAIN _X_CTRL	User set gain on X-axis(x0-x2).	RW	0x80
1Ah	USR_GAIN _Y_CTRL	User set gain on Y-axis(x0-x2).	RW	0x80
1Bh	USR_GAIN _Z_CTRL	User set gain on Z-axis(x0-x2).	RW	0x80
1Ch	USR _OFS_X_CTRL	User set offset on X-axis.(x64)	RW	0x00
1Dh	USR _OFS_Y_CTRL	User set offset on Y-axis.(x64)	RW	0x00
1Eh	USR _OFS_Z_CTRL	User set offset on Z-axis. (x64)	RW	0x00
1Fh~22h		Reserved		

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23h	DIGITAL_FILTER_CTRL	Digital filter control	RW	0x00
24h	INT_FUNC_CTRL1	FIFO/NDR Interrupt Control	RW	0x00
25h	INT_FUNC_CTRL2	Motion Interrupt Control	RW	0x80
26h		Reserved		
27h	FIFO_CTRL	FIFO Control	RW	0x00
28h	FIFO_DATA_STATUS	FIFO Stored level status	R	-
29h	INT_FUNC_CTRL1_STATUS	FIFO /NDR Interrupt Status	R	-
2Ah	MOTION_CTRL	Motion Detection Mode Control	RW	0x01
2Bh	MOTION_STATUS	Motion Interrupt status	R	-
2Ch	MOTION_HIGH_TH	High Event Threshold	RW	0xBE
2Dh	MOTION_HIGH_DUR	High Event Duration	RW	0x02
2Eh	MOTION_LOW_TH	Low Event Threshold	RW	0x2D
2Fh	MOTION_LOW_DUR	Low Event Duration	RW	0x02
30h~71h		Reserved		

Registers marked as ***Reserved*** must not be changed. The Writing to those Register may cause Operation Fail and Damage to the device

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5. RegisterDescription

5.1. DEV_ID (01h)

This register contains the device identifier.

7							0
ID[7:0]							

DEV_ID Register(R/O)

Initial value: 0xA1

Name	Description
ID [7:0]	Device identifier Of SGA100

5.2. STATUS Register (02h)

This register shows device operating status flag. It is set when the associated events are occurred.

7	5	4	3	2	1	0
Reserved	SWRD	NDR_Z	NDR_Y	NDR_X	WKUPD	INITD

STATUS Register(R/O)

Initial value: -

Name	Description
SWRD	Status of Soft Reset. Default: 0 0:None 1:Soft Reset Done
NDR_Z	New data Ready for Z axis. Default: 0 0: Not Ready 1: New data available for Z Axis
NDR_Y	New data Ready for Y axis. Default: 0 0: Not Ready 1: New data available for Y Axis
NDR_X	New data Ready for X axis. Default: 0 0: Not Ready 1: New data available for X Axis
WKUPD	Status of sleep to Wakeup. Default: 0 0: No Wake Up 1:Sleep to Wakeup done

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INITD	Status of Initialization. Default: 0 0: No Init 1: Auto Init done

5.3. CTRL_REG1 Register (03h)

This register controls main power modes and output data rates. In addition, specifies low power sleep period

7	6	5 ~ 3	2 ~ 0
Power_Down	PM	Sleep_Dur	ODR

CTRL_REG1 Register(R/W)

Initial value: 0x61

Name	Description
ODR[2:0]	Output data rate Selection In Normal Power Mode. Default: 001 000: ODR =25 Hz 001: ODR =50 Hz 010: ODR =100 Hz 011: ODR =200 Hz 100: ODR =400 Hz 101: ODR =780 Hz 110: ODR =1600hz 111: ODR =3000hz (Bypass LPF)
Sleep_Dur[5:3]	Configuration of sleep duration for low power mode. Default: 100. 000: Sleep Duration 2s 001: Sleep Duration 1s 010: Sleep Duration 500ms 011: Sleep Duration 100ms 100: Sleep Duration 50ms 101: Sleep Duration 25ms 110: Sleep Duration 10ms 111: Sleep Duration 5ms

PM	Configuration of Main power modes. Default: 1. 0: Low Power Mode 1: Normal Mode
Power_Down	Controls device power down. Default: 0 0: Disable 1: Enable

5.4. CTRL_REG2 Register (04h)

This Register enable/disables acceleration of each sensor axis, controls accelerometer full scale range and user offset sign value.

7	6	5	4	3	2	1	0
ZEN	YEN	XEN	ZOS	YOS	XOS	FS	

CTRL_REG2 Register(R/W)

Initial value: 0xFC

Name	Description
ZEN	Z-Axis Enable. Default: 1 1: Enabled. 0: Disabled
YEN	Y-Axis Enable. Default: 1 1: Enabled. 0: Disabled
XEN	X-Axis Enable. Default: 1 1: Enabled. 0: Disabled
ZOS	Controls user z-axis offset sign value. Default: 1 1: Positive Direction 0: Negative Direction

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YOS	Controls user y-axis offset sign value. Default: 1 1: Positive Direction 0: Negative Direction
XOS	Controls user x-axis offset sign value. Default: 1 1: Positive Direction 0: Negative Direction
FS	Full Scale Selection. Default: 00 00- 2g 01- 4g 10- 8g 11- 16g

5.5. CTRL_REG3 Register (05h)

This register controls soft reset of the sensor, data sync, and configuration of the sleep to wake up mode for low power mode.

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	reserved	SOFT_RST	Reserved	SWM

CTRL_REG3 Register(R/W)

Initial value: 0x1A

Name	Description
SOFT_RST	All user configuration settings are overwritten with the setting stored in ROM. Default : 0 1: Reset 0: No Reset
SWM	Selection for sleep to wake up mode. Default: 0 1: Enabled 0: Disabled

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5.6. INT1_CTRL Register (10h)

This register controls the behavior of the Interrupt pin1.

7	6	5	4	3	2	1	0
reserved	reserved	reserved	INT1_ACTIVE_LEVEL	INT1_PP_SELECT	reserved	INT1_MODE	INT1_RST

INT1_CTRL Register(R/W)

Initial value: 0x1A

Name	Description
INT1_ACTIVE_LEVEL	Active high/low level for Interrupt pin1. Default: 1 1: Active high 0: Active low
INT1_PP_SELECT	Push- Pull / Open drain selection on Interrupt pin1. Default: 1 1: Push-Pull 0: Open drain.
INT1_MODE	Interrupt1 mode selection. Default: 1 1: Interrupt not latched. 0: Interrupt latched.
INT1_RST	Interrupt 1 reset (Clear any latched interrupt). default: 0 1:Reset 0:None

5.7. INT1_MAP_FUNC Register (11h)

This register controls which interrupt signals are the mapped to the interrupt pin1.

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	MAP_FIFO	MAP_MOTION	Reserved	MAP_DRDY

INT1_MAP_FUNC Register(R/W)

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Initial value: 0x00

Name	Description
MAP_FIFO	Map FIFO interrupt to interrupt1 pin. Default: 0 1:Enable 0:Disable
MAP_MOTION	Map motion Interrupt to interrupt1 pin. Default: 0 1:Enable 0:Disable
MAP_DRDY	Map new data ready Interrupt to interrupt1 pin. Default: 0 1: Enable 0: Disable

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5.8. OUT_DATA_XL Register (12h)

X-Axis acceleration data is stored this register. This register is a read only.

7							0
XL[7:0]							

OUT_DATA_XL Register(R/O)

Initial value: -

Name	Description
XL[7:0]	X- Axis acceleration data. The value is expressed in two's complement with 8bit Low Byte

5.9. OUT_DATA_XH Register (13h)

X-Axis acceleration data is stored this register. This register is a read only.

7							0
XH[15:8]							

OUT_DATA_XH Register(R/O)

Initial value: -

Name	Description
XH[15:8]	X- Axis acceleration data. The value is expressed in two's complement with 8bit High Byte

5.10. OUT_DATA_YL Register (14h)

Y-Axis acceleration data is stored this register. This register is a read only.

7							0
YL[7:0]							

OUT_DATA_YL Register(R/O)

Initial value: -

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YL[7:0]	Y- Axis acceleration data. The value is expressed in two's complement with 8bit Low Byte

5.11. OUT_DATA_YH Register (15h)

Y-Axis acceleration data is stored this register. This register is a read only.

7							0
YH[15:8]							

OUT_DATA_YH Register(R/O)

Initial value: -

Name	Description
YH[15:8]	Y- Axis acceleration data. The value is expressed in two's complement with 8bit High Byte

5.12. OUT_DATA_ZL Register (16h)

Z-Axis Acceleration data is stored this register. This register is a read only.

7							0
ZL[7:0]							

OUT_DATA_ZL Register(R/O)

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Initial value: -

Name	Description
ZL[7:0]	Z- Axis acceleration data. The value is expressed in two's complement with 8bit Low Byte

5.13. OUT_DATA_ZH Register (17h)

Z-Axis acceleration data is stored this register. This register is a read only.

7							0
ZH[15:8]							

OUT_DATA_ZH Register(R/O)

Initial value: -

Name	Description
ZH[15:8]	Z- Axis acceleration data. The value is expressed in two's complement with 8bit High Byte

5.14. OUT_DATA_TEMP Register (18h)

Temperature data is stored this register. This register is a read only.
Readout value of TEMP[7:0]=0x0 corresponds to a temperature of 23ºC.

7							0
TEMP[7:0]							

OUT_DATA_TEMP Register(R/O)

Initial value: -

Name	Description
TEMP[7:0]	8bit Temperature data. The value is expressed in two's complement. Default: 0x0

5.15. USR_GAIN_X_CTRL Register (19h)

This register controls user sensitivity compensation for X-Axis acceleration value.
Gain value is represented with mapping of 0x0->x0.0, 0xff->x1.99.

.

7							0
GAIN_X[7:0]							

USR_GAIN_X_CTRL Register(R/W)

Initial value: 0x80

Name	Description
GAIN_X[7:0]	Gain values for sensitivity trimming of X-Axis. The value is expressed in unsigned format. Total gain range:x0~x2 Default: 0x80 (x1)

5.16. USR_GAIN_Y_CTRL Register (1Ah)

This register controls user sensitivity compensation for Y-Axis acceleration value.
Gain value is represented with mapping of 0x0->x0.0, 0xff->x1.99.

7							0
GAIN_Y[7:0]							

USR_GAIN_Y_CTRL Register(R/W)

Initial value: 0x80

Name	Description
GAIN_Y[7:0]	Gain values for sensitivity trimming of Y-Axis. The value is expressed in unsigned format. Total gain range:x0~x2 Default: 0x80 (x1)

5.17. USR_GAIN_Z_CTRL Register (1Bh)

This register controls user sensitivity compensation for Z-Axis acceleration value.

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Gain value is represented with mapping of 0x0= x0.0, 0xff= x1.99.

7							0
GAIN_Z[7:0]							

USER_GAIN_CTRL_Z Register(R/W)

Initial value: 0x80

Name	Description
GAIN_Z[7:0]	Gain values for sensitivity trimming of Z-Axis. The value is expressed in unsigned format. Total gain range:x0~x2 Default: 0x80 (x1)

5.18. USR_OFS_X_CTRL Register (1Ch)

This register user offset compensation for X-Axis acceleration value.
Offset value is represented with mapping of 0x0= ±0 count, 0xff= ±16320 count.

7							0
OFS_X[7:0]							

USR_OFS_X_CTRL Register(R/W)

Initial value: 0x00

Name	Description
OFS_X[7:0]	Offset values for offset trimming of X-Axis. The value is expressed in unsigned format. Scale Factor:x64 Default : 0

5.19. USR_OFS_Y_CTRL Register (1Dh)

This register user offset compensation for Y-Axis acceleration value.

Offset value is represented with mapping of 0x0= ±0 count, 0xff= ±16320 count.

7							0
OFS_Y[7:0]							

USR_OFS_Y_CTRL Register(R/W)

Initial value: 0x00

Name	Description
OFS_Y[7:0]	Offset values for offset trimming of Y-Axis. The value is expressed in unsigned format. Scale Factor:x64 Default : 0

5.20. USR_OFS_Z_CTRL Register (1Eh)

This register user offset compensation for Z-Axis acceleration value.
Offset value is represented with mapping of 0x0= ±0 count, 0xff= ±16320 count.

7							0
OFS_Z[7:0]							

USR_OFS_Z_CTRL Register(R/W)

Initial value: 0x00

Name	Description
OFS_Z[7:0]	Offset values for offset trimming of Z-Axis. The value is expressed in unsigned format. Scale Factor:x64 Default : 0

5.21. DIGITAL_FILTER_CTRL Register (23h)

This register controls high-pass filter cut-off frequency and input source data selection.

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7	6	5	4	3	2	1	0
reserved	reserved	reserved	HPF_RST	INT_SRC	OUTPUT_SRC	HPF_FREQ	

DIGITAL _FILTER_CTRL Register(R/W)

Initial value: 0x00

Name	Description
HPF_RST	High pass filter reset. Default:0 1: Reset 0: None
INT_SRC	Interrupt1 data source selection. Default: 0 0: Low Pass Filter Data 1: High Pass Filter Data
OUTPUT_SRC	Output data source selection. Default: 0 0: Low Pass Filter Data 1: High Pass Filter Data
HPF_FREQ[1:0]	High pass filter cut-off frequency Configuration. Default: 0 When ODR=3Khz. 00: 64hz 01: 32hz 10: 16hz 11: 8hz

5.22. INT_FUNC_CTRL1 Register (24h)

This register controls FIFO Interrupt and new data ready Interrupt.

7	6	5	4	3	2	1	0
reserved	reserved	reserved	reserved	FWTM_EI	FFULL_ EI	FEMPTY_ EI	NDR_ EI

INT_FUNC_CTRL1 Register(R/W)

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Initial value: 0x00

Name	Description
FWTM_EI	Enable interrupt for FIFO watermark. Default: 0 0: Disabled 1: Enabled.
FFULL_EI	Enable interrupt for FIFO full. Default: 0 0: Disabled 1: Enabled
FEMPTY_EI	Enable interrupt for FIFO Empty. Default: 0 0: Disabled 1: Enabled
NDR_EI	Enable interrupt for new data ready. Default: 0 0: Disabled 1: Enabled

5.23. INT_FUNC_CTRL2 Register (25h)

Detect HIGH-G and LOW-G motion event of a device.
This register enable/disables interrupts of the high motion and the low motion for each of the 3-axes.

7	6	5	4	3	2	1	0
AO_MI	ZHIE	YHIE	XHIE	DIR_EN	ZLIE	YLIE	XLIE

INT_FUNC_CTRL2 Register(R/W)

Initial value: 0x80

Name	Description
AO_MI	AND/OR combination of motion Interrupt events. Default: 1 0 : AND combination of interrupt events 1 : OR combination of interrupt events

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ZHIE	Enable interrupt generation on Z high event. Default: 0 0 : Disable interrupt 1 : Enable interrupt
YHIE	Enable interrupt generation on Y high event. Default: 0 0 : Disable interrupt 1 : Enable interrupt
DIR_EN	Enable Direction Mode. Default: 0 0: No Direction Mode 1: Enable Direction Detection
XHIE	Enable interrupt generation on X high event. Default: 0 0 :Disable interrupt 1 :Enable interrupt
ZLIE	Enable interrupt generation on Z low event. Default: 0 0 : Disable interrupt 1 : Enable interrupt
YLIE	Enable interrupt generation on Y low event. Default: 0 0 : Disable interrupt 1 : Enable interrupt
XLIE	Enable interrupt generation on X low event. Default: 0 0 : Disable interrupt 1 : Enable interrupt

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5.24. FIFO_CTRL Register (27h)

This register controls FIFO mode selection and FIFO watermark threshold.
SGA100 embeds a 32-depth FIFO for each of the 3-axes.
In bypass mode, FIFO is not operating and remains empty.

In other mode, data from acceleration detection on x, y, and z-axes measurements are stored in FIFO.
When FIFO is full, the FIFO discards the older data (STREAM) or stops collecting data (FIFO).

A watermark interrupt can be enabled. (FWTM_EI bit into INT_FUNC_CTRL1 in order to be raised when the FIFO is filled to the level specified into the WTM_TH bits)

7	6 5	4 0
FFC	FMS[1:0]	WTM_TH[4:0]

FIFO_CTRL Register(R/W)

Initial value: 0x00

Name	Description
FFC	FIFO buffer clear. Default: 0 1: Clear 0: None
FMS[1:0]	FIFO operation mode selection. Default: 00 00: Bypass Mode 01: FIFO Mode 10: Stream Mode 11: Stream-to-FIFO Mode
WTM_TH[4:0]	FIFO threshold. Watermark level setting.(0~31Level) Default: 0

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5.25. FIFO_DATA_STATUS Register (28h)

This is the register that indicates FIFO stored data depth level. It is a read only register.

7	5	4	0
reserved		FSD_DEPTH[5:0]	

FIFO_DATA_STATUS Register(R/O)

Initial value: -

Name	Description
FSD_DEPTH[5:0]	FIFO stored data depth level. Default: 0

5.26. INT_FUNC_CTRL1_STATUS Register (29h)

This register shows the status flag of FIFO interrupt and new data ready interrupt. It is a read only register.

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	NDR	FF_WTM	FF_FULL	FF_EMPTY

INT_FUNC_CTRL1_STATUS Register(R/O)

Initial value: -

Name	Description
NDR	New data ready Interrupt Status. Default: 0 0:No generated 1:Generated new data ready Interrupt
FF_WTM	Watermark Interrupt status. Default: 0 . 0 : FIFO filling is lower than WTM_TH level 1 : Generated WTM Interrupt (FIFO filling is equal or higher than WTM_TH Level)
FF_FULL	FIFO full Interrupt status. Default: 0 . 0 : FIFO not full 1 : Generated FIFO full Interrupt

FF_EMPTY	FIFO empty Interrupt status. Default: 0 0 : FIFO not empty 1 : Generated FIFO empty Interrupt

5.27. MOTION_CTRL Register (2Ah)

This Register specifies threshold motion duration mode for each of the events.
When no duration mode is selected, an interrupts is generated as soon as appropriate threshold is fulfilled.

7	6	5	4	3	2	1	0
Reserved					MOTION_DIR_INT	MOTION_DUR_MODE	

MOTION_CTRL Register(R/W)

Initial value: 0x01

Name	Description
MOTION_DIR_INT	Motion Interrupt Clear Control. Default: 0 0 : Non-latched Interrupt mode 1 : Auto clear mode(1/ODR ms)
MOTION_DUR_MODE[1:0]	Motion duration mode selection. Default: 01 00:Up & down Duration 01:Only Up Duration 10:Only down Duration 11: No Duration

5.28. MOTION_STATUS Register (2Bh)

This is the register that indicates the high-g and low-g motion interrupt status for each of the axes.
It is a read only Register.

7	6	5	4	3	2	1	0
Reserved	ZH	YH	XH	Reserved	ZL	YL	XL

MOTION_STATUS Register(R/O)

Initial value: -

Name	Description
ZH	Z High event status. Default: 0 0 : no interrupt 1 : ZH Interrupts has occurred
YH	Y High event status. Default: 0 0 : no interrupt 1 : YH Interrupts has occurred
XH	X High event status. Default: 0 0 : no interrupt 1 : XH Interrupts has occurred
ZL	Z Low event status. Default: 0 0 : no interrupt 1 : ZL Interrupts has occurred
YL	Y Low event status. Default: 0 0 : no interrupt 1 : YL Interrupts has occurred
XL	X Low event status. Default: 0 0 : no interrupt 1 : XL Interrupts has occurred

5.29. MOTION_HIGH_TH Register (2Ch)

This register specifies high-g threshold for the event detection.
The high-g threshold level can be selected anywhere in full scale range.

7							0
HIGH_TH[7:0]							

MOTION_HIGH_TH Register(R/W)

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Initial value: 0xBE

Name	Description
HIGH_TH[7:0]	High-g detection threshold. Unsigned format. Scale Factor: x128 count. Default: 0xBE High-g interrupt trigger threshold according to HIGH_TH[7:0]* scale factor in a range from 0 count to 32670 count

5.30. MOTION_HIGH_DUR Register (2Dh)

This Register specifies the duration of the High-g threshold for the event detection.

7							0
HIGH_DUR [7:0]							

MOTION_HIGH_DUR Register(R/W)

Initial value: 0x02

Name	Description
HIGH_DUR	High Event Duration Threshold. Unsigned format. Default:0x02 (Duration/ODR ms)

5.31. MOTION_LOW_TH Register (2Eh)

This register specifies low-g threshold for the event detection.
The low-g threshold level can be selected anywhere in full scale range.

7							0
LOW_TH[7:0]							

MOTION_LOW_TH Register(R/W)

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Initial value: 0x2D

Name	Description
LOW_TH[7:0]	Low Event Detection Threshold. Unsigned format. Scale Factor: x128 count Default: 0x2D low-g interrupt trigger threshold according to LOW_TH[7:0]* scale factor in a range from 0 count to 32670 count

5.32. MOTION_LOW_DUR Register (2Fh)

This Register specifies the duration of the low-g threshold for the event detection.

7							0
LOW_DUR [7:0]							

MOTION_LOW_DUR Register(R/W)

Initial value: 0x02

Name	Description
LOW_DUR	Low Event Duration Threshold. Unsigned format. Default:0x02 (Duration/ODR ms)

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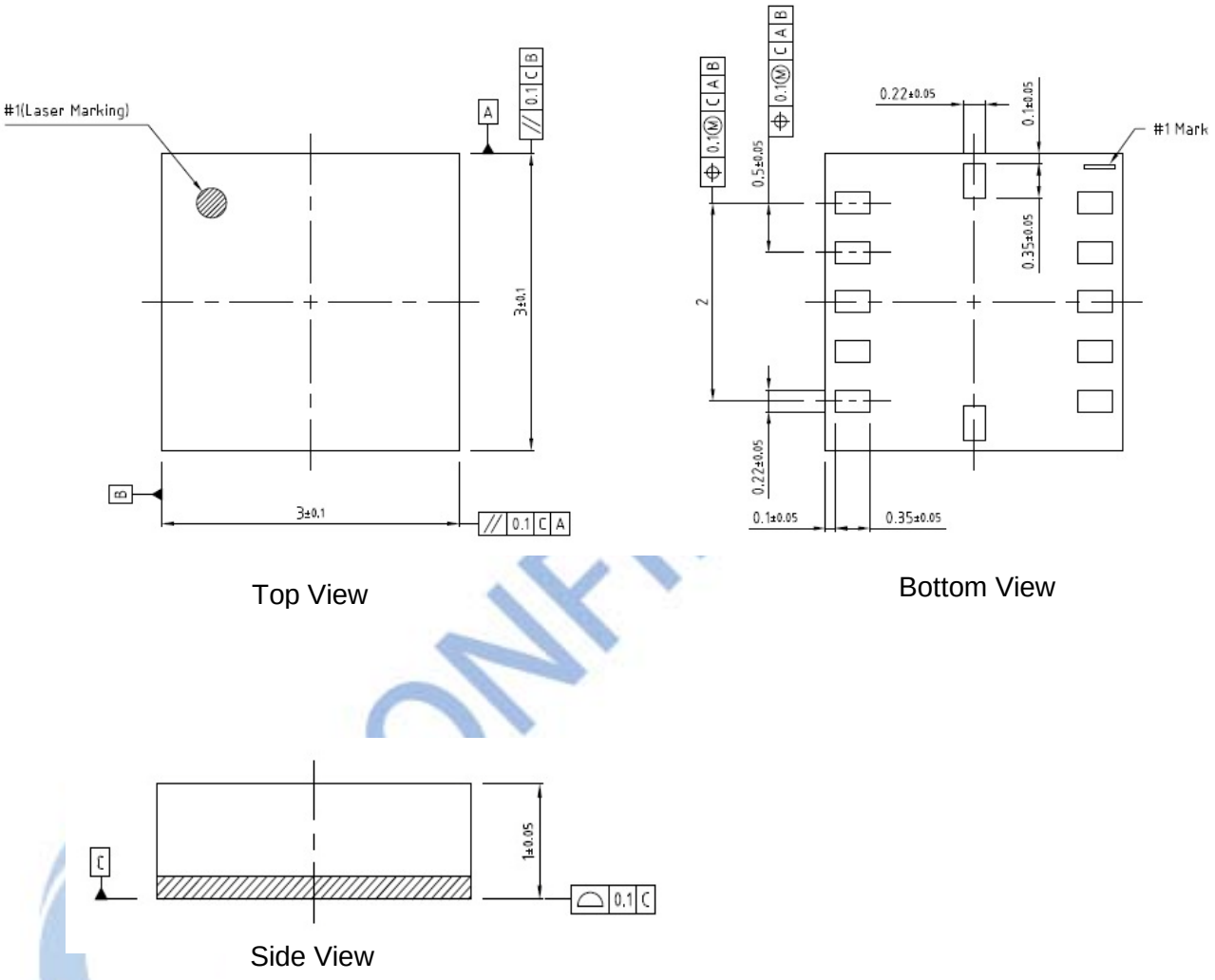
6. Package Information

6.1. Package dimensions

SGA100 is packaged in a 3mm x 3mm x 1.0mm 12LGA Package.



Top View

Bottom View

Side View

Figure 13. Top, Bottom and Side views of the LGA Package (Dimensions in mm)

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6.2. Axes orientation

The Following diagram describes the orientation of the package with respect to the axes of acceleration measurement.

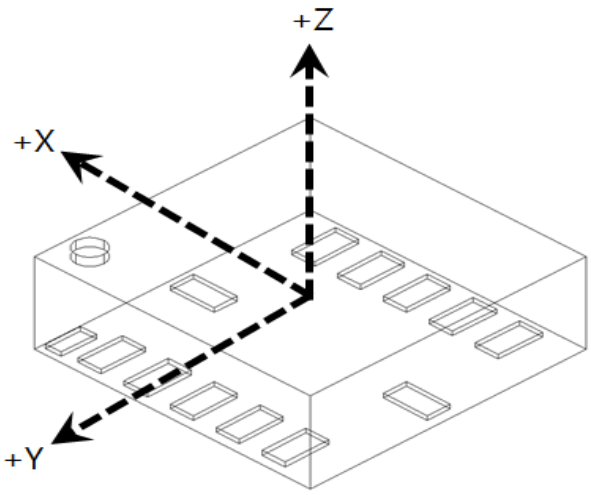

Figure 14. Axis Orientation of the SGA100

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7. Revision History

Revision	Date	changes
1.0		First release.

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