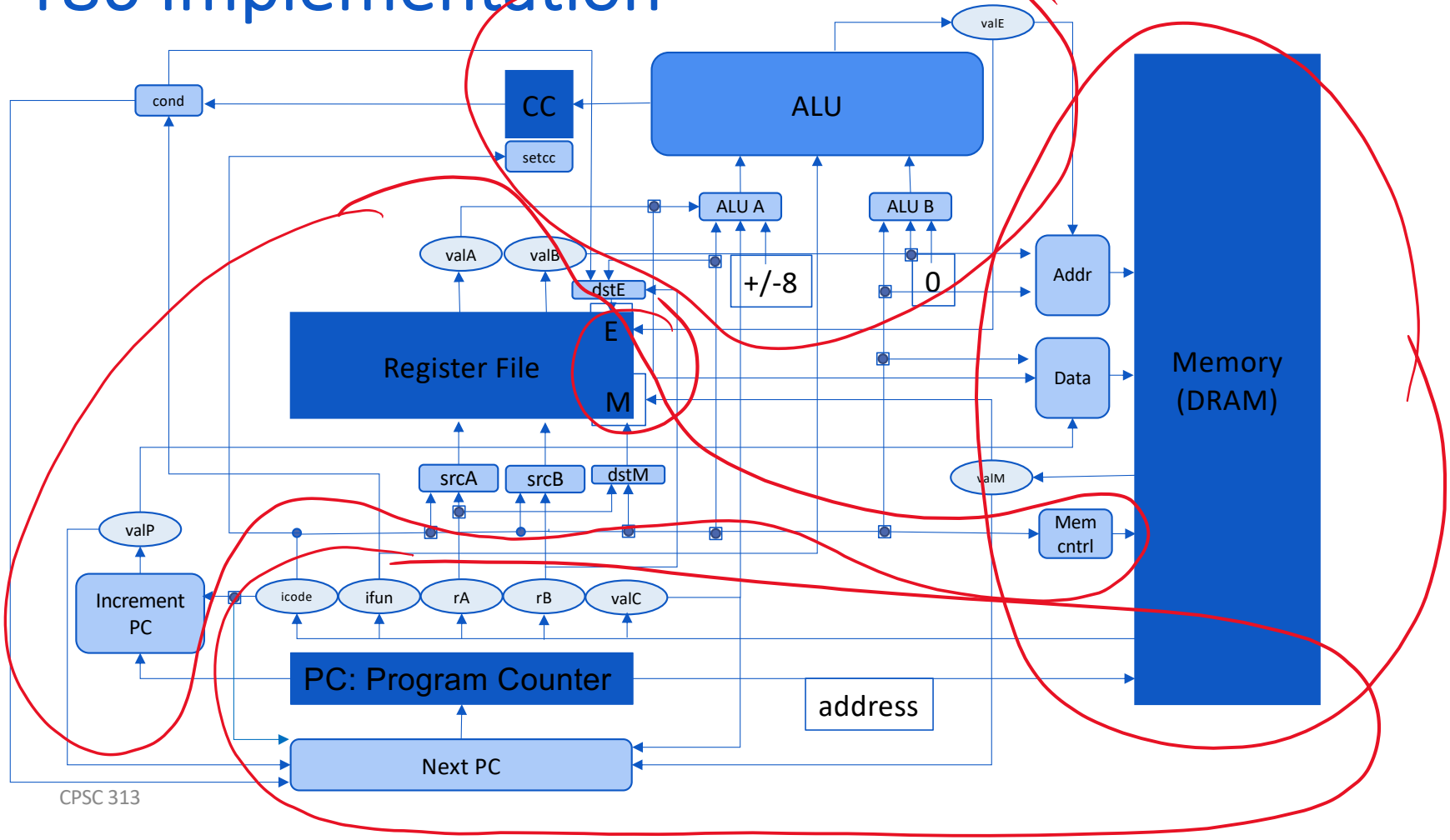
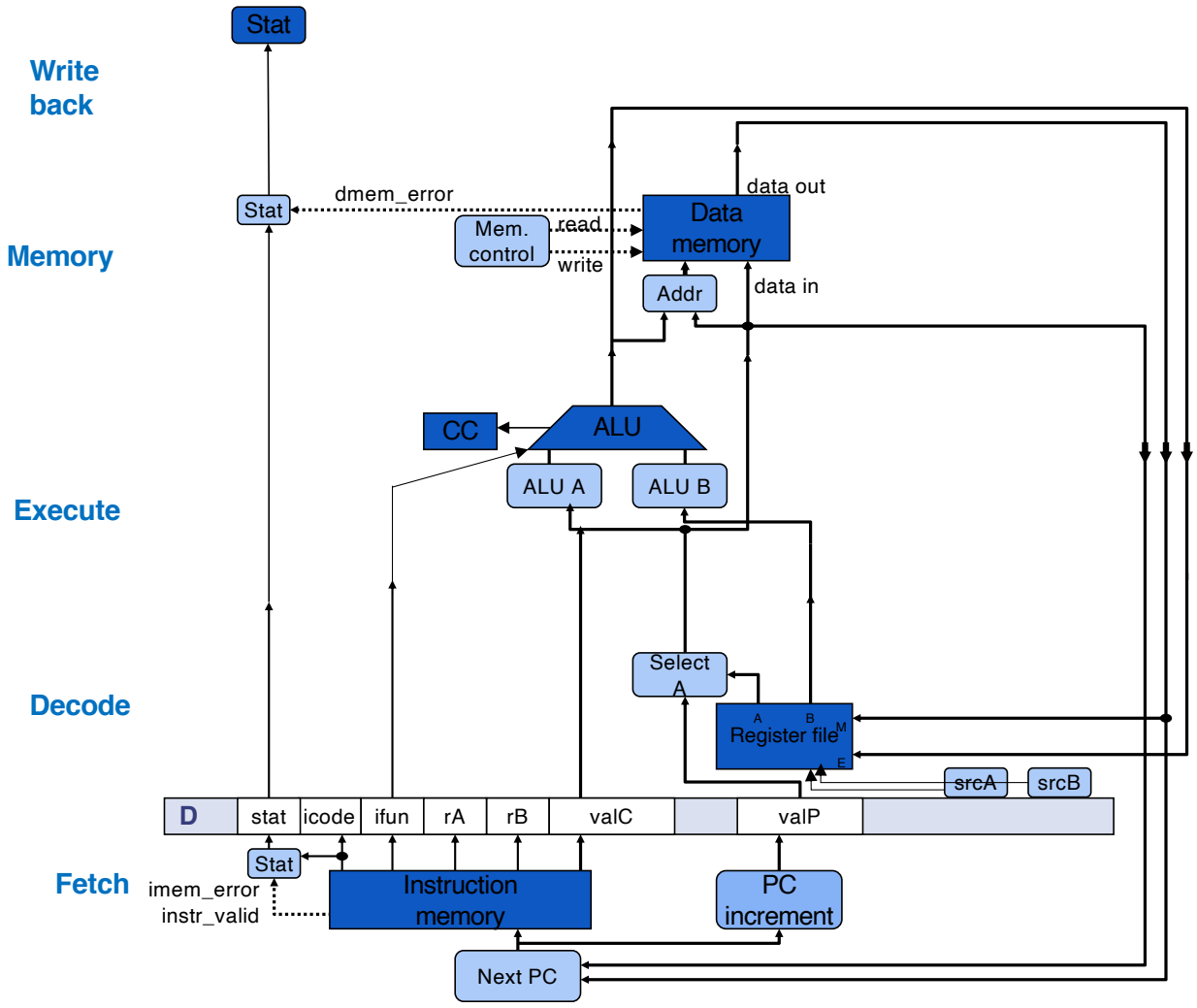
Pipeline Registers

- Topics
  - Rearranging the implementation for pipelining
  - Introducing pipeline registers
  - Figuring out what information is needed in each register
- Learning outcomes
  - Place pipeline registers to create a y86 pipelined architecture
  - Define hazard
  - Identify hazards in an implementation
- Reading
  - 4.4.4, 4.5.1 – 4.5.5

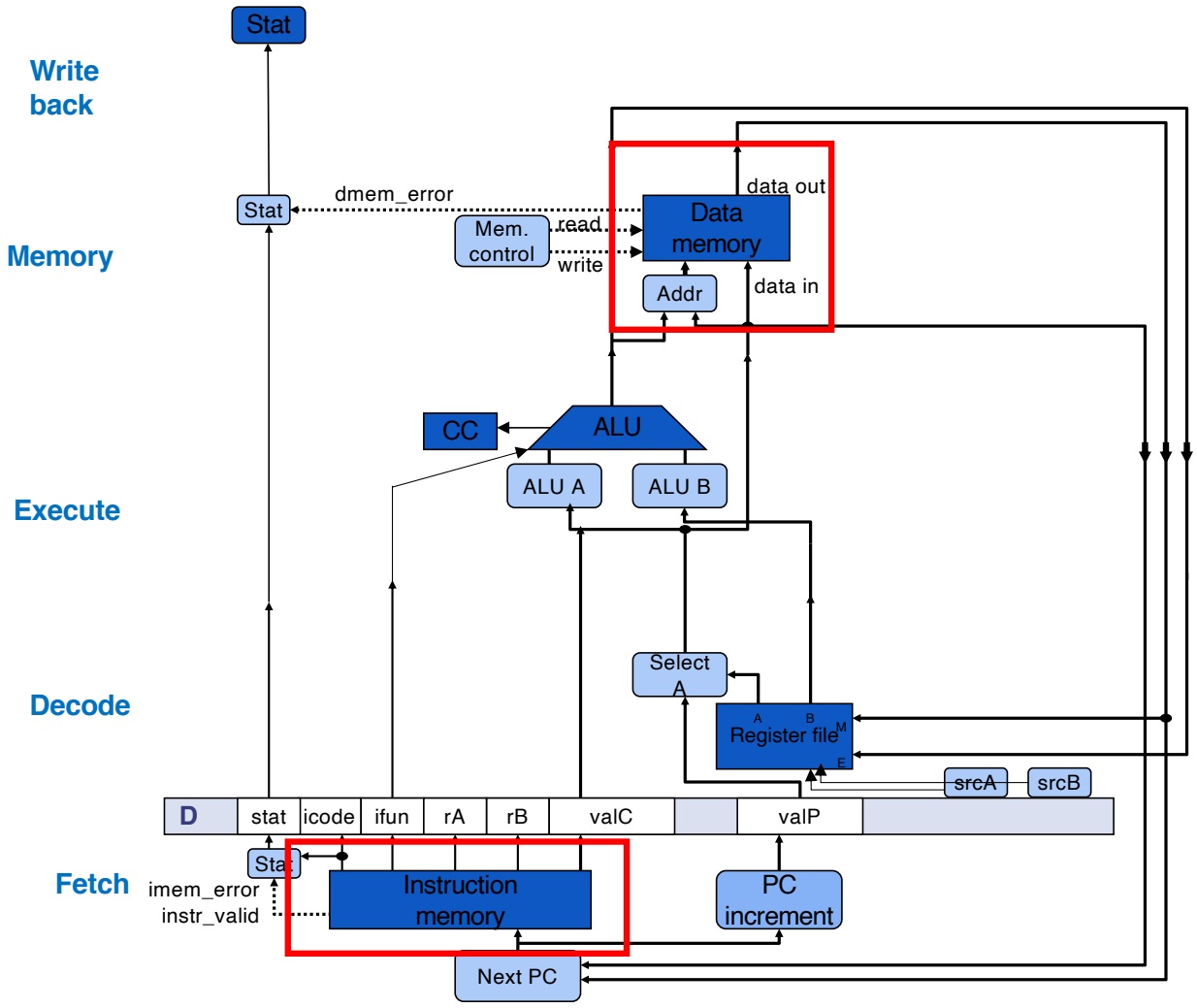
Y86 Implementation



Y86 Rearranged



Y86 Rearranged



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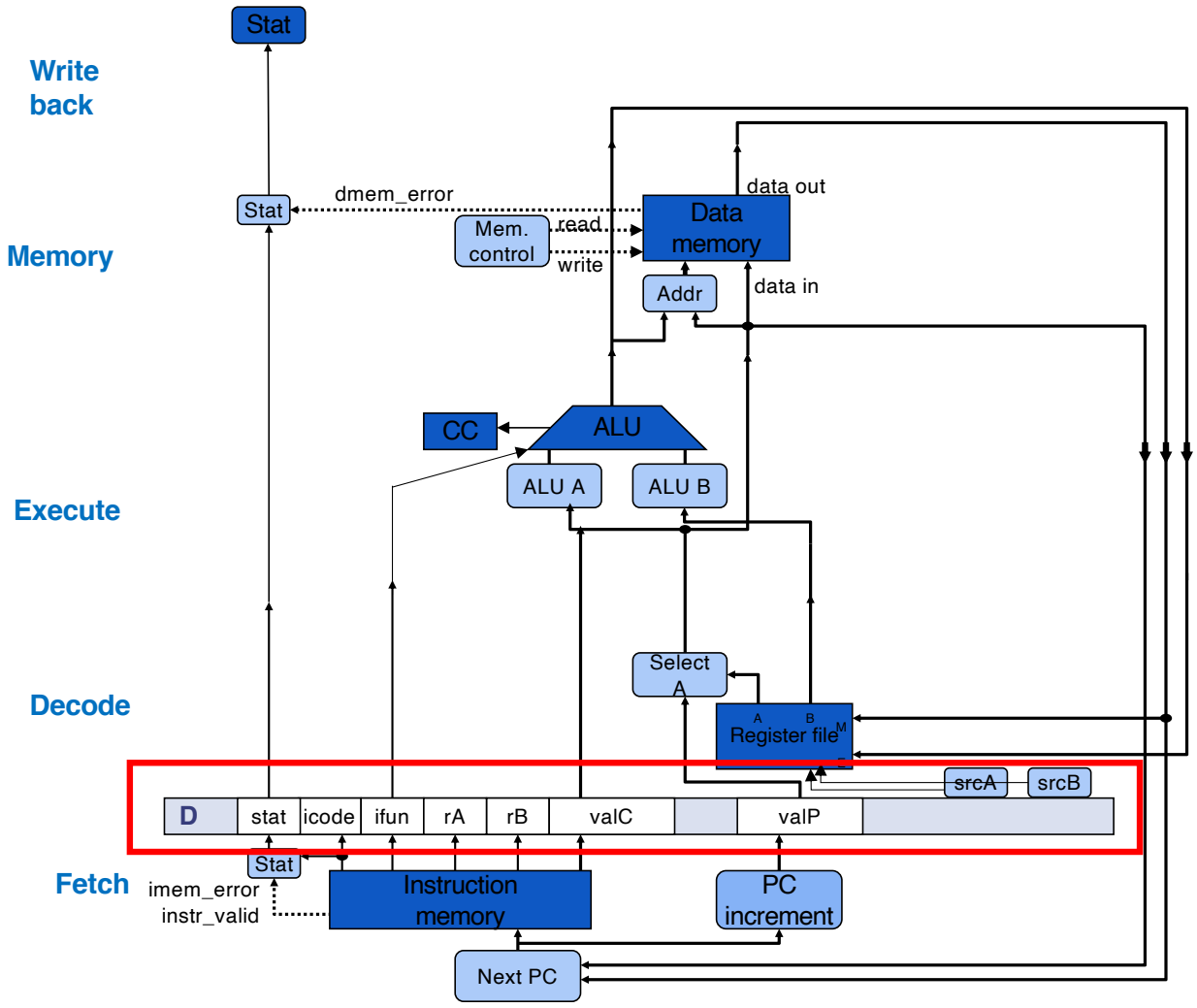

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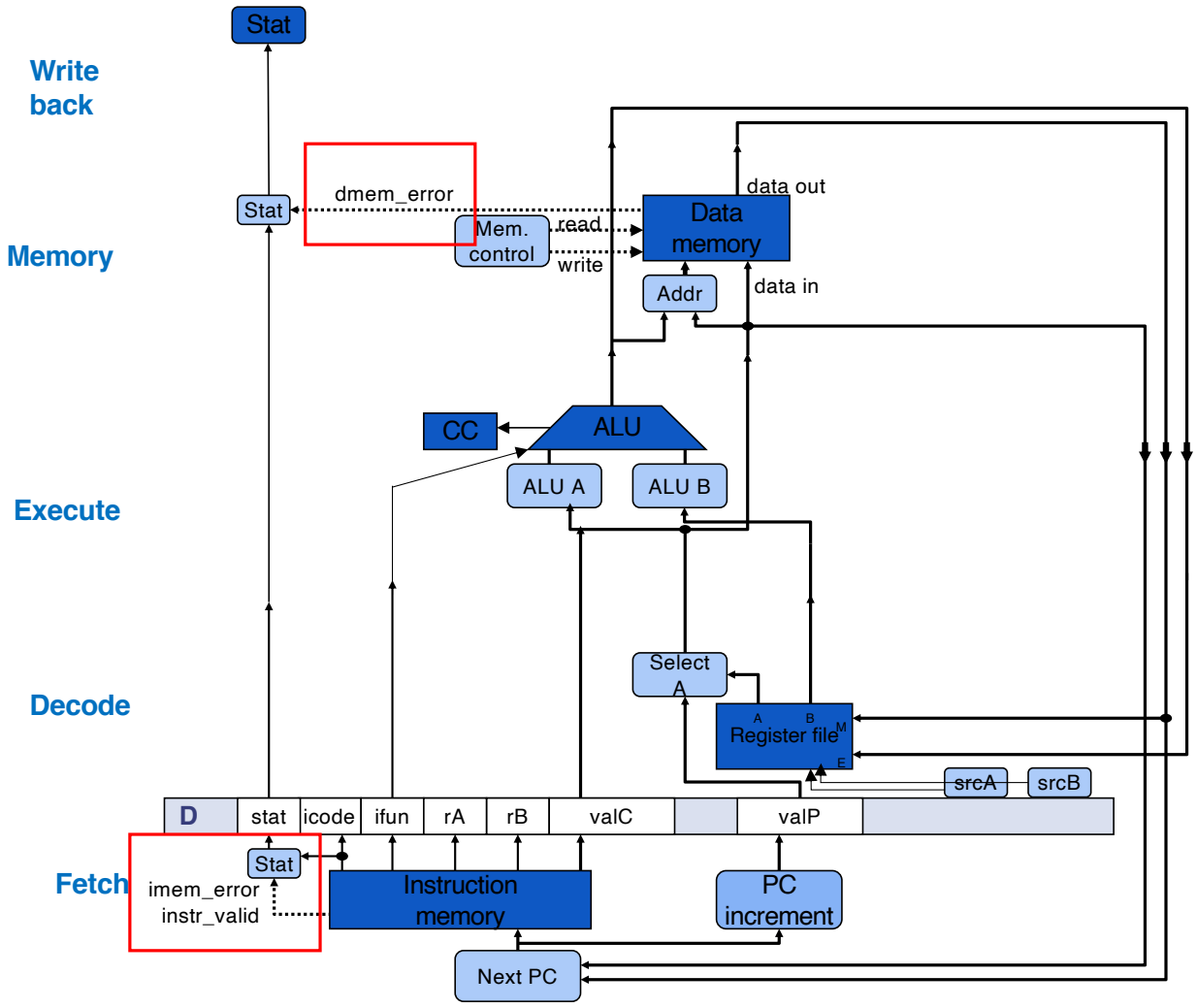

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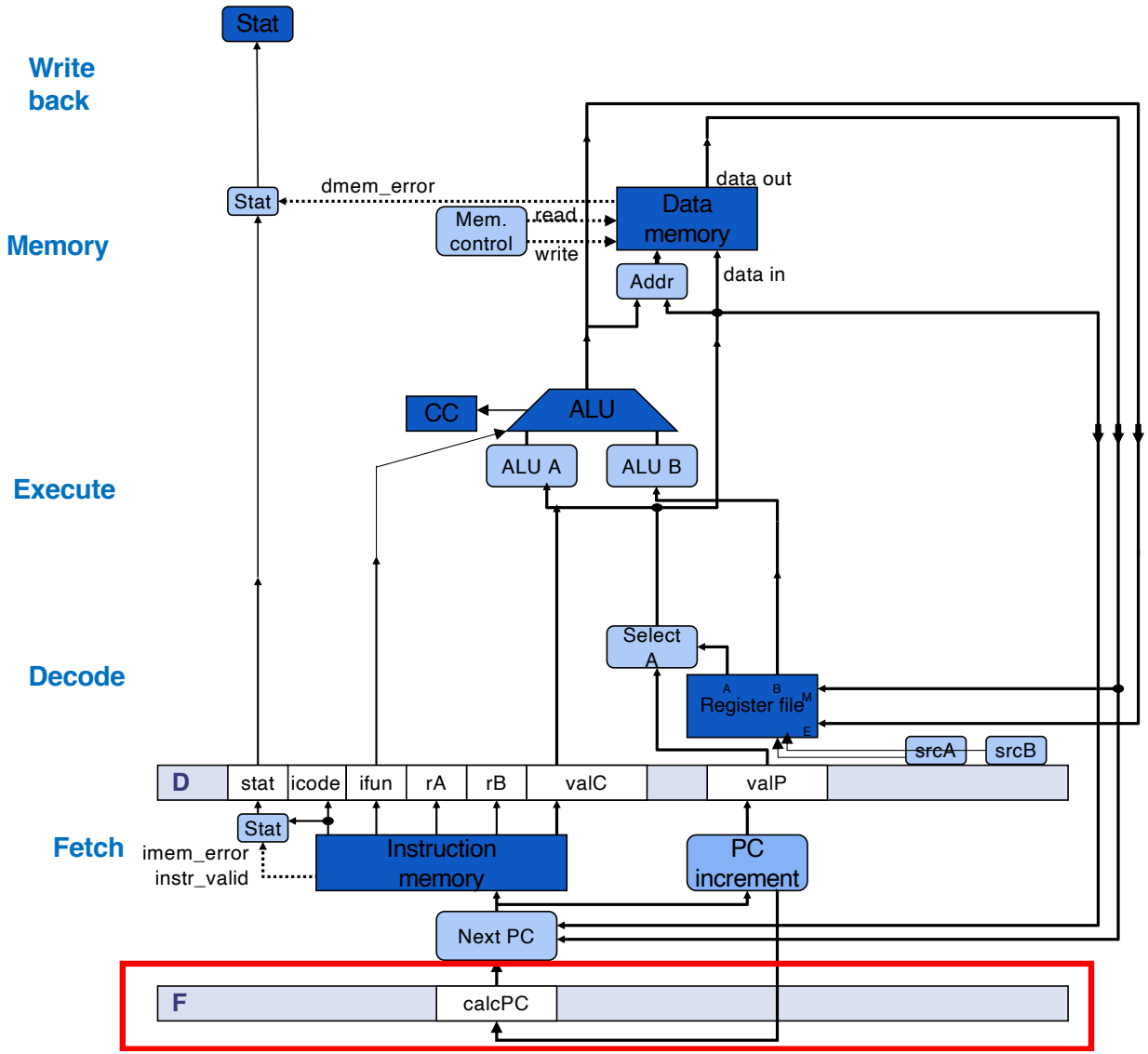

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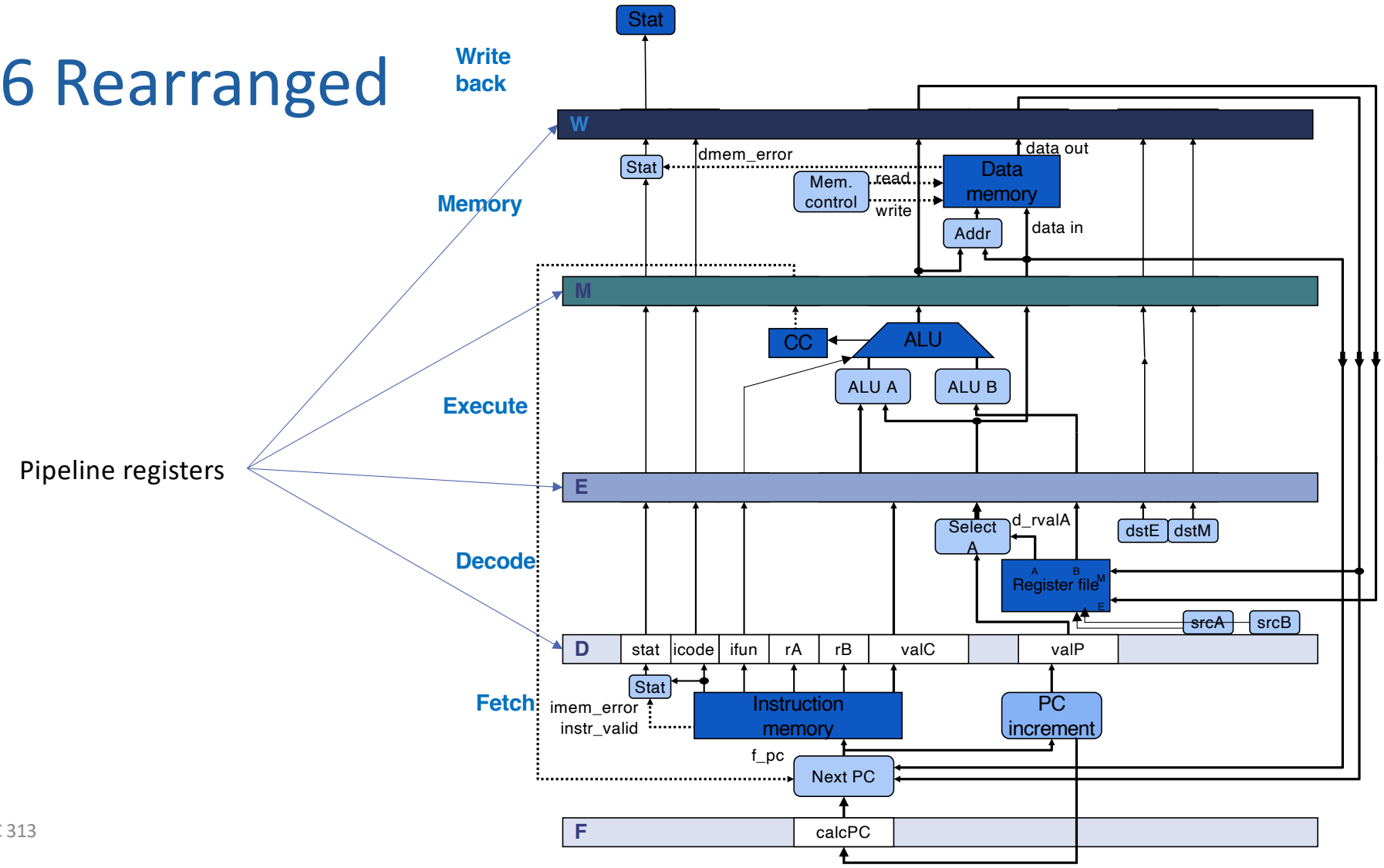

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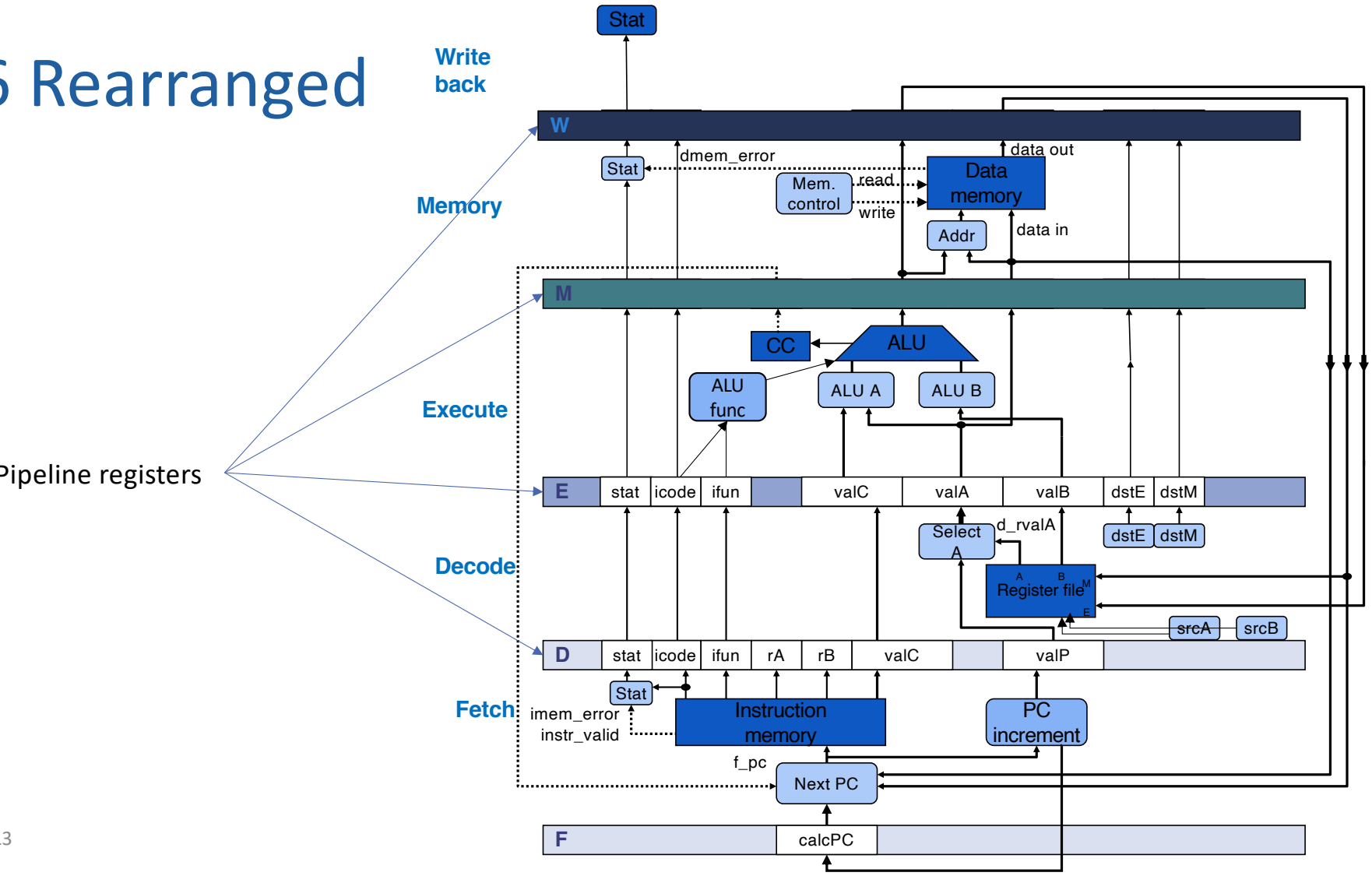

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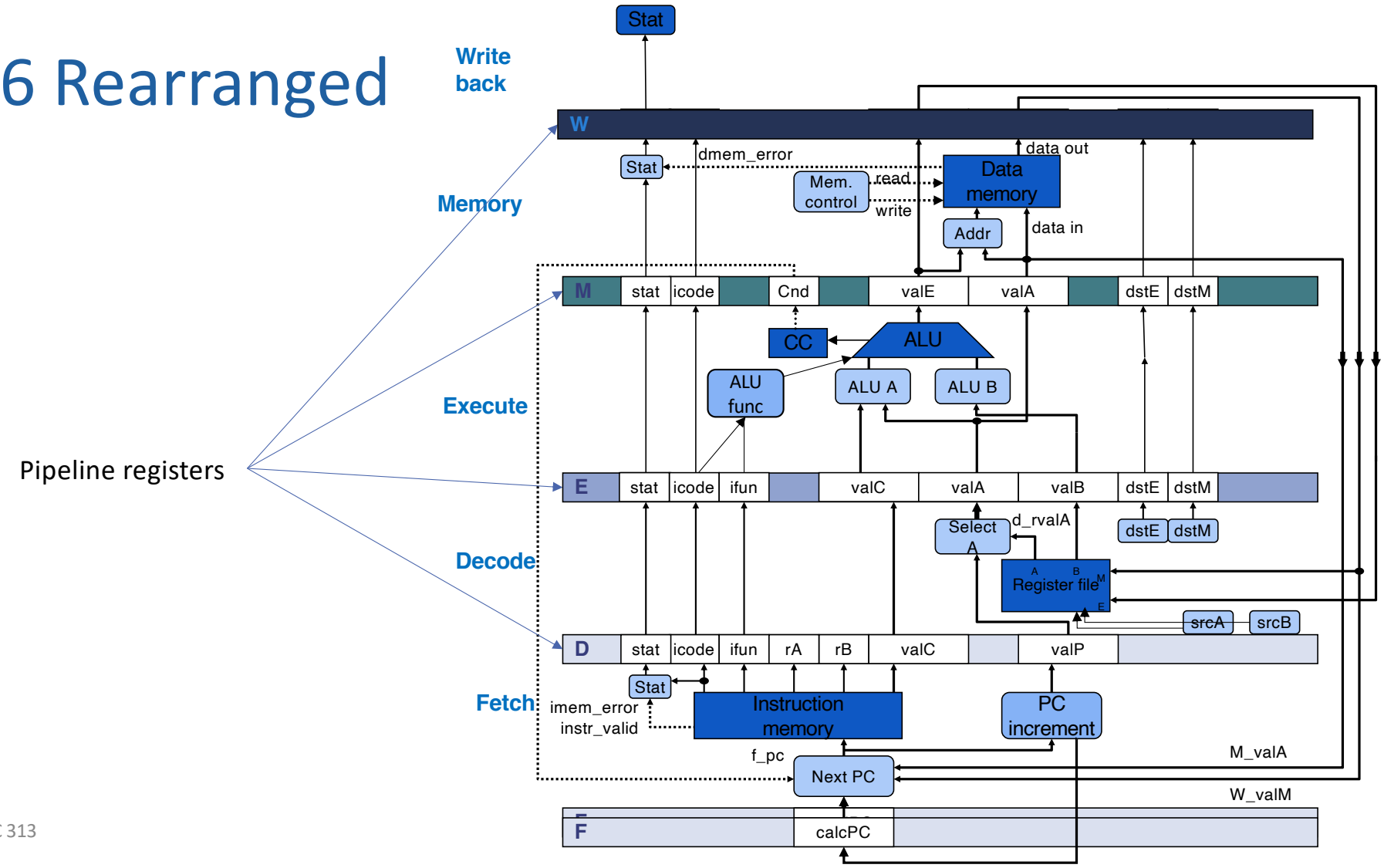

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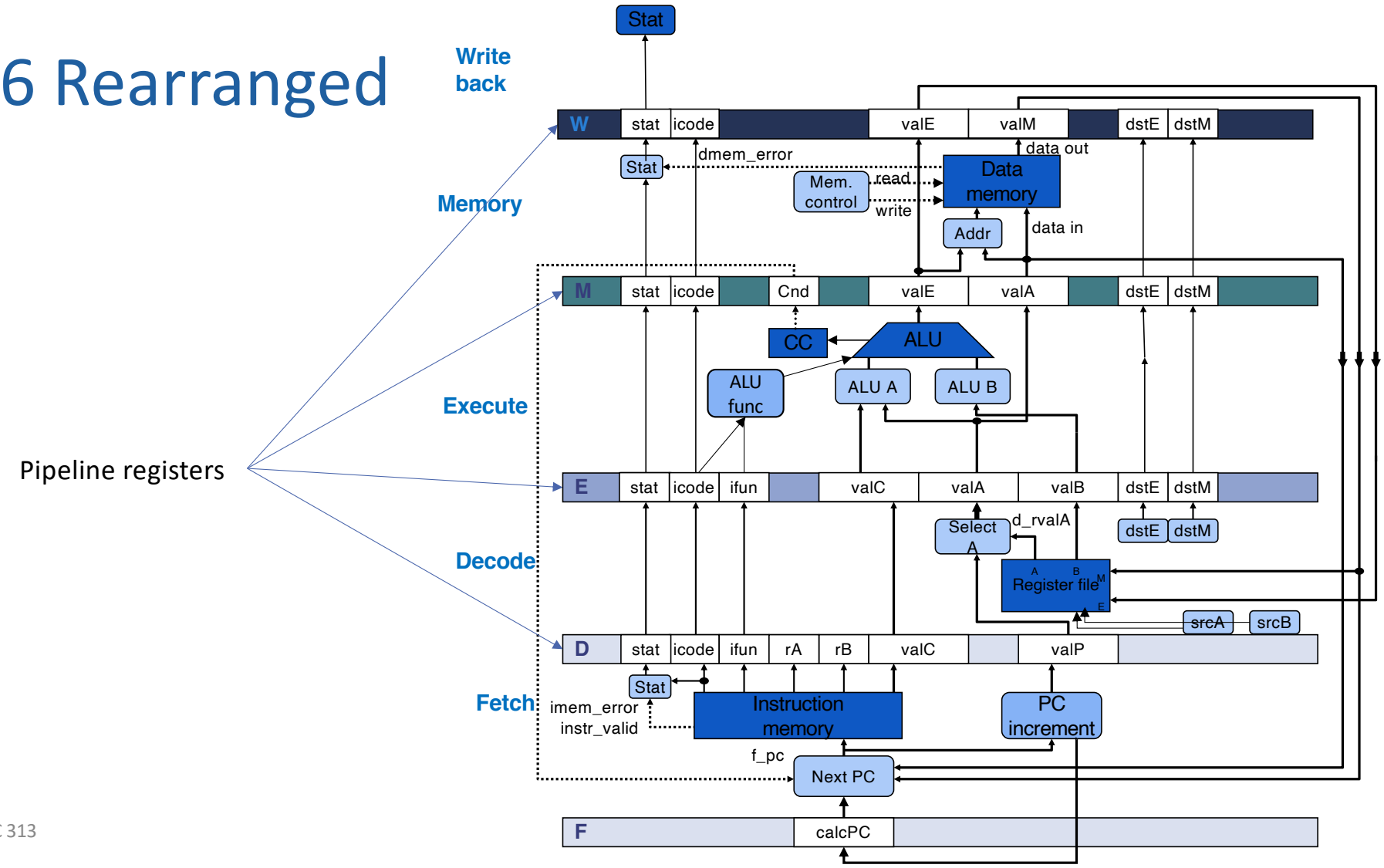
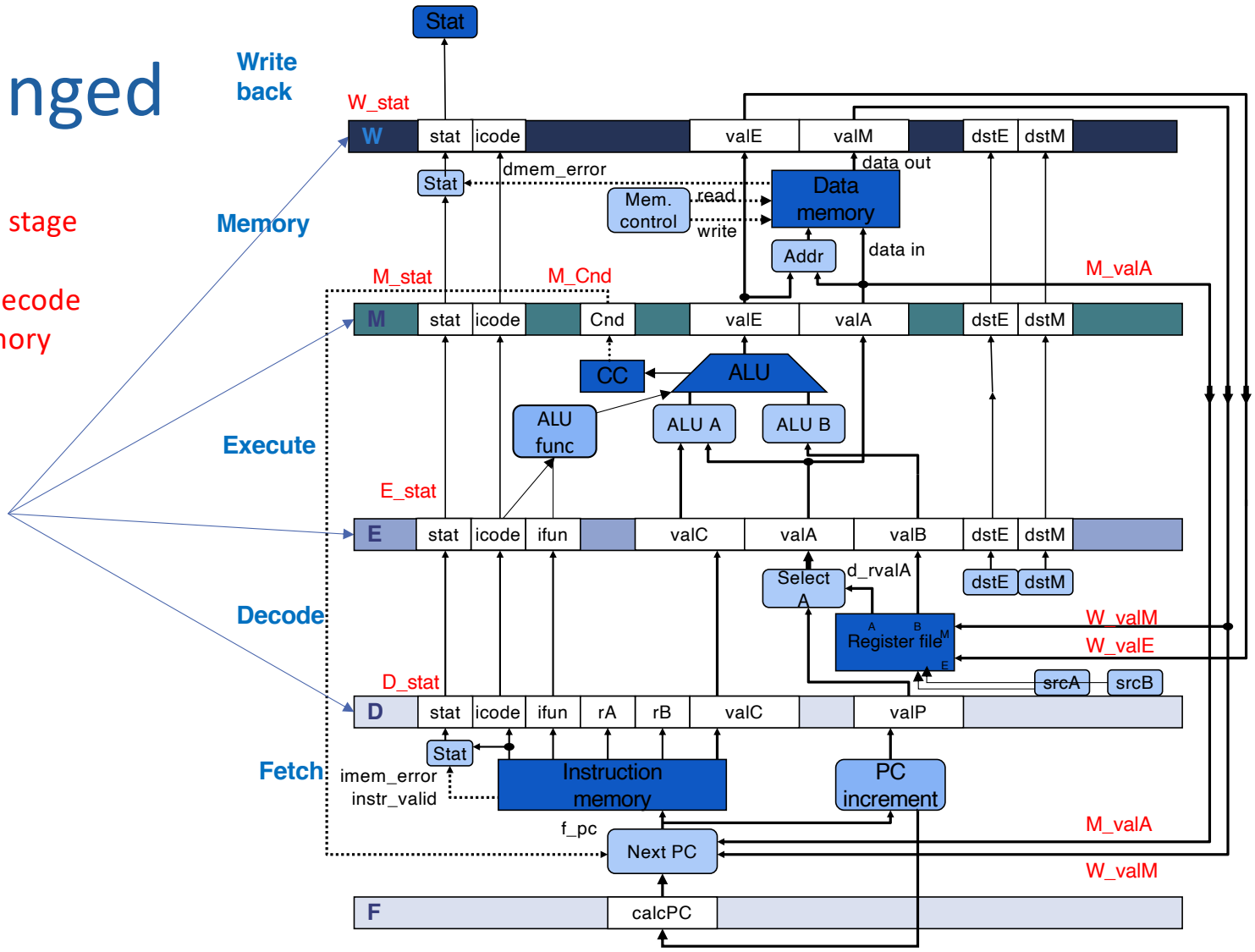


Y86 Rearranged

Preface signal names:
S_signal: a signal from the S stage
Examples:

- D_stat: right out of the decode
- M_stat: right out of memory

Pipeline registers



Y86 Rearranged

Preface signal names:
S_signal: a signal from the S stage
Examples:

- D_stat: right out of the decode
- M_stat: right out of memory

- d_stat: At the very end of the decode stage

Pipeline registers