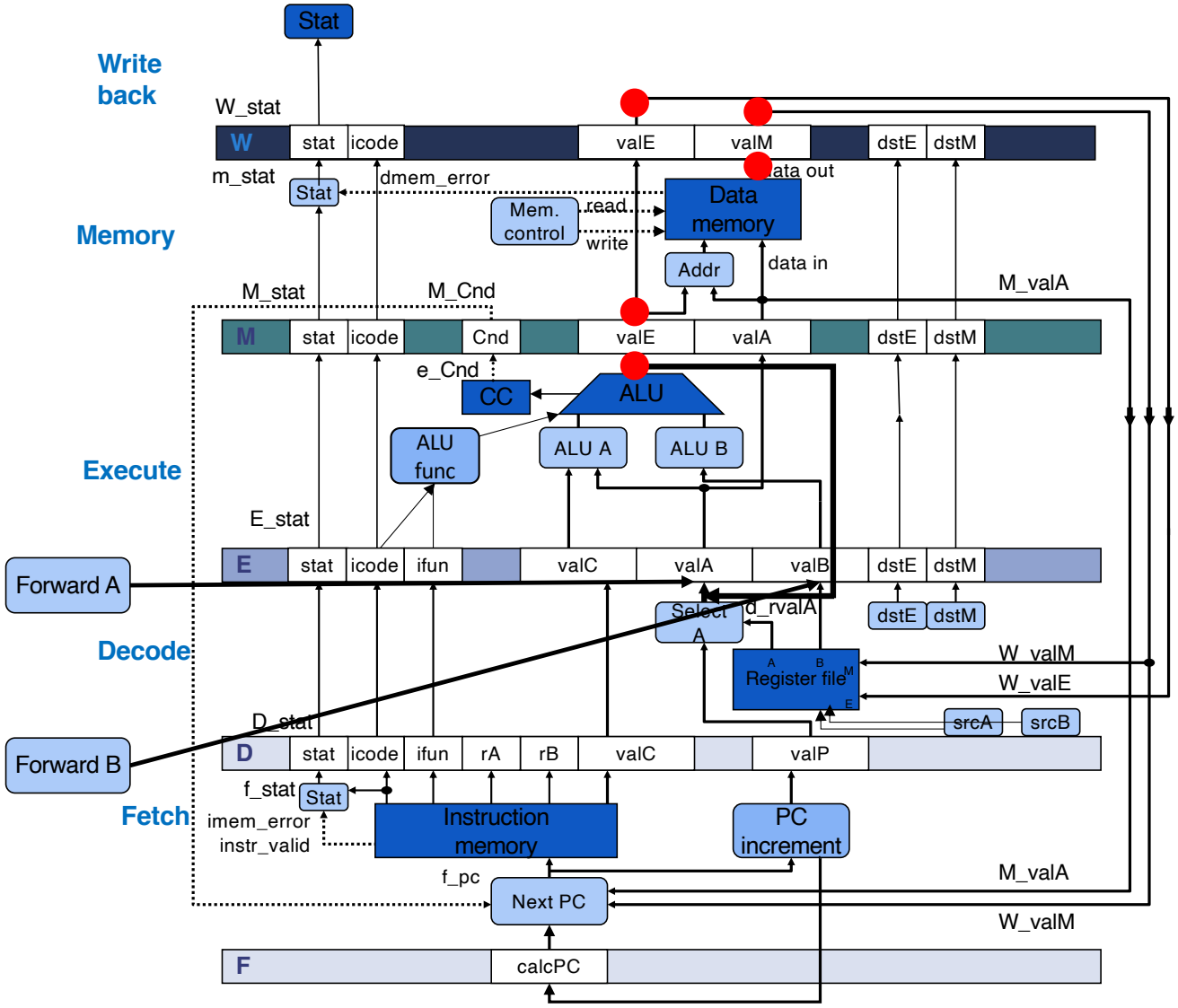
Control Hazards

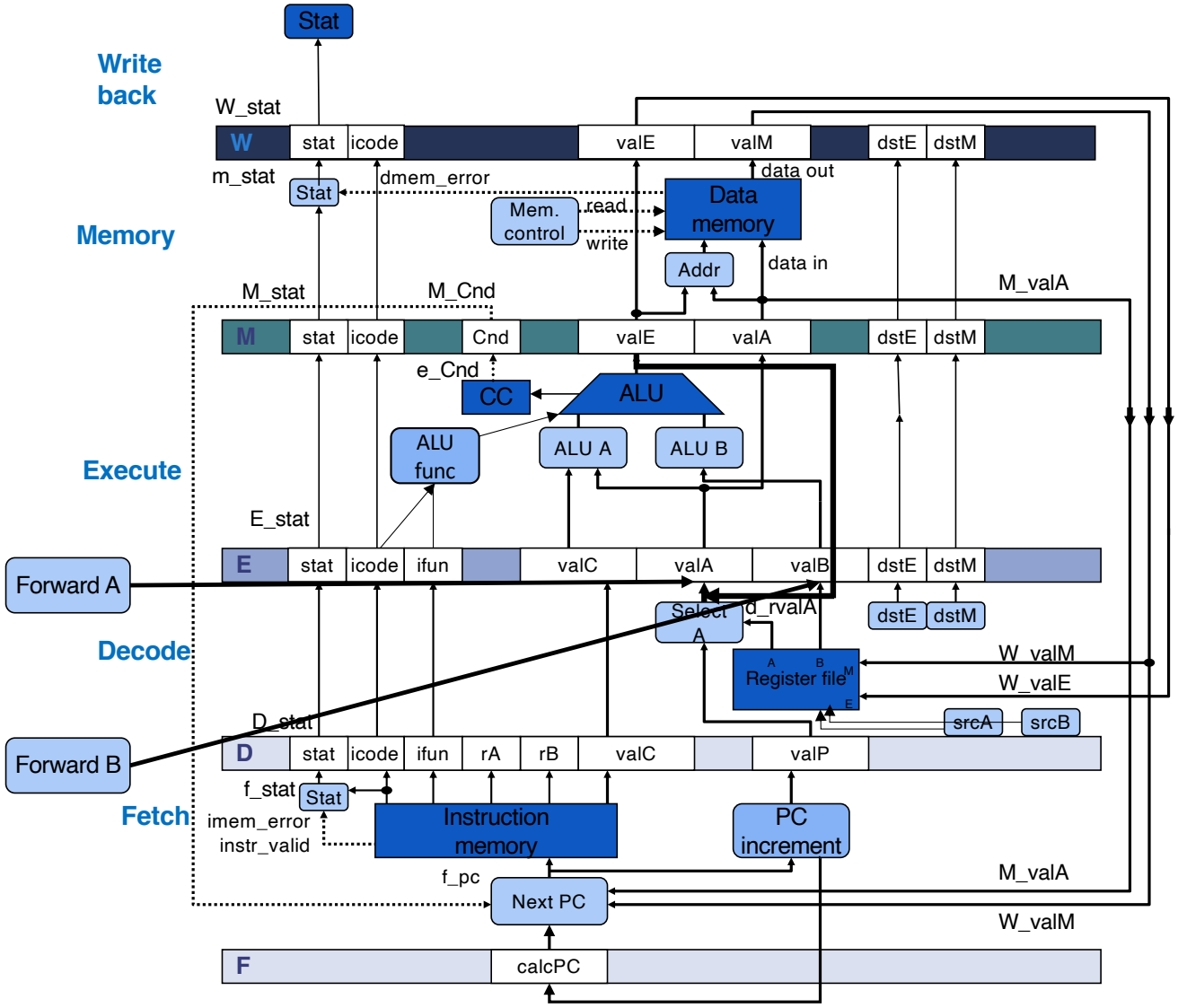
- Topics
  - Jump instructions in a pipelined implementation
  - Control hazards
- Learning outcomes
  - Identify when control flow instructions introduce hazards
  - Distinguish between hazards that can be addressed and hazards that cannot be addressed.
- Reading
  - 4.5.5 (Section on Avoiding Control Hazards)

Where we left off:



Unconditional Jmp

When do we need the address of the next instruction?

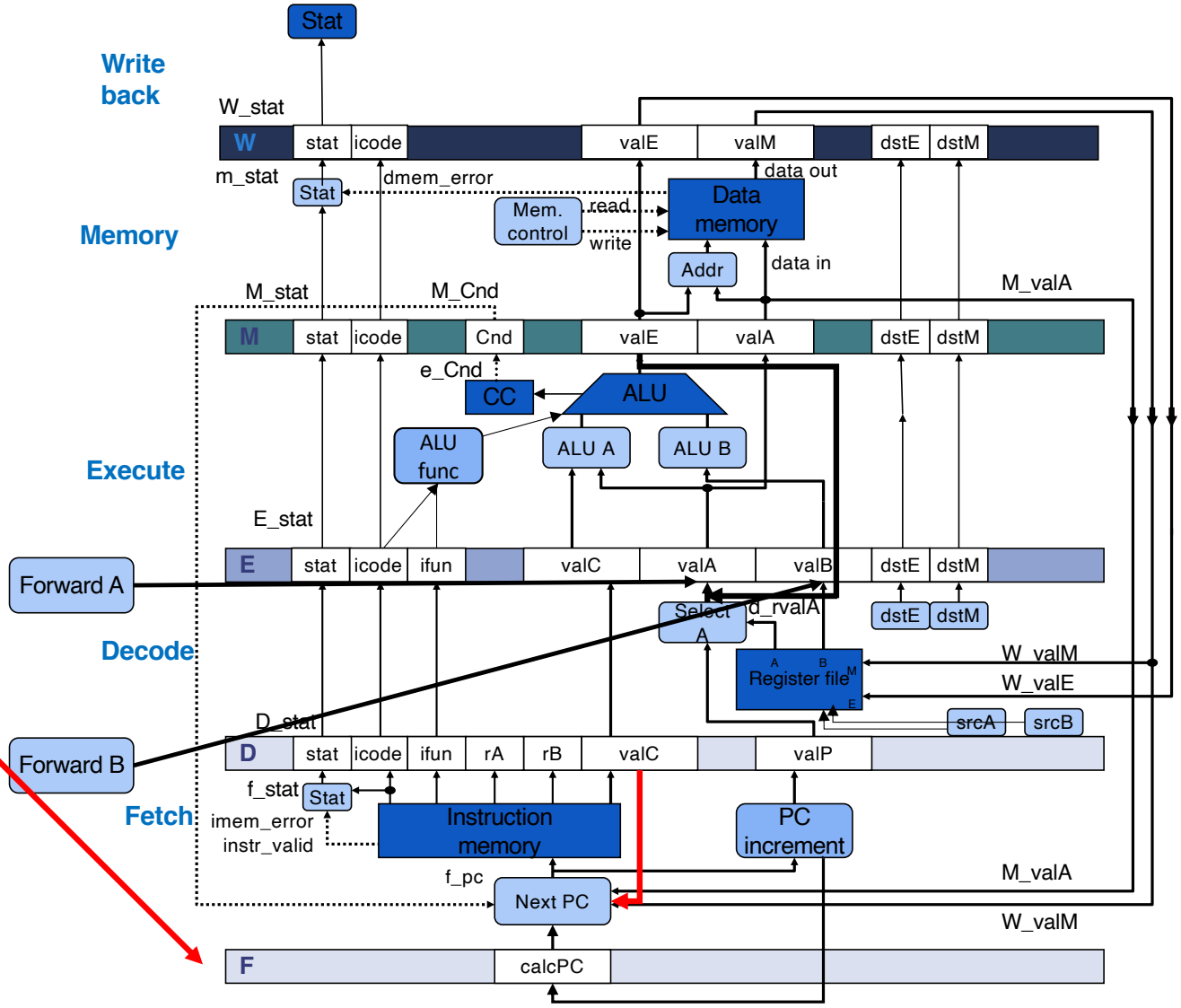


Unconditional Jmp

When do we need the address of the next instruction?

At the fetch stage of the next instruction.

From where do we get it?



Unconditional Jmp

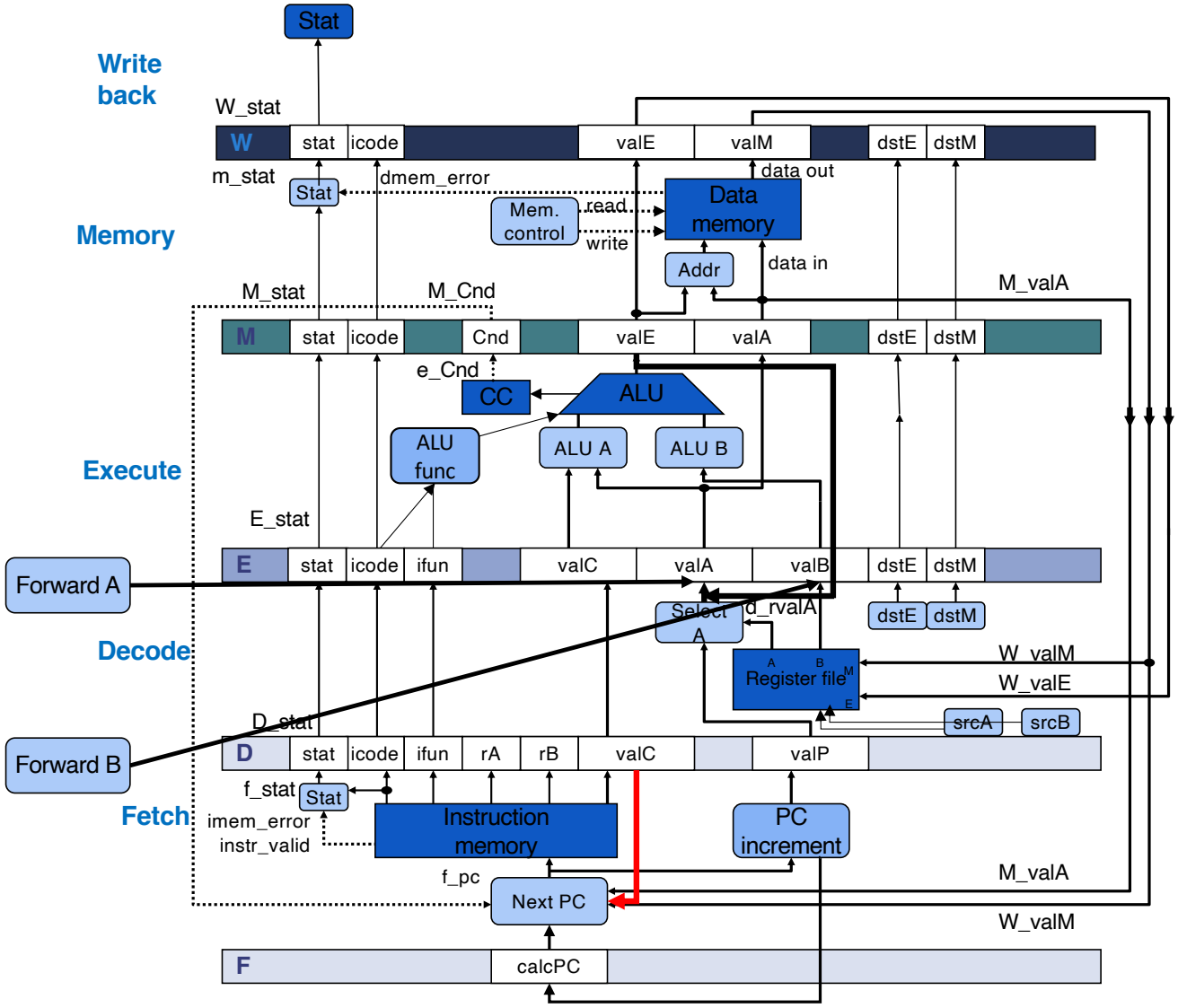
When do we need the address of the next instruction?

At the fetch stage of the next instruction.

From where do we get it?

f_valC

What about a CALL instruction?



CALL

When do we need the address of the next instruction?

At the fetch stage of the next instruction.

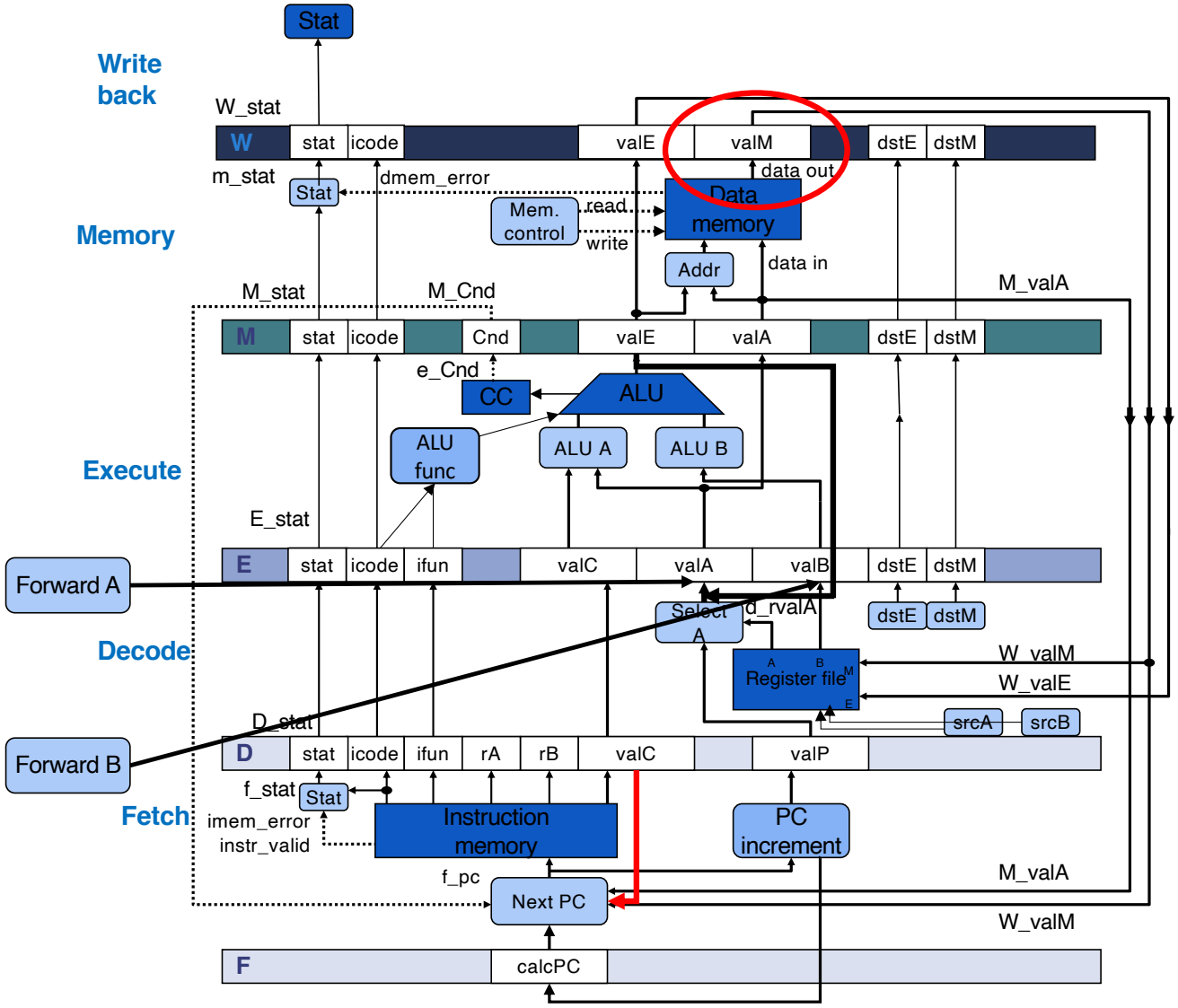
From where do we get it?

f_valC

What about a CALL instruction?

No problem!

What about RET?



RET Instructions

- RET instructions are always going to require that we stall for three cycles, because we simply do not have the information we need.

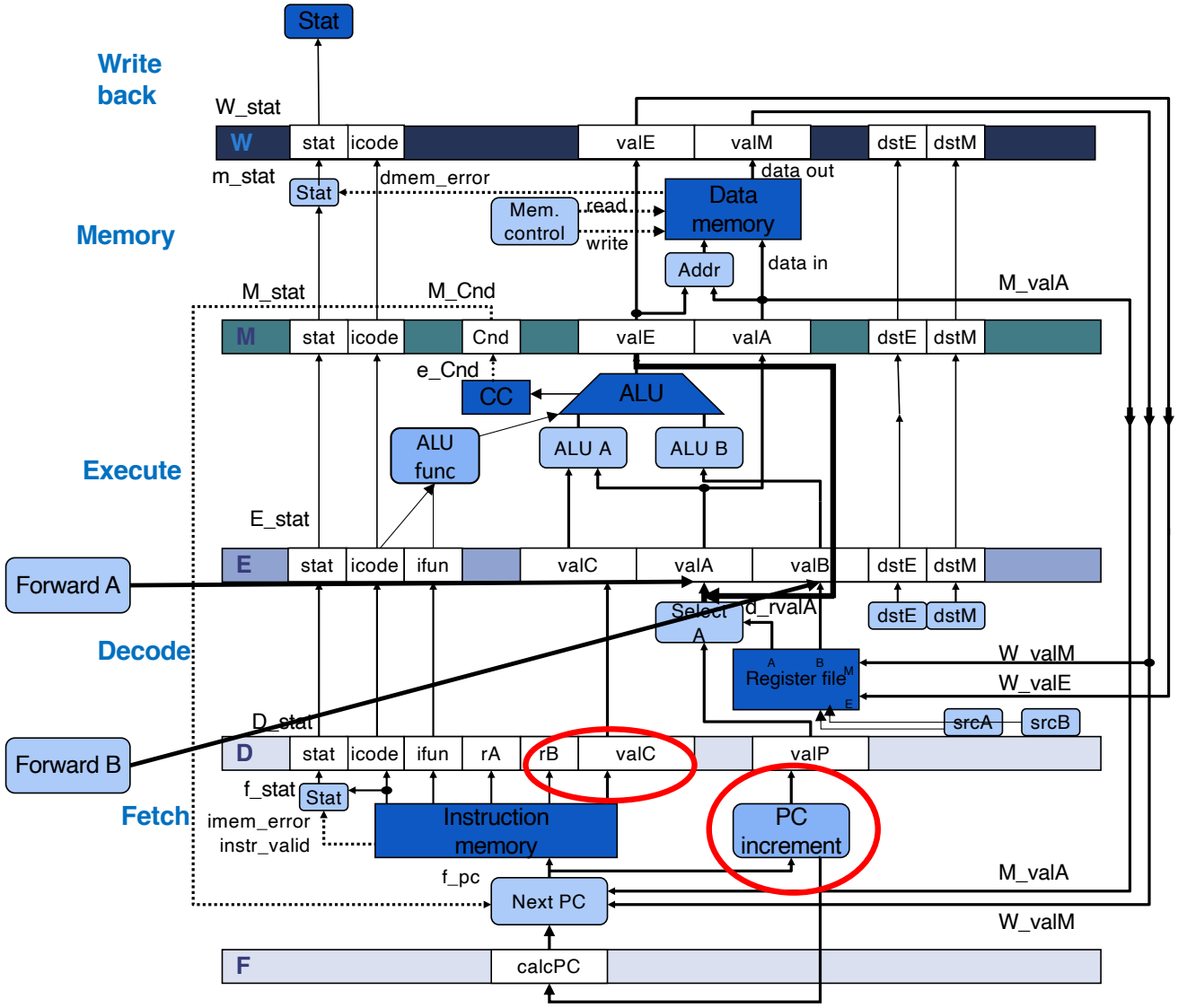
Conditional Jmp

We need the address during the fetch stage of the next instruction.

Two choices:

- valC from the instruction
- Result of PC increment

What tells us which to choose?



Conditional Jmp

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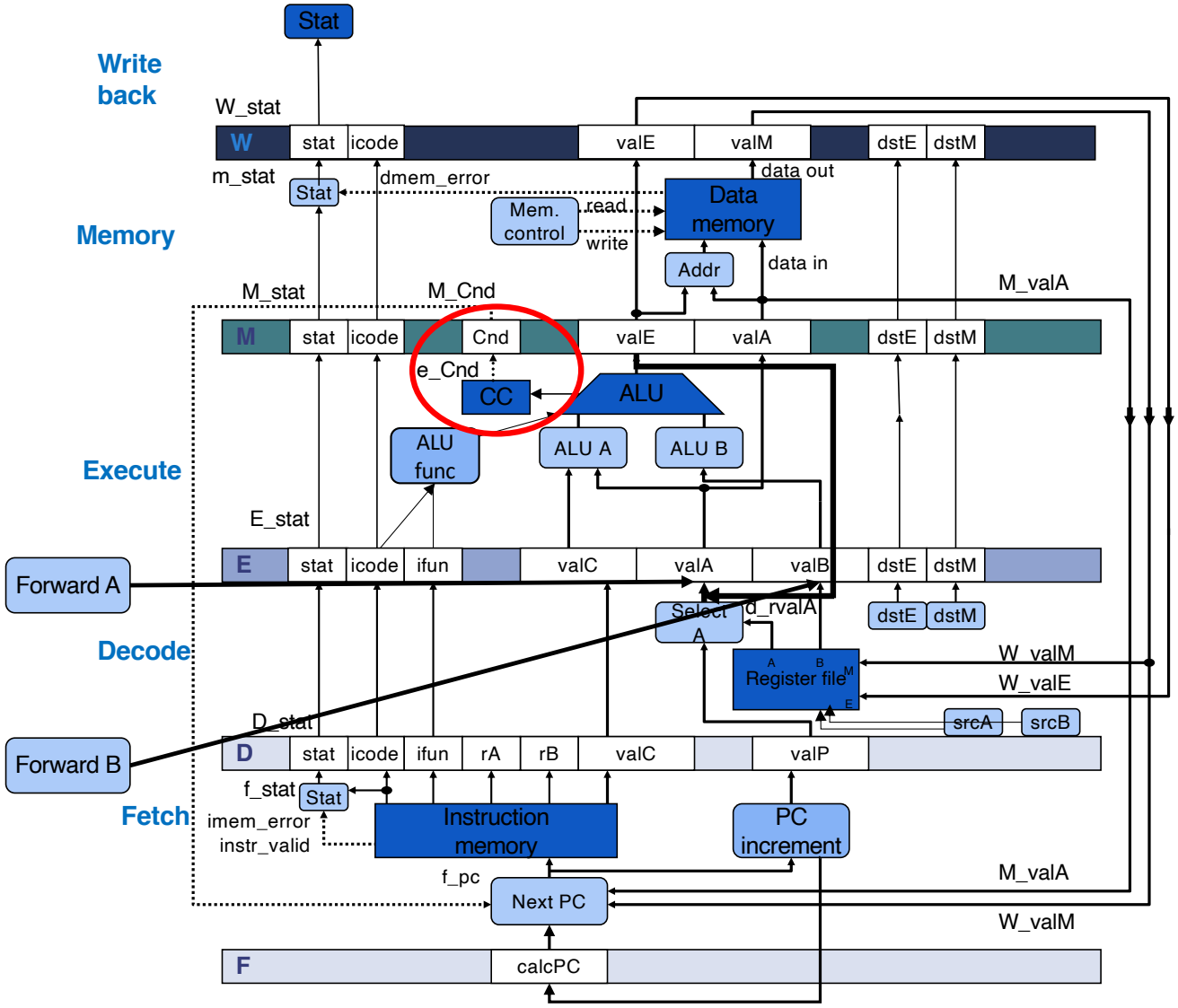
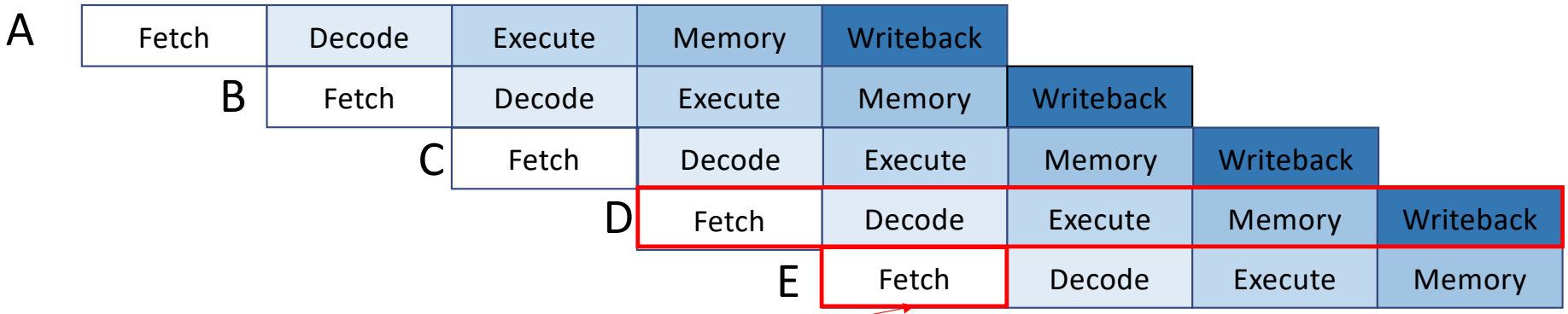


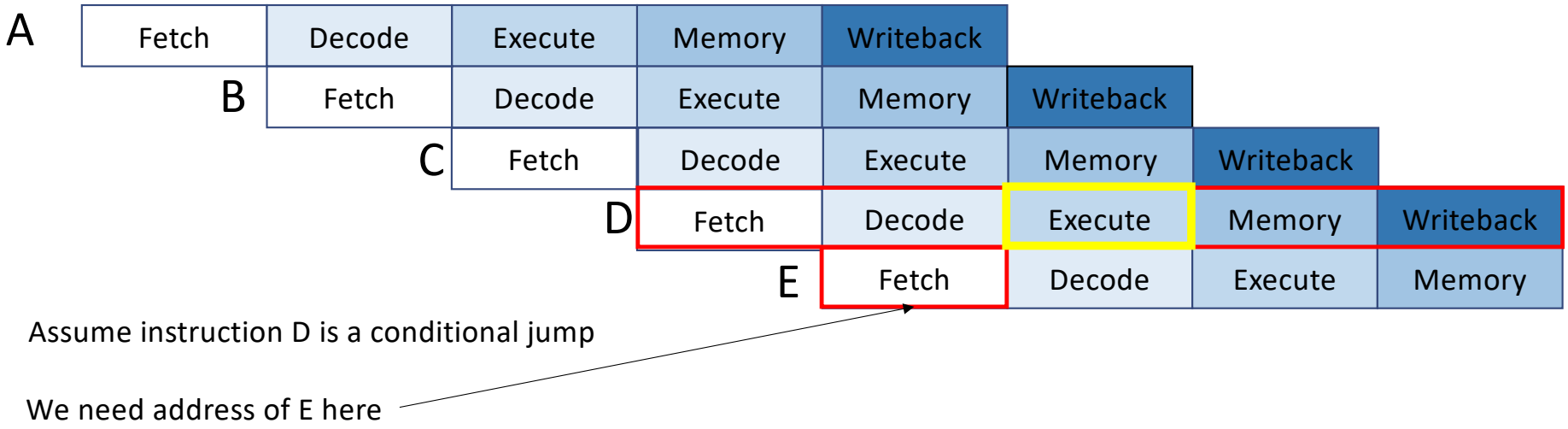
When do we have condition code values?



Assume instruction D is a conditional jump

We need address of E here

When do we have condition code values?



Dealing with Control Hazards

- Unconditional jumps (and CALL) pose no problem
- RET is always a problem (i.e., we cannot do anything)
- Conditional jumps provide an opportunity:
  - We know both addresses in time
  - We just don't know which one
  - Can we make an educated guess?