CAMERA PLCC SPECIFICATION

Customer: _____

Product Description: IMX219 6.5*6.5 PLCC

Version: 1.0

Revision History

Version	Date [Y/M/D]	Notes	Writer

Approved By	Reviewed By	Prepared By

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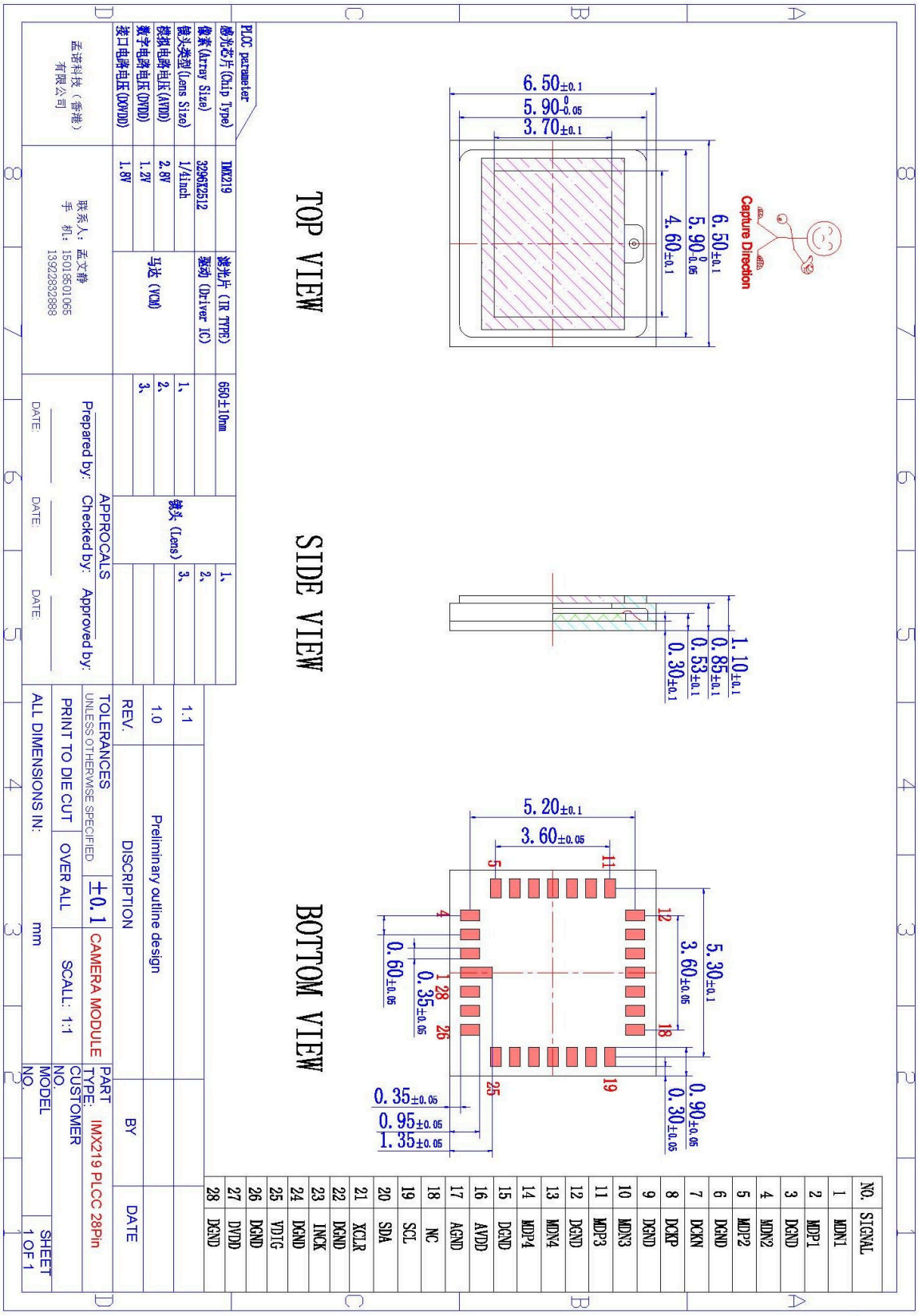

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2、Sensor Specifications

2.1 Description

The IMX219PQH5-C is a diagonal 4.60 mm (Type 1/4.0) CMOS active pixel type image sensor with a square pixelarray and 8.08M effective pixels. This chip operates with three power supplies, analogue 2.8 V, digital 1.2 V, and IF1.8 V, and has low power consumption. High sensitivity, low dark current, and no smear are achieved through theadoption of R, G, and B primary color pigment mosaic filters. This chip features an electronic shutter with variablecharge-storage time.In addition, this product is designed for use in cellular phone and tablet pc. When using this for another application,Sony does not guarantee the quality and reliability of product. Therefore, don't use this for applications other thancellular phone and tablet pc. Consult your Sony sales representative if you have any questions.

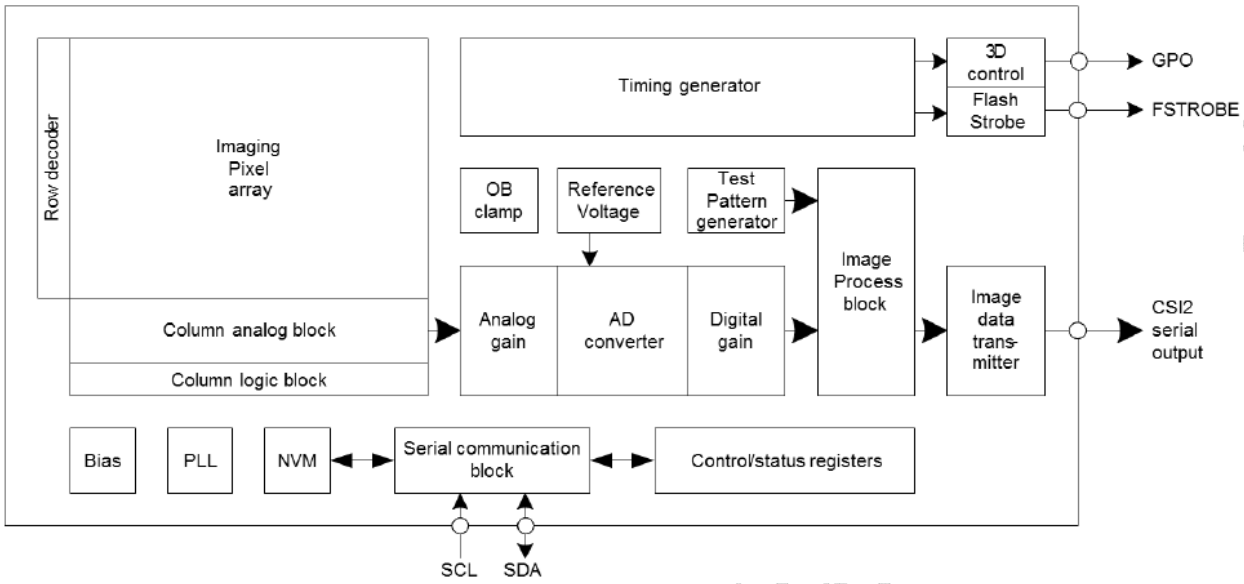
2.2 Features

- Back-illuminated CMOS image sensor Exmor RTM
- 2-wire serial communication circuit on chip
- CSI2 serial data output (selection of 4lane/2lane)
- Timing generator, H and V driver circuits on chip
- CDS/PGA on chip
- 10-bit A/D converter on chip
- Automatic optical black (OB) clamp circuit on chip
- PLL on chip (rectangular wave)
- High sensitivity, low dark current, no smear
- Excellent anti-blooming characteristics
- Variable-speed shutter function (1 H units)
- R, G, B primary color pigment mosaic filters on chip
- Max. 30 frame/s in all-pixel scan mode
- Pixel rate: 280 MHz (All-pixels mode)
- 720p/120 frame/s, 1080p (crop)/30 frame/s
- Data rate: Max. 755 Mbps/lane

2.3 Device Structure

- CMOS image sensor
- Image size : Diagonal 4.60 mm (Type 1/4.0)
- Total number of pixels : 3296 (H) X 2512 (V) approx. 8.28 M pixels
- Number of effective pixels : 3296 (H) X 2480 (V) approx. 8.17 M pixels
- Number of active pixels : 3280 (H) X 2464 (V) approx. 8.08 M pixels
- Chip size : 5.095 mm (H) X 4.930 mm (V) (w/ Scribe)
- Unit cell size : 1.12 µm (H) X 1.12 µm (V)
- Substrate material : Silicon

2.4 Block diagram



Block Diagram

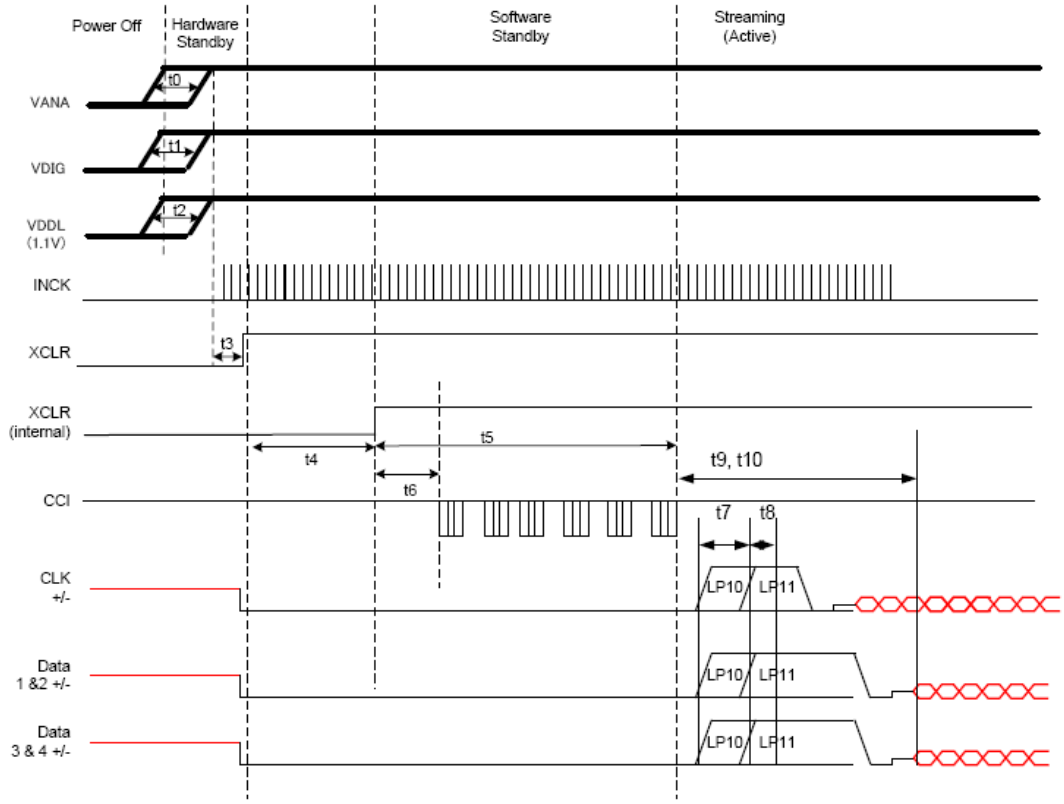
2.5 Power on sequence

Power on sequence of IMX219PQH5-C is below figure.

Startup Sequence in 2-wire Serial Communication Mode

Perform power-on according to the following sequence.

The XCLR pin must be released (Low -> High) after all the power supplies (VANA,VDIG,VDDL) are completed.



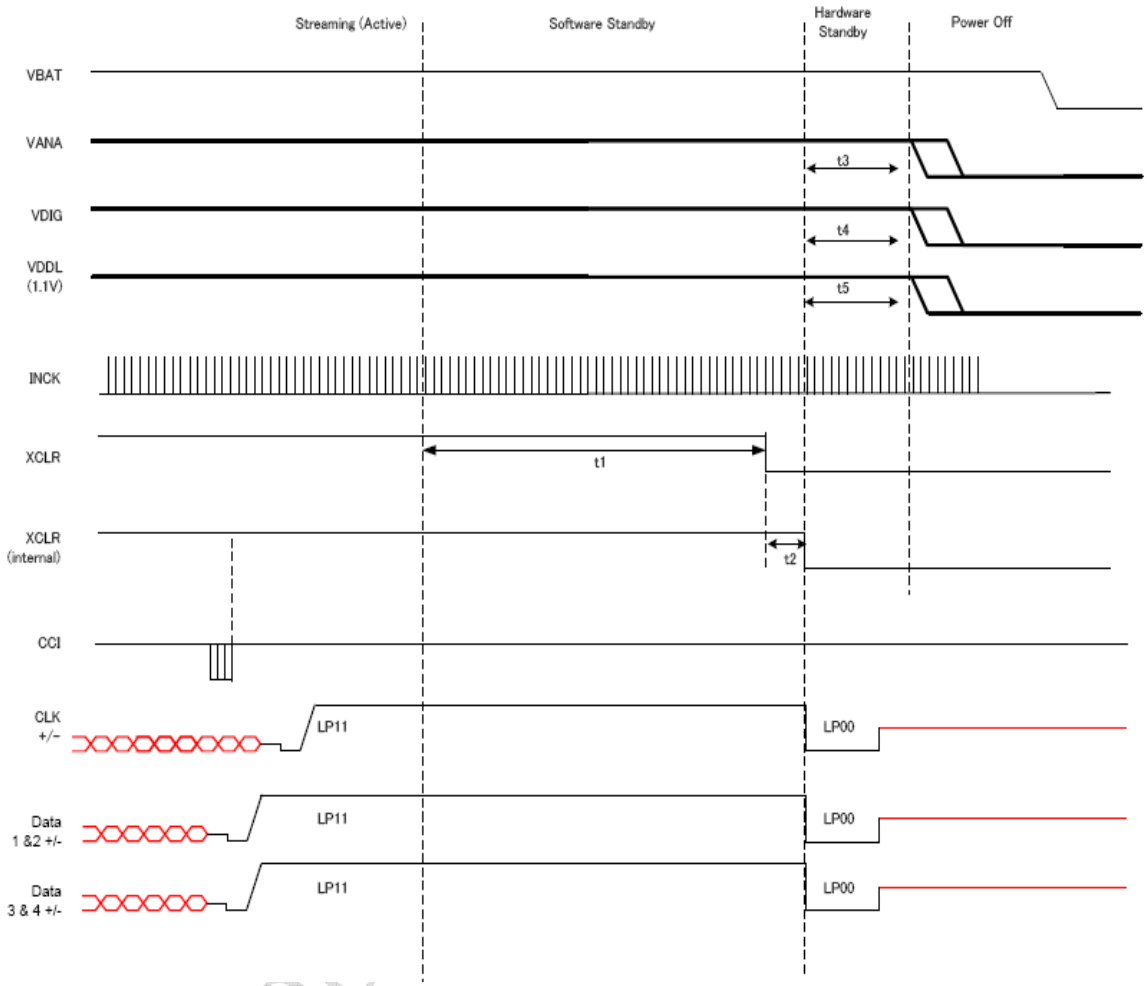
Power-on Sequence in 2-wire Serial Communication Mode

Operation Specifications 2-wire Serial Communication Mode

Constraint	Label	Min.	Max.	Units	Comment
Sequence free of VDDs rising	t0, t1, t2	VANA, VDIG, VDDL may rise in any order.		ns	
XCLR rising	t3	0.5	—	µs	
Internal XCLR is Low to High after VDDs & XCLR supplied	t4		200	µs	
releasing software standby after XCLR Low to High	t5	6	—	ms	charge up VRL
Initializing time of silicon	t6	—	32000	clocks	clock is INCK Case of INCK = 6[MHz], 5.3[msec]
D-PHY power-up	t7	1	1.1	ms	
D-PHY init	t8	100	110	µs	
After releasing software standby to data streaming time	t9	1.2 ms + exposure time	—		
Quick launch up time	t10	—	1	frame	stable time until optimal image quality

2.6 Power off sequence

Perform the power-off in the sequence shown below.



Power-off Sequence in 2-wire Serial Communication

Operation Specifications in 2-wire Serial Communication

Constraint	Label	Min.	Max.	Units	Comment
Software standby - XCLR H → L	t1	0		ns	
Falling time of internal XCLR after XCLR H → L	t2		10	μs	
VANA falling - VDIG falling - VDDL falling	t3,t4,t5	VANA, VDIG and VDDL may fall in any order.		ns	

Can set fast standby mode when fast standby register (0x0106)] set to enable (0x01).
Sequence for fast standby mode;
(1) 0x0106 set to 0x01 (fast standby mode is enable)
(2) 0x0100 set to 0x00 (SW standby)
(3) Can change to SW standby after read out of current line.

2.7 Electrical Characteristics

2.7.1 Absolute Maximum Ratings

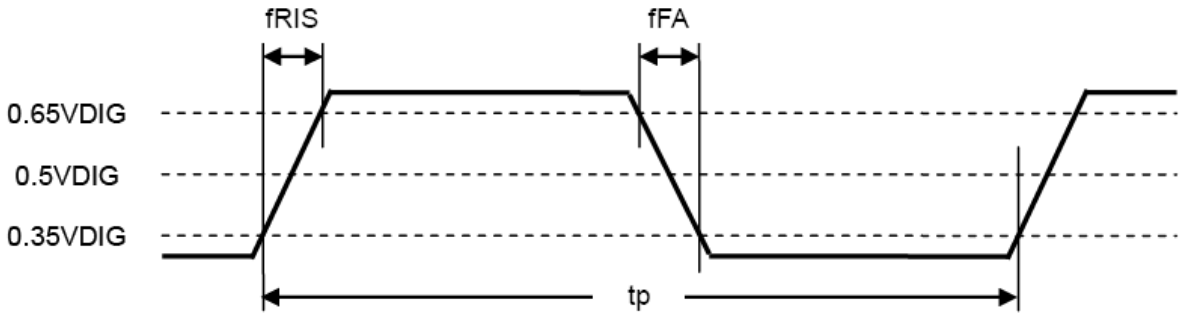
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage (analogue)	V_{ANA}	-0.3		3.3	V	
Supply voltage (Core)	V_{DDL}	-0.3		2.0	V	
Supply voltage (IF)	V_{DIG}	-0.3		3.3	V	
Input voltage	V_I	-0.3		3.3	V	
Output voltage	V_O	-0.3		3.3	V	
Operating temperature (function)	Topr	-20		60	˚C	Junction temperature
Storage temperature	Tstg	-30		80	˚C	Junction temperature
Performance guarantee temperature	Tspec	-20		60	˚C	Junction temperature

2.7.2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage (analogue)	V_{ANA}	2.6	2.8	3.0	V	
Supply voltage (Core)	V_{DDL}	1.08	1.2	1.3	V	
Supply voltage (IF)	V_{DIG}	1.62	1.8	1.98	V	
Analog ripple voltage				20	mVpp	10 kHz-1 MHz needs to be protected by system

2.7.3 AC Characteristics

Input specifications are shown below when square-wave inputs directly into the external pin INCK.



Master Clock Square Waveform Diagram

Master Clock Square Waveform Input Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Comment
Frequency	fSCK	6	18	27	MHz	
jitter (period, peak-to-peak)	Tjitter			600	ps	
Rise Time	fRISE	1		10	ns	
Fall Time	fFALL	1		10	ns	
Duty Cycle	fDUTY	40		60	%	
Input Leakage	fILEAK	-10		10	μA	

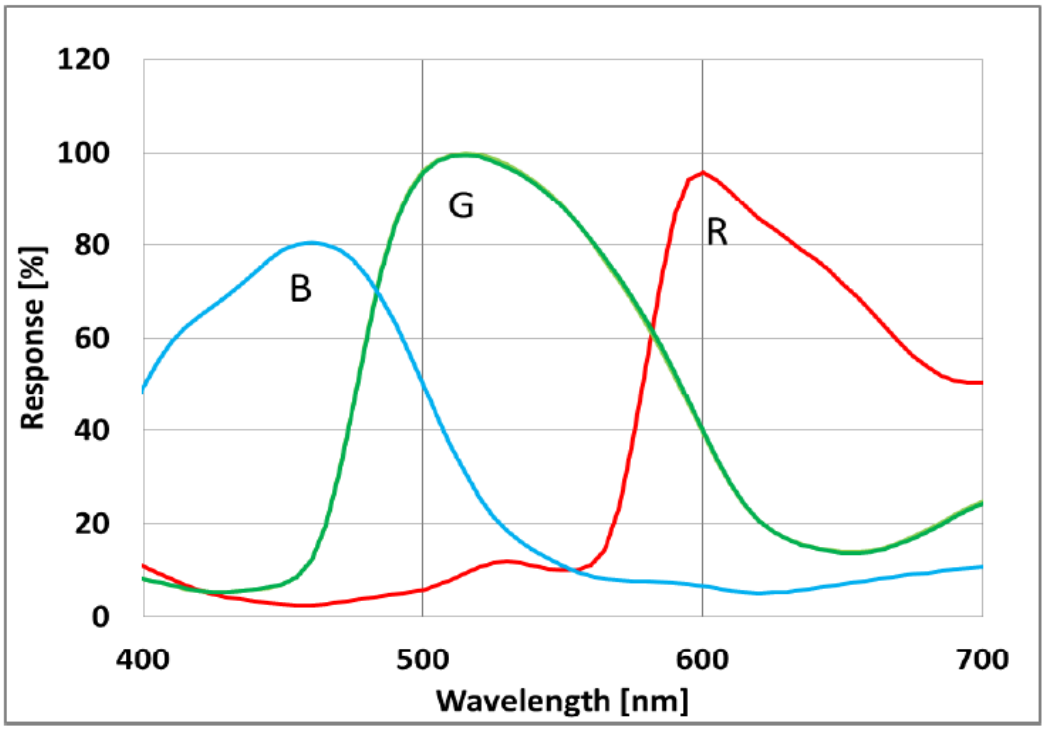
2.7.4 Electrical Characteristics

(V_{ANA} = 3.0 V, V_{DDL} = 1.3 V, V_{DIG} = 1.98 V, Tj = 60 ˚C)

Item	Symbol	Min.	Typ.	Max.	Unit	Comment
Current consumption (Full,30 frame/s)	IVAVA_strm		33	38	mA	VTmax is max speed read out from pixel array CSI2 4 lanes, V_{ANA} current
	IVDDL_strm		100	160	mA	VTmax is max speed read out from pixel array CSI2 4 lanes, V_{DDL} current Defect Correction, L.S.C. function off
HW-Standby current	ISTB_ana			50	μA	XCLR = Lo, V_{ANA} current
	ISTB_dig			10	μA	XCLR = Lo, V_{DIG} current
	ISTB_lddl			50	μA	XCLR = Lo, V_{DDL} current

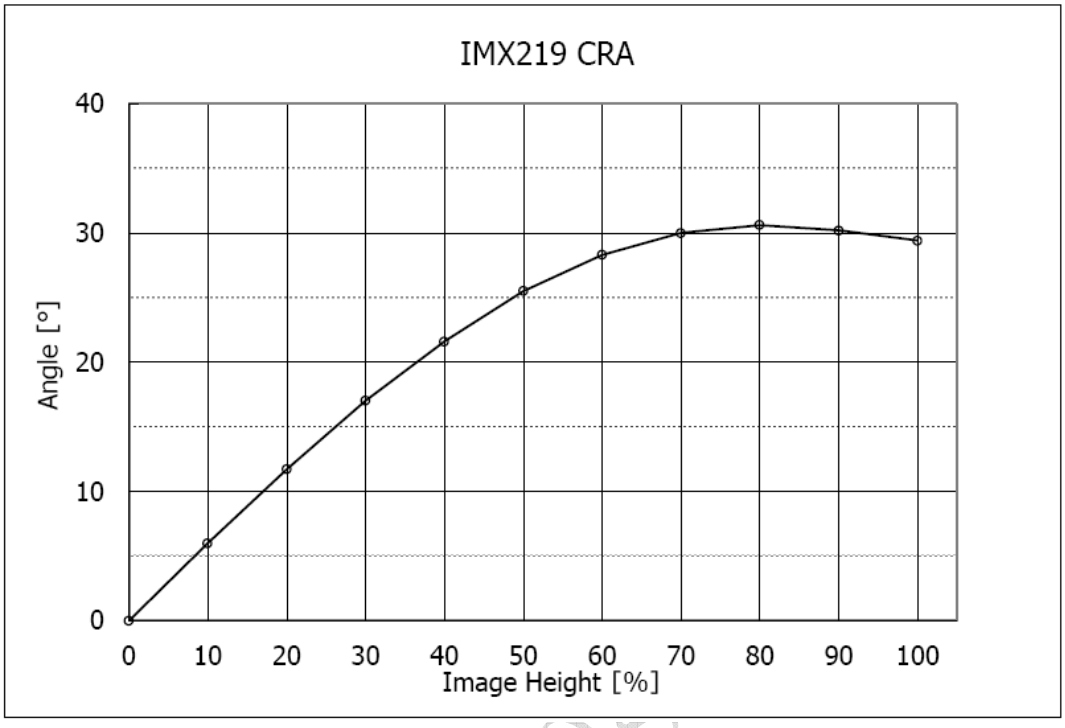
Note) Measurement conditions

2.8 Spectral Sensitivity Characteristic



Spectral sensitivity characteristics

3、Chief Ray Angle Characteristics

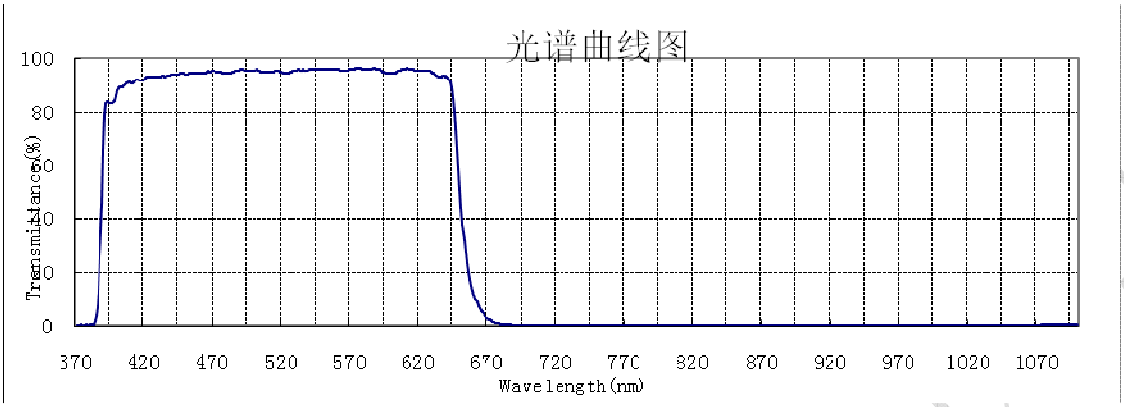


Chief Ray Angle Characteristics

4、PLCC Pin Descriptions

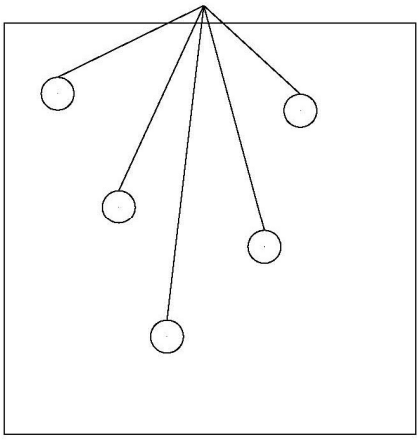
PIN No.	NAME	Type	Description
1	MDN1	Output	MIPI output (data)
2	MDP1	Output	MIPI output (data)
3	DGND	Ground	Ground of digital circuit block
4	MDN2	Output	MIPI output (data)
5	MDP2	Output	MIPI output (data)
6	DGND	Ground	Ground of digital circuit block
7	DCKN	Output	MIPI output (clk)
8	DCKP	Output	MIPI output (clk)
9	DGND	Ground	Ground of digital circuit block
10	MDN3	Output	MIPI output (data)
11	MDP3	Output	MIPI output (data)
12	DGND	Ground	Ground of digital circuit block
13	MDN4	Output	MIPI output (data)
14	MDP4	Output	MIPI output (data)
15	DGND	Ground	Ground of digital circuit block
16	AVDD	Power	Analog power
17	AGND	Ground	Analog ground
18	NC	_	_
19	SCL	Input	SCCB interface input clock
20	SDA	I/O	SCCB interface data pin
21	XCLR	Ground	Shutdown pin
22	DGND	Ground	Ground of digital circuit block
23	INCK	Input	Clock input
24	DGND	Ground	Ground of digital circuit block
25	DOVDD	Power	I/O power
26	DGND	Ground	Ground of digital circuit block
27	DVDD	Power	Digital circuit power
28	DGND	Ground	Ground of digital circuit block

5、IR Schematic



Wavelength [nm]	%T	Wavelength [nm]	%T	Wavelength [nm]	%T	Wavelength [nm]	%T	Wavelength [nm]	%T	Wavelength [nm]	%T	Wavelength [nm]	%T	Wavelength [nm]	%T
370	-0.23	470	95.33	560	95.85	660	11.40	750	0.02	850	0.06	940	0.00	1040	0.03
390	66.26	490	95.78	580	96.12	680	0.74	770	0.00	870	0.00	960	0.01	1060	0.13
410	90.78	510	94.79	600	94.47	700	0.20	790	0.01	890	0.00	980	0.07	1080	0.49
430	93.36	530	95.60	620	95.52	720	0.05	810	0.00	910	0.15	1000	0.03	1100	0.50
450	94.29	550	95.87	640	93.46	740	0.04	830	0.00	930	0.00	1020	0.02		

脏点



备注：

外观说明：

A、脏点<30um （5个以内）允许通过且两点间距>0.5mm

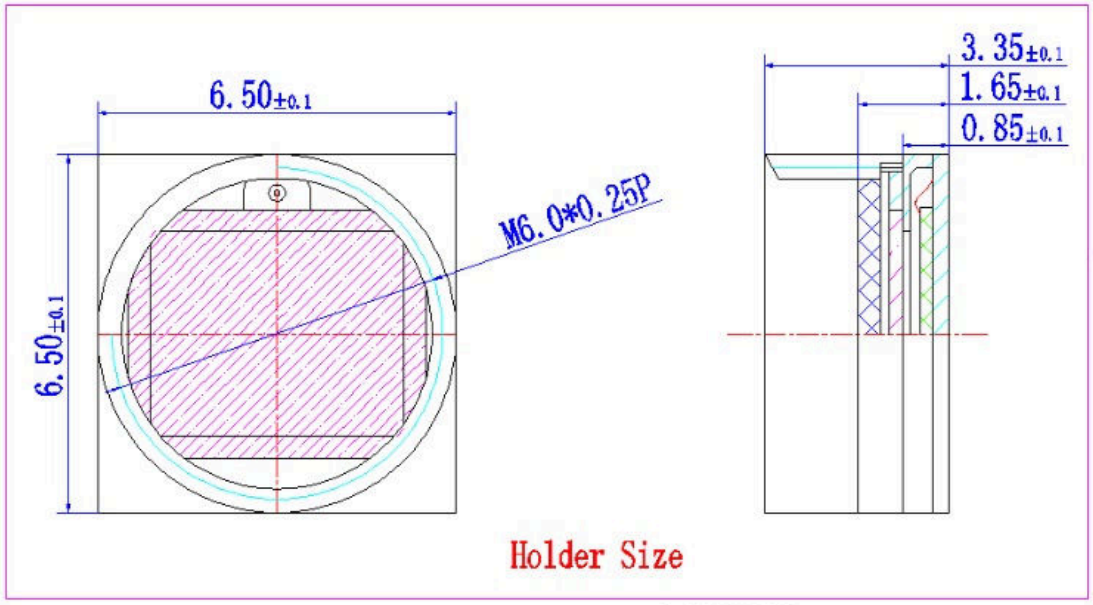
B、脏污不允许(溢胶、水雾、膜印、缺胶)

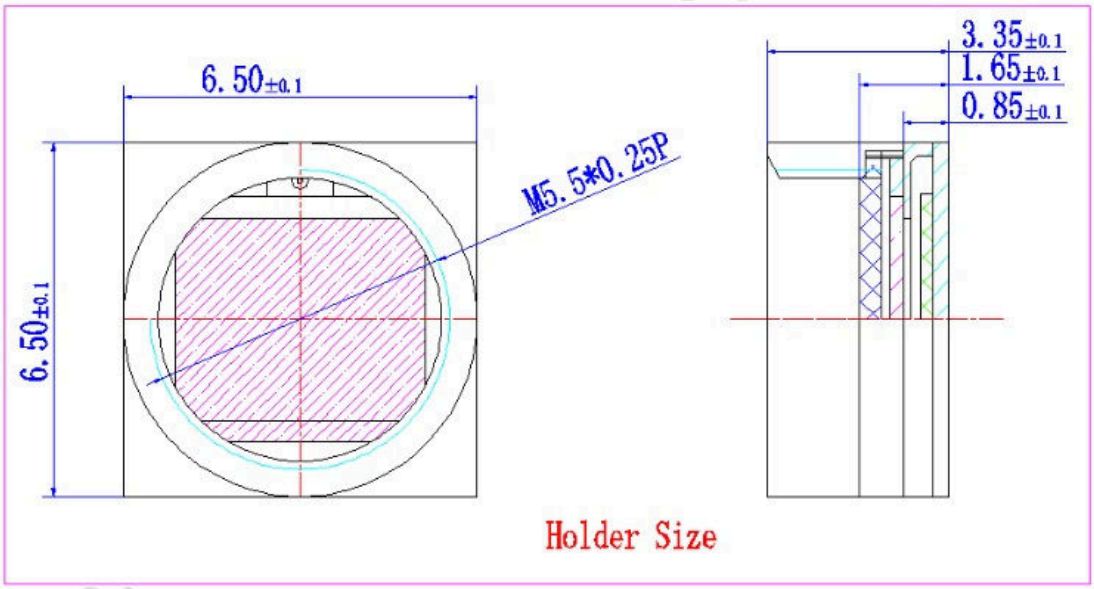
C、伤：宽＜20um ，长＜1/4D;

点（20um）和伤（宽＜20um）加起来不可大于5

D、未遮住感光区允许通过(脏污)

6、Holder





7、Recommend Solution

Lens	Vcm

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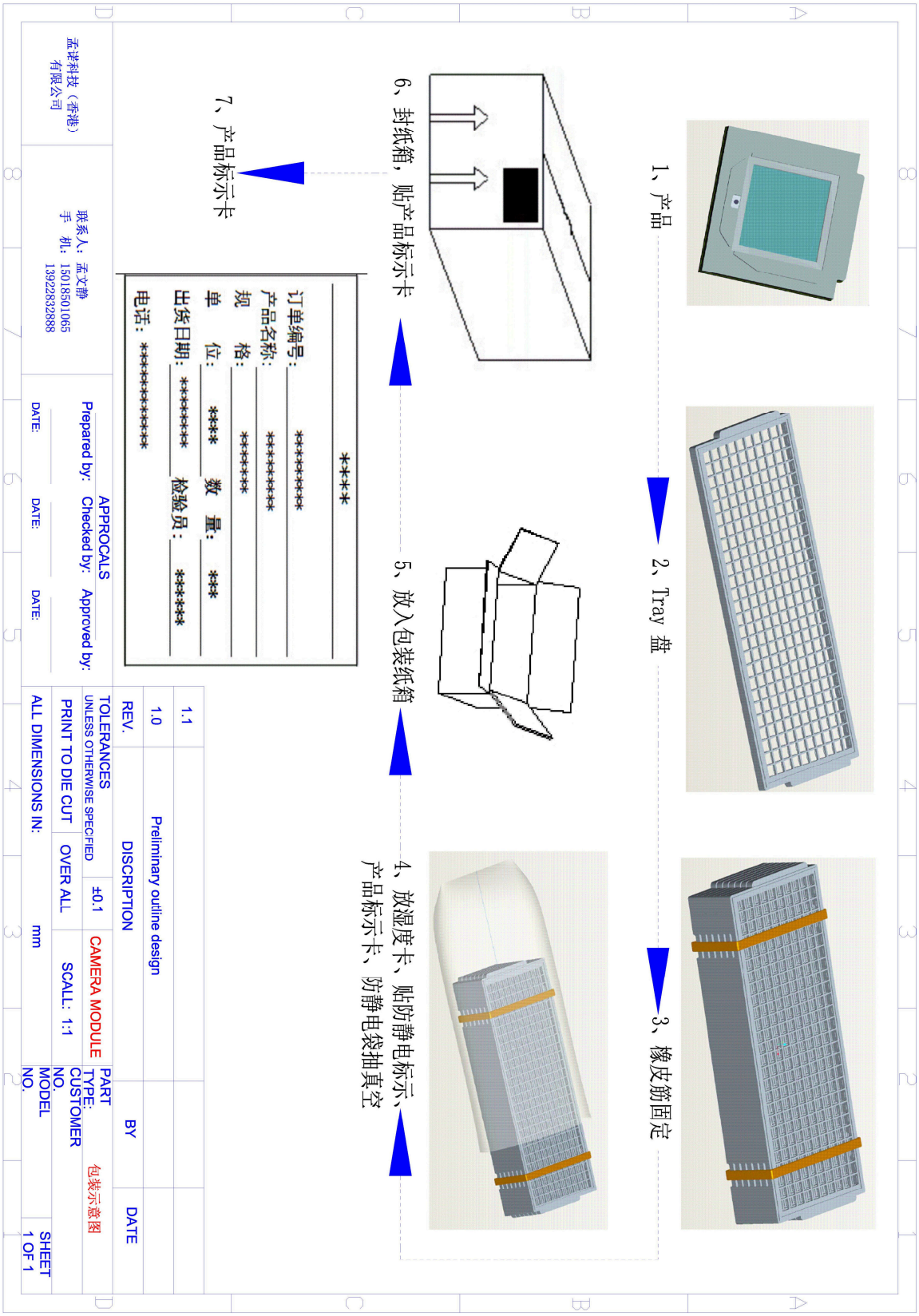
8、Packing specification



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