LEOPARD IMAGING INC

Rev. 1.0

LI-IMX385-MIPI-M12 Data Sheet

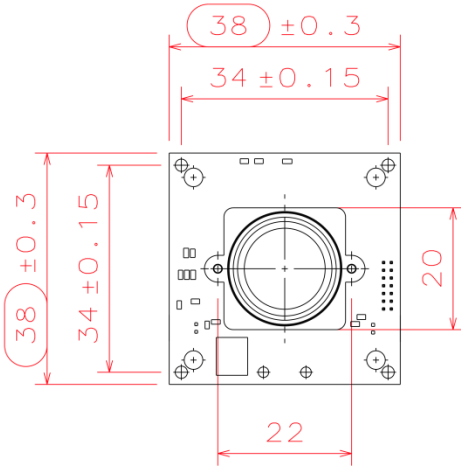
Key Features

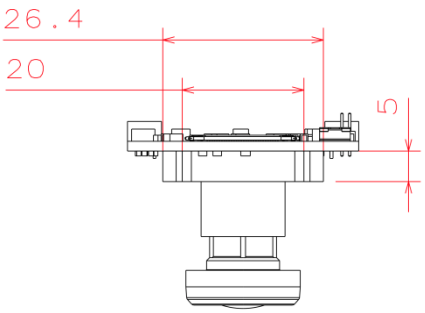
- Sony Diagonal 8.35mm Type 1/2 CMOS Image Sensor IMX385LQR
- Active pixels: 1937H x 1097V
- Pixel size: 3.75 um x 3.75 um
- Color sensor
- Interface: MIPI output
- Support M12 lens
- Module Size: 38mm x 38mm
- Weight:12 g
- Part#: LI-IMX385-MIPI-M12

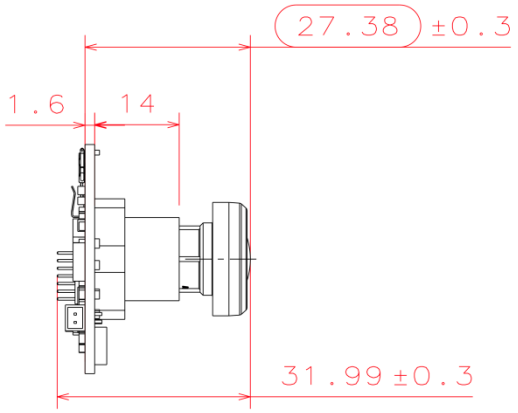
Lens Spec

- Model: SYD1201A
- Focal length: 3.7 mm
- Aperture, F/#: 2.8 +/- 5%
- Built in 650nm IR cut filter
- FOV (D/H/V): 102 °/ 92 °/60 °
- TV Distortion: -1.0 %
- Mount: M12 x P0.5

Dimensions







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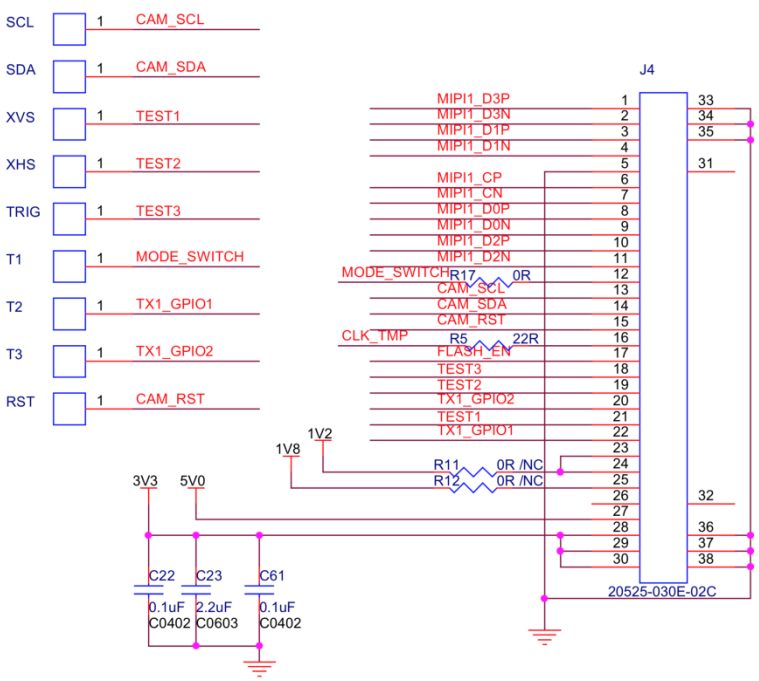
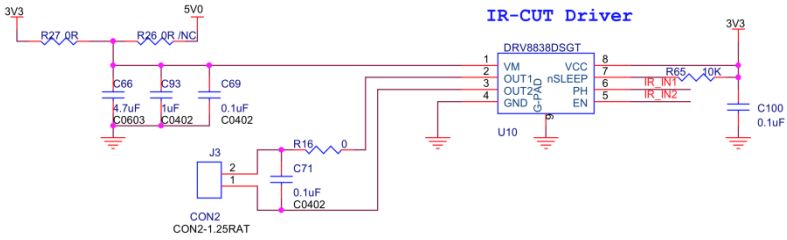
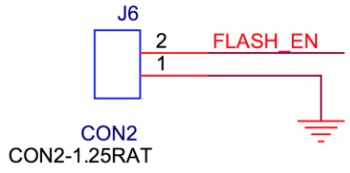
Interfaces

Interfaces	
Interface J4: ▪ Part#: 20525-030E-02C ▪ Number of Positions: 30 ▪ Pitch: 0.4mm ▪ Mating I-PEX cable: FAW-1233-03 (300mm)	
Interface J3: ▪ Part#: 1734829-2 ▪ Number of Positions: 2 ▪ Pitch: 1.25mm	
Interface J6: ▪ Part#: 1734829-2 ▪ Number of Positions: 2 ▪ Pitch: 1.25mm	

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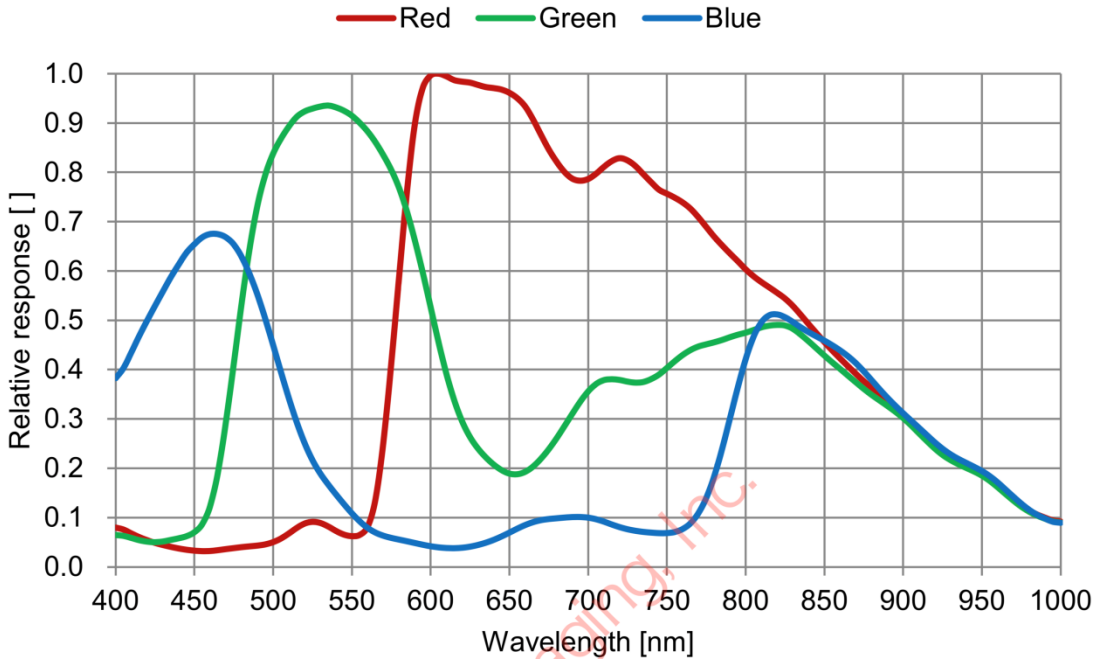
Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage (analog 3.3 V)	AV_{DD}	-0.3	4.0	V	—
Supply voltage (interface 1.8 V)	OV_{DD}	-0.3	3.3	V	—
Supply voltage (digital 1.2 V)	DV_{DD}	-0.3	2.0	V	—
Input voltage	VI	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Output voltage	VO	-0.3	OV_{DD} + 0.3	V	Not exceed 3.3 V
Operating temperature	Topr	-30	85	˚C	—
Storage temperature	Tstg	-40	85	˚C	—

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (analog 3.3 V)	AV_{DD}	3.15	3.30	3.45	V
Supply voltage (Interface 1.8 V)	OV_{DD}	1.70	1.80	1.90	V
Supply voltage (digital 1.2 V)	DV_{DD}	1.10	1.20	1.30	V

Spectral Sensitivity Characteristics



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DC Characteristics

Item		Pins	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	analog	VDDHx	AV_{DD}	—	3.15	3.30	3.45	V
	Interface	VDDMx	OV_{DD}	—	1.70	1.80	1.90	V
	digital	VDDLx	DV_{DD}	—	1.10	1.20	1.30	V
Digital input voltage		XHS XVS XCLR INCK XMASTER OMODE SCK SDI XCE XTRIG	VIH	XVS / XHS Slave Mode	$0.8OV_{DD}$	—	—	V
			VIL		—	—	$0.2OV_{DD}$	V
Digital output voltage		DLOP [A:H] DLOM [A:H] DLCKP DLCKM	VCM	Low voltage LVDS	—	$OV_{DD}/2$	—	V
			VOD	Low voltage LVDS (Termination resistance: 100 Ω)	100	150	220	mV
		XHS XVS SDO TOUT	VOH	XVS / XHS Master Mode	OV_{DD}-0.4	—	—	V
			VOL		—	—	0.4	V

Power Consumption

Item	pin	Symbol	Typ.		Max.		Unit
			Standard luminous intensity	Saturated luminous intensity	Standard luminous intensity	Saturated luminous intensity	
Operating current Low voltage LVDS serial 4 ch 12 bit 60 frame / s All pixel scan mode	VDDH	IAV_{DD}	85	85	140	140	mA
	VDDM	IOV_{DD}	15	15	25	25	mA
	VDDL	IDV_{DD}	80	100	135	170	mA
Operating current MIPI CSI-2 / 4 lane 12 bit 60 frame / s All pixel scan mode	VDDH	IAV_{DD}	85	85	140	140	mA
	VDDM	IOV_{DD}	1	1	5	5	mA
	VDDL	IDV_{DD}	92	112	155	185	mA
Standby current	VDDH	IAV_{DD}_STB	—		0.1		mA
	VDDM	IOV_{DD}_STB	—		0.1		mA
	VDDL	IDV_{DD}_STB	—		14		mA

Operating current: (Typ.) Supply voltage3.3 V / 1.8 V / 1.2 V, Tj = 25 ˚C
(Max.) Supply voltage3.45 V / 1.9 V / 1.3 V, Tj = 60 ˚C, worst state of internal circuit operating current consumption,

Standby: (Max.) Supply voltage3.45 V / 1.9 V / 1.3 V, Tj = 60 ˚C, INCK: 0 V,
The device in the light-obstructed state.

Standard luminous intensity: luminous intensity at 1/3 of the sensor saturated.
Saturated luminous intensity: luminous intensity when the sensor is saturated.

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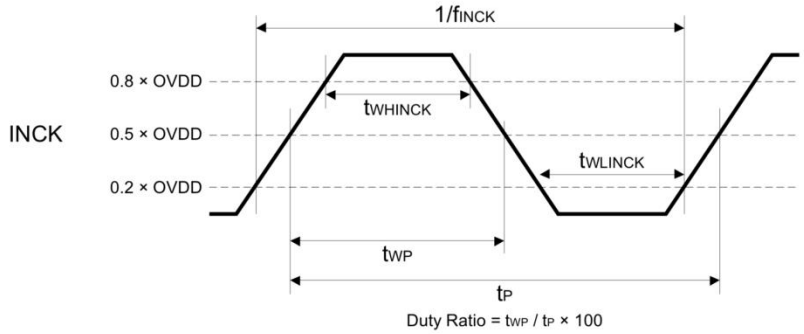
AC Specification

Master Clock Waveform (INCK)

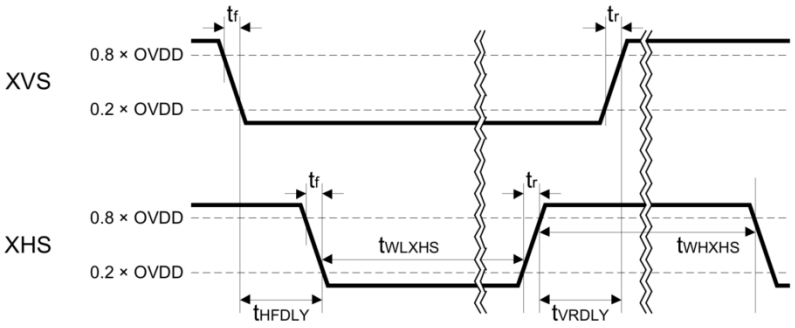


Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
INCK clock frequency	f_{INCK}	f_{INCK} × 0.96	f_{INCK}	f_{INCK} × 1.02	MHz	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK Low level pulse width	t_{WLINCK}	4	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK High level pulse width	t_{WHINCK}	4	—	—	ns	f_{INCK} = 37.125 MHz, 74.25 MHz
INCK clock duty	—	45.0	50.0	55.0	%	Define with 0.5 × OV_{DD}

*The INCK fluctuation affects the frame rate.

XVS / XHS Input Characteristics In Slave Mode (DMODE pin = High)



Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
XHS Low level pulse width	t_{WLXHS}	4 / f_{INCK}	—	—	ns	—
XHS High level pulse width	t_{WHXHS}	4 / f_{INCK}	—	—	ns	—
XVS - XHS fall width	t_{HFDLY}	1 / f_{INCK}	—	—	ns	—
XHS - XVS rise width	t_{VRDLY}	1 / f_{INCK}	—	—	ns	—
XVS, XHS rise time	t_r	—	—	5	ns	20 % to 80 %
XVS, XHS fall time	t_f	—	—	5	ns	80 % to 20 %

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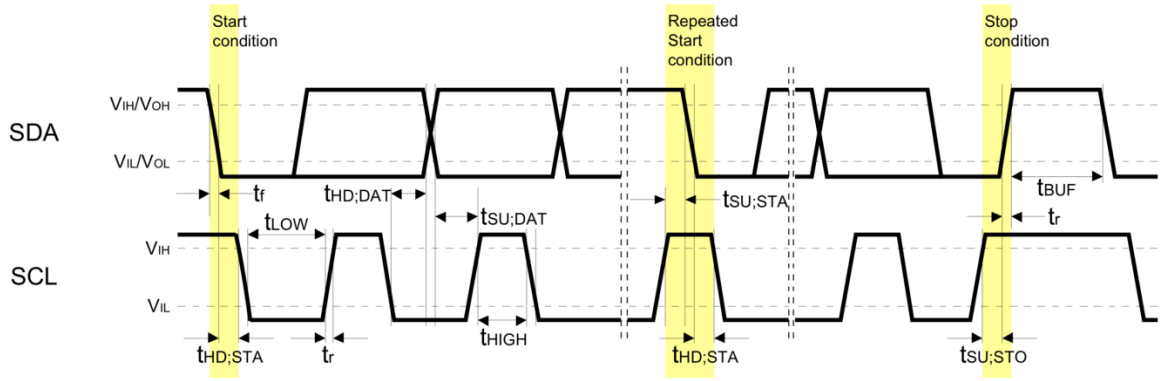
I²C Communication



I²C Specification

Item	Symbol	Min.	Typ.	Max.	Unit	条件
Low level input voltage	VIL	-0.3	—	0.3 × OVDD	V	—
High level input voltage	VIH	0.7 × OVDD	—	1.9	V	—
Low level input voltage	VOL	0	—	0.2 × OVDD	V	OVDD < 2 V, Sink 3 mA
High level input voltage	VOH	0.8 × OVDD	—	—	V	—
Output fall time	tof	—	—	250	ns	Load 10 pF – 400 pF, 0.7 × OVDD – 0.3 × OVDD
Input current	Ii	-10	—	10	μA	0.1 × OVDD – 0.9 × OVDD
Capacitance for SCK (SCL) /SDI (SDA)	Ci	—	—	10	pF	—

I²C AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	400	kHz
Hold time (Start Condition)	$t_{HD;STA}$	0.6	—	—	μs
Low period of the SCL clock	t_{LOW}	1.3	—	—	μs
High period of the SCL clock	t_{HIGH}	0.6	—	—	μs
Set-up time (Repeated Start Condition)	$t_{SU;STA}$	0.6	—	—	μs
Data hold time	$t_{HD;DAT}$	0	—	0.9	μs
Data set-up time	$t_{SU;DAT}$	100	—	—	ns
Rise time of both SDA and SCL signals	t_r	—	—	300	ns
Fall time of both SDA and SCL signals	t_f	—	—	300	ns
Set-up time (Stop Condition)	$t_{SU;STO}$	0.6	—	—	μs
Bus free time between a STOP and START Condition	t_{BUF}	1.3	—	—	μs

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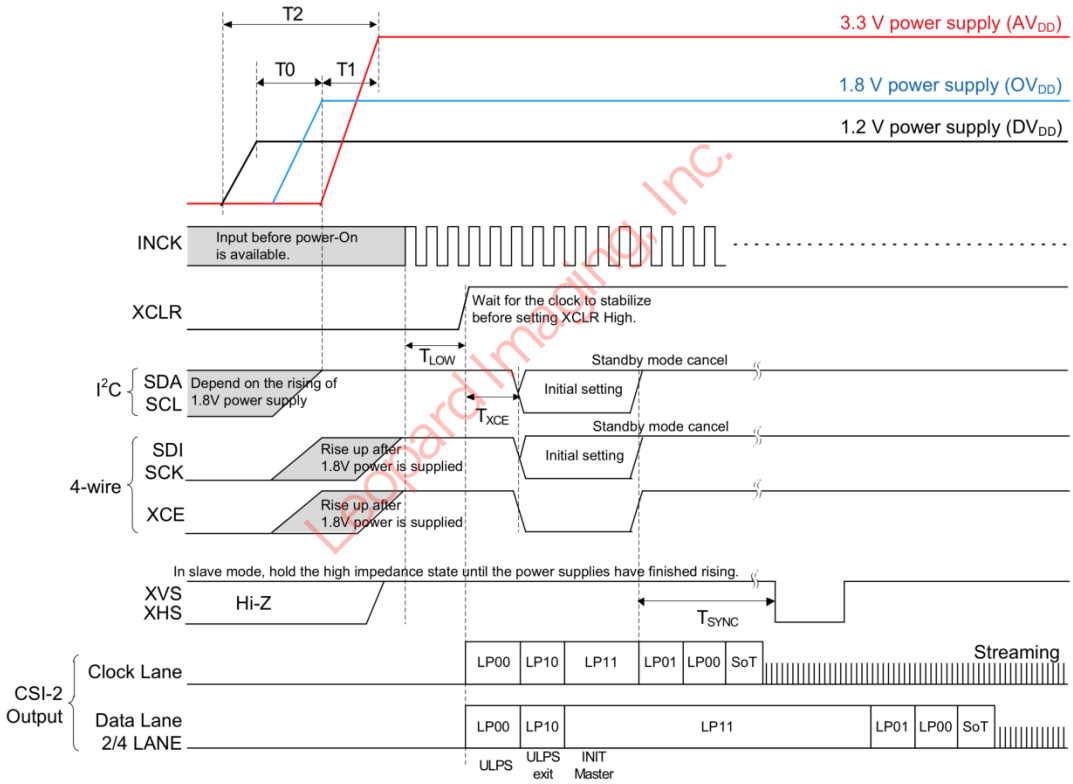
Power-on Sequence

1. Turn On the power supplies so that the power supplies rise in order of 1.2 V power supply (DV_{DD}) →1.8 V power supply (OV_{DD}) → 3.3 V power supply (AV_{DD}). In addition, all power supplies should finish rising within 200 ms.
2. Start master clock (INCK) input after turning On the power supplies.
3. The register values are undefined immediately after power-on, so the system must be cleared. Hold XCLR at Low level for 500 ns or more after all the power supplies have finished rising. (The register values after a system clear are the default values.) In addition, hold XCE to High level during this period. Rise XCE after 1.8 V power supply (OV_{DD}).
4. The system clear is applied by setting XCLR to High level. However, the maser clock needs to stabilize before setting the XCLR pin to High level.
5. Make the sensor setting by register communication after the system clear. A period of 20 µs or more should be provided after setting XCLR High before inputting the communication enable signal XCE. In I^2C communication, XCE is fixed to High.



Item	Symbol	Min.	Max.	Unit
1.2 V power supply rising → 1.8 V power supply rising	T0	0	—	ns
1.8 V power supply rising → 3.3 V power supply rising	T1	0	—	ns
Rising time of all power supply	T2	—	200	ms
INCK active → Clear OFF	T_{LOW}	500	—	ns
Clear OFF → Communication start	T_{XCE}	20	—	µs
Standby OFF (communication) → External input XHS,XVS (slave mode only)	T_{SYNC}	20	—	ms

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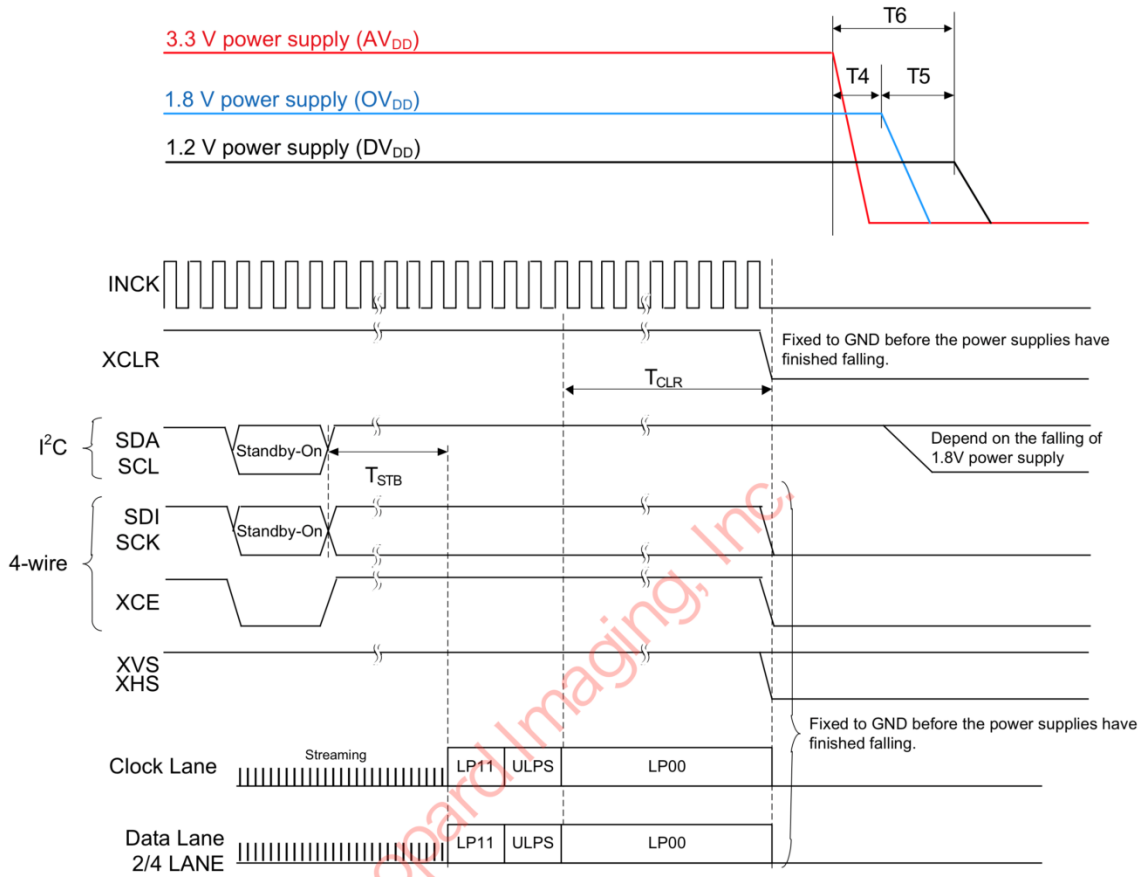
Power-off Sequence

Turn Off the power supplies so that the power supplies fall in order of 3.3 V power supply (AV_{DD}) → 1.8 V power supply (OV_{DD}) → 1.2 V power supply (DV_{DD}). In addition, all power supplies should falling within 200 ms. Set each digital input pin (INCK, XCE, SCK, SDI, XCLR, XMASTER, OMODE, XVS, XHS) to 0 V before the 1.8 V power supply (OV_{DD}) falls.



Item	Symbol	Min.	Max.	Unit
Standby ON (communication) → LP11 mode start	T_{STB}	Until FE		—
LP00 → XCLR falling	T_{CLR}	128	—	cycle
3.3 V power shut down → 1.8 V power shut down	T4	0	—	ns
1.8 V power shut down → 1.2 V power shut down	T5	0	—	ns
Shut down time of all power supply	T6	—	200	ms

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